

Stratix IV-HardCopy IV-Quartus II v.8.0 FAQ

Stratix IV FPGAs and HardCopy IV ASICs

Q: What are you announcing today?

A: Altera is announcing the industry's first 40-nm FPGAs and HardCopy® ASICs. The Stratix® IV FPGAs and HardCopy IV ASICs, both with transceivers options, provide unprecedented densities, performance, and low-power leadership.

Q: What applications are you targeting for these 40-nm devices?

A: Altera® 40-nm devices meet the diverse high-end application needs of a large number of markets such as wireless and wireline communications, military, broadcast, and ASIC prototyping.

Q: What are the benefits of 40 nm versus 45 nm?

A: The 40-nm process provides higher density, lower power per function, and lower cost.

Q: What is the highest density part in the Stratix IV family?

A: The Stratix IV family has up to 680K logic elements, which is 2X bigger than Altera's Stratix III family, currently the largest FPGA on the market.

Q: How many transceivers does Stratix IV GX offer?

A: The Stratix IV GX FPGAs offer up to 48 transceivers operating at up to 8.5 Gbps, which provides designers with the industry's highest available bandwidth, more than twice the bandwidth of any other FPGA.

Q: Have transceivers been available with previous HardCopy ASIC families?

A: This is the first time Altera is offering a transceiver-based ASIC option.

Q: When can customers start to design with Stratix IV FPGAs?

A: Customers can immediately start designing Stratix IV devices with Quartus® II design software v8.0.

Q: When can I get devices?

A: Engineering samples of the first member of the Stratix IV device family will be available in the fourth quarter of 2008.

Q: What is Programmable Power Technology?

A: Programmable Power Technology is Altera's patented power saving technology that optimizes logic, DSP, and memory blocks to maximize performance where needed while delivering the lowest power elsewhere in the design.

Quartus II/IP

Q: What is new in Quartus II design software v8.0?

A: Quartus II software version 8.0 delivers unprecedented performance and productivity for high-density FPGAs, and is the first FPGA vendor software to support 40-nm devices with Stratix IV FPGAs. Version 8.0 introduces many new features and enhancements including a design partition planner, a tasks window, expanded SOPC Builder, and enhanced FPGA I/O planning.

Q: What are incremental compilation and the design partition planner in Quartus II software?

A: With incremental compilation, only partitions in your designs that have been modified are recompiled. The graphical interface of the design partition planner helps designers create better partitions for their designs and get the most out of incremental compilation. The Quartus II software's incremental compilation feature and design partition planner enable designers to reduce their compilation by up to 70 percent.

Q: What new IP cores do you have and what are they?

A: There are six new intellectual property (IP) products and many new feature enhancements. PCI Express hard IP, which supports generations 1.0, 1.1, and 2.0 of the protocol standard, has been added to the portfolio in support of the new Stratix IV GX FPGAs. Also five new video and image processing cores have been added to the Video and Imaging Suite: clocked video input and output, frame buffer, clipper, and color frame sequencer. In addition, feature enhancements have been made to the soft PCI Express, Triple-Speed Ethernet, Serial RapidIO[®], Nios[®] II processor, SDI, SerialLite II, and memory controller IP products.