SOPC DESIGN CONFERENCE 2002

High-Speed Board Design Tutorial

What Is High Speed?

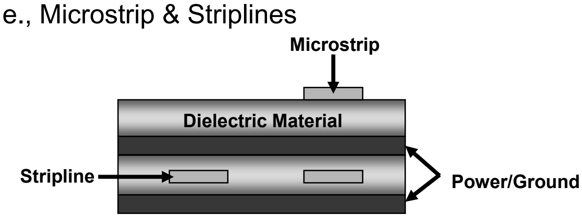
- Definition of High Speed Has Changed with Technology
  - 1990: 50 MHz
  - 1995: 200 MHz
  - 2002: 1.25 – 3.125 Gbps or More
- Faster Systems Require More Attention to Detail

Agenda

- Ideal Transmission Lines
- Termination
- Lossy Transmission Lines
- Pre-Emphasis & Equalization
- Simulation (Using HyperLynx)
- References
- Summary

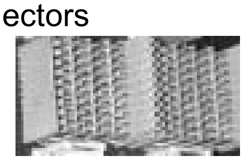
Wires

- Wires in Digital Systems Consist of
  - Traces on PC Boards & Backplanes
    - i.e., Microstrip & Striplines



  - Conductors in Cables & Connectors

Coaxial Cable



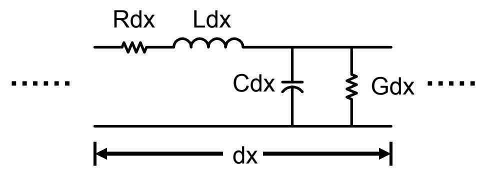
Tyco VHDM Connectors

Wire Model

- Traditional Wire Model - Ideal
  - No Capacitance, Inductance or Resistance

Traditional Wire Representation

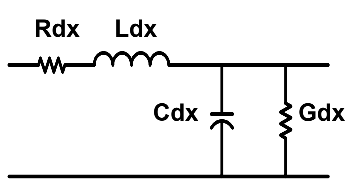
- High-Speed Analysis
  - Model Wire as Infinitesimal Segments of Resistance-Inductance-Conductance-Capacitance (RLGC) Elements



Infinitesimal Segment of a Wire Modeled as RLGC Circuit

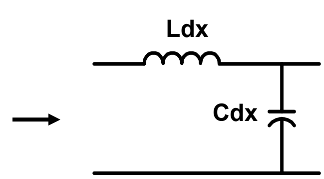
Lossless Transmission Line Model

- R & G Significantly Small
  - Omitted for First-Order Approximation
  - No Line Losses from Dissipation
- R & G Components of Impedance Significant Only for High-Frequency or Lossy Lines



RLGC Wire Representation

$$Zo = \left(\frac{R + Ls}{G + Cs}\right)^{1/2}$$



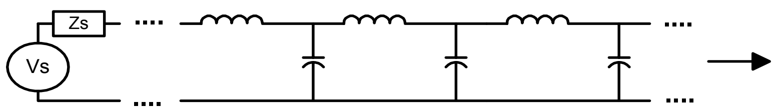
First Order Approximation Wire Representation

$$Zo = \left(\frac{L}{C}\right)^{1/2}$$

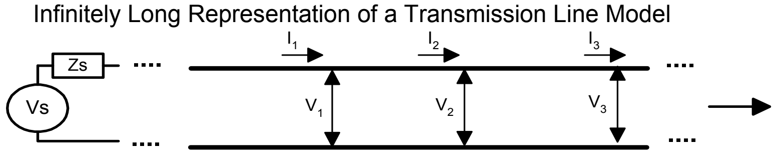
Characteristic Impedance

- Characteristic Impedance (Z_O) of Transmission Line
  - Ratio of Voltage & Current Waves at Any Point of Line

$$Z_O = \left(\frac{L}{C}\right)^{1/2} = \left(\frac{V}{I}\right)$$



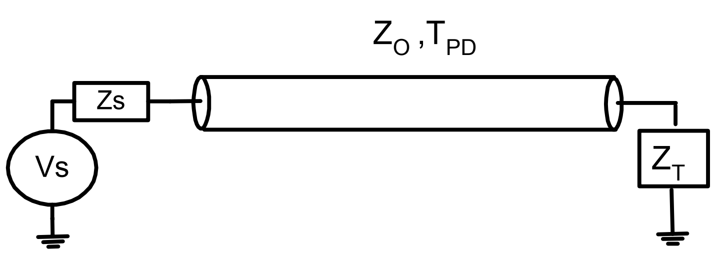
Infinitely Long Representation of a Transmission Line Model



Infinitely Long Representation of a Transmission Impedance

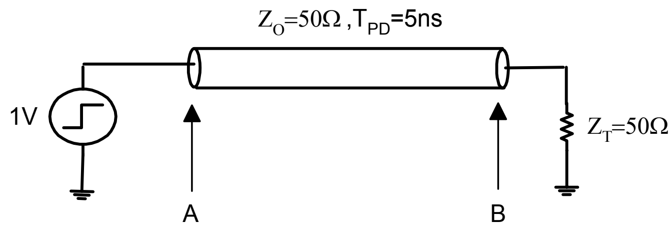
Transmission Line Representation

- Transmission Line Characteristics
  - Characteristic Impedance, Z_O
  - Length (Propagation Delay), T_{PD}



Transmission Line Basic Rules

- Three Basic Rules for Transmission Line Analysis
  - Waves Propagate on Line
    - Both Directions
  - Waves Reflect Unless Terminated
  - Voltage Is Superposition of Waves



Later Slides Show Simulation Example

Agenda

- Ideal Transmission Lines
- Termination
- Lossy Transmission Lines
- Pre-Emphasis & Equalization
- Simulation (Using HyperLynx)
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- Summary

Termination Circuits

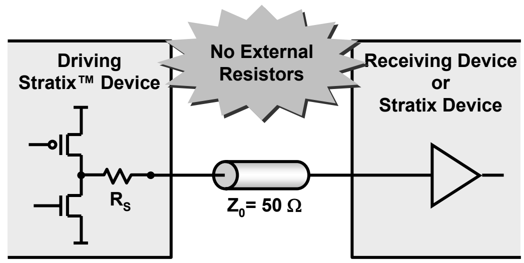
- Many Common Termination Circuits
  - Parallel Termination
  - Series Termination
  - Thevenin Load Termination
  - Active Load Termination
  - Fly-By Termination
  - Differential Termination

Stratix Terminator Technology

- On-Chip Termination Resistors
  - Dynamically Adjust with Voltage & Temperature
  - Two Reference Resistors Required for Each I/O Bank
- Each I/O Bank is All Parallel or All Series
  - External Resistors Must be Used if Both Series & Parallel Termination Required

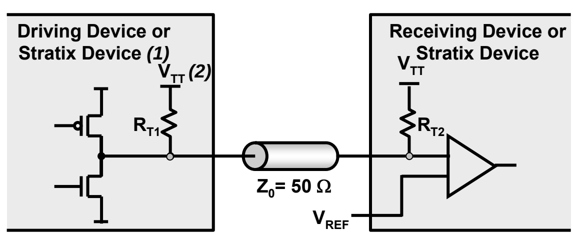
Termination Type	Top & Bottom I/O Banks	Left & Right I/O Banks
Series / Impedance Matching (R_s)	✓	✓
Parallel (R_t)	✓	
Differential		✓

Series Termination & Impedance Matching



I/O Standard	R_S
3.3-/2.5-/1.8-V LVTTL	25 or 50 Ω
3.3-/2.5-/1.8-V LVCMOS	25 or 50 Ω
SSTL-2/-3 Class I	25 Ω
SSTL-2/-3 Class II	25 Ω

Parallel Termination



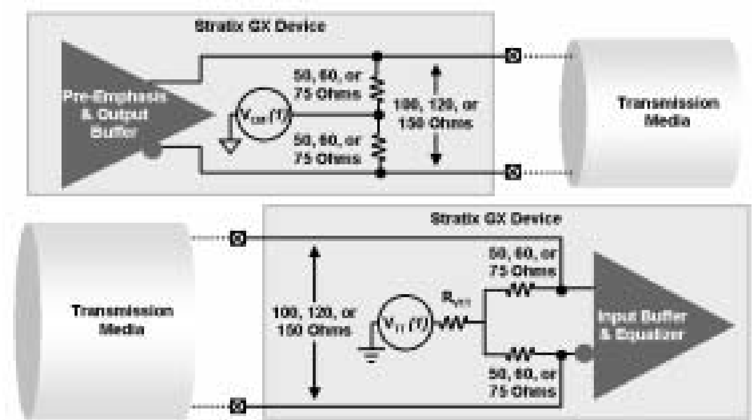
(1) HSTL Class II Pin Example
(2) Internally Generated

I/O Standard	R_{T1}	R_{T2}
SSTL-2/-3 Class I	-	50 Ω
SSTL-2/-3 Class II	50 Ω *(3)*	50 Ω
HSTL Class I	-	50 Ω
HSTL Class II	50 Ω	50 Ω
GTL / GTL+	50 Ω	50 Ω
CTT	-	50 Ω

(3) Driver Uses On-Chip Series & External Parallel Termination Resistors

Stratix GX Differential Termination

- Stratix GX Offers On-Chip Differential Termination
  - Both Transmitter & Receiver



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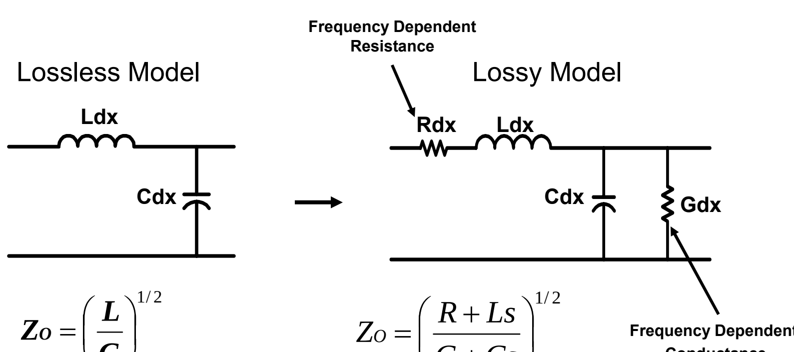
Lossy Transmission Lines

- High-Frequency Signals Subject to Losses within Transmission Medium
  - Skin Effect Causes Frequency-Dependent Series Resistance
  - Dielectric Absorption Causes Frequency-Dependent Conductance
- Both Skin Effect & Dielectric Absorption Increase High-Frequency Attenuation

Lossy Transmission Line Model

- Cannot Omit R & G When Analyzing Lossy Transmission Lines

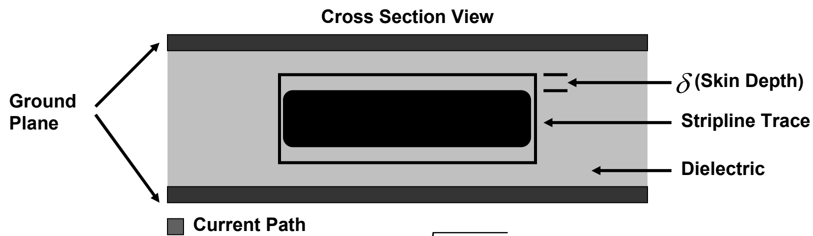


$$Zo = \left(\frac{L}{C}\right)^{1/2}$$

$$Zo = \left(\frac{R+Ls}{G+Cs}\right)^{1/2}$$

Skin Effect

- High-Frequency Current Flows Primarily on Conductor Surface
- Changing Current Distribution Increases Resistance as Function of Frequency



$$\delta = \sqrt{\frac{\rho}{\pi F \mu}}$$

ρ — Resistivity; μ — Permeability of Free Space; F — Frequency

Dielectric Absorption

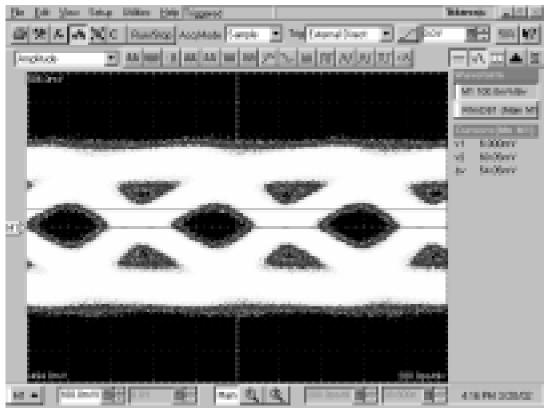
- High-Frequency Signals Excite Insulator Molecules
  - Attenuate Signal
- Dielectric Absorption Often Specified as Loss Tangent tan(δ)
- Lower tan(δ) = Less Loss

List of Common Dielectric Material Loss Tangents

Material	tan(δ) at 1MHz
FR4	0.035
Polyamide	0.025
GETEK	0.010
Teflon	0.001

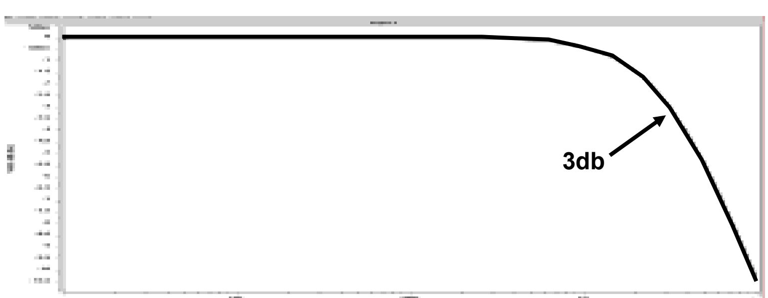
Why Are Losses Important?

- Transmission Line Losses Attenuate Eye Diagram
  - Reduces Noise Margins



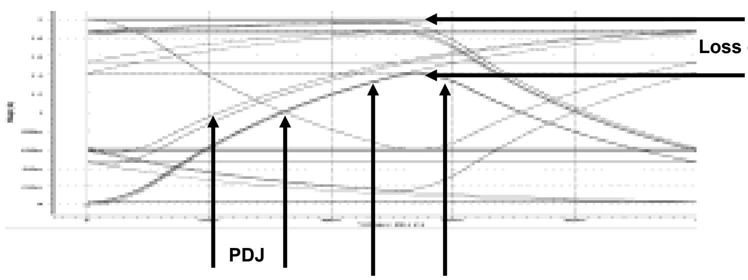
Effects of Lossy Line

- Effect 1: IR Loss (Frequency Attenuation)
  - Caused by Skin Effect Increasing Resistance for High Frequency Signals
  - Simulate Frequency Response as Low Pass Filter



Effects of Lossy Line

- Effect 2: Pattern-Dependent Jitter (PDJ)
  - Due to Intersymbol Interference (ISI)
  - Rise & Fall Times Affected by Data Sequence



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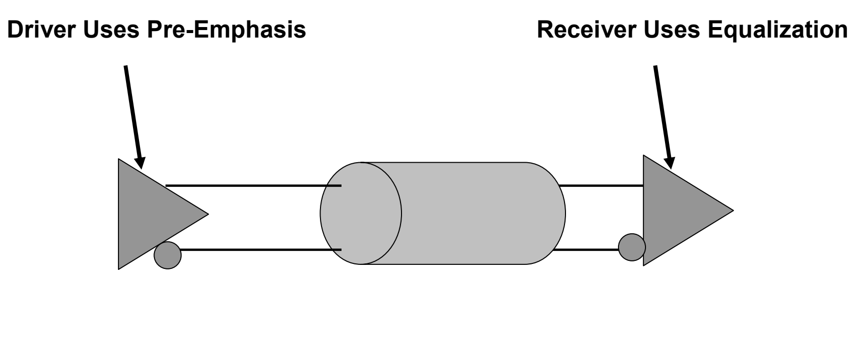
Compensate for Lossy Line

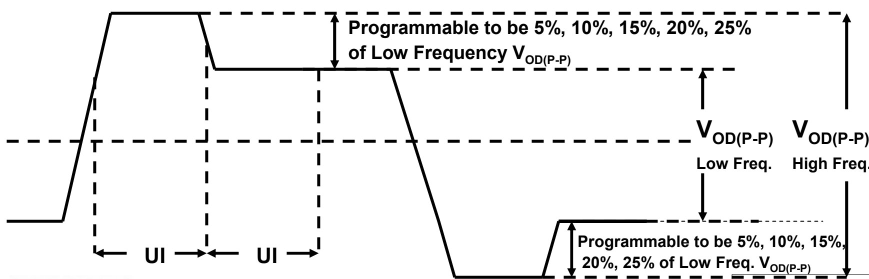
- Compensate for Losses, Boost High-Frequency Components
- Increasing Overall Signaling Level Causes Negative Effects
  - Increases Proportional Noise
  - Increases Pattern-Dependent Jitter
  - Increases Power Consumption

Pre-Emphasis & Equalization

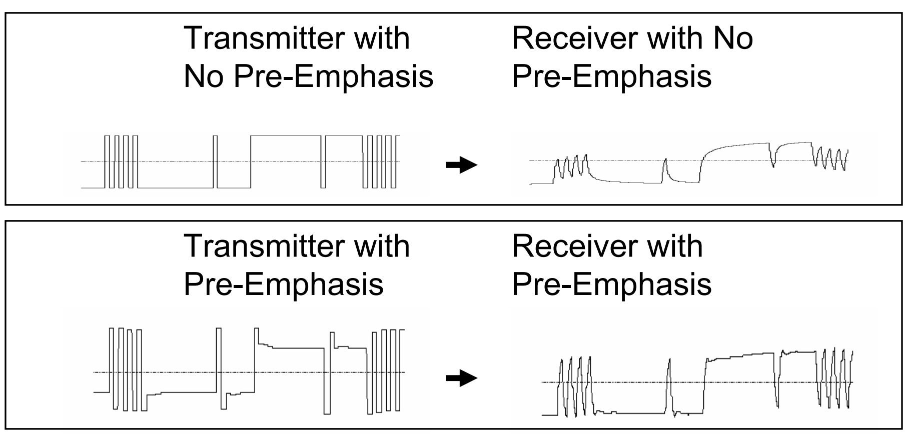


Pre-Emphasis Theory

- Reduce PDJ, Increase (Pre-Emphasize) High-Frequency Components
  - When Signal Switches, Increase Differential Swing
  - When Run Length Exceeds One, Signal Is De-Emphasized to Lower Voltage Level



Pre-Emphasis Example 1

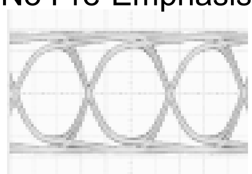


Signal Transmitted over 1-m, 5-mil Stripline

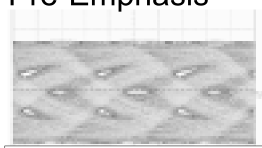
Digital Systems Engineering, William J. Dally & John W. Poulton, Pg 365

Pre-Emphasis Example 2

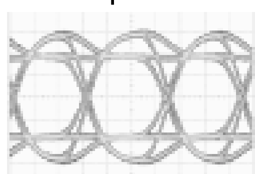
Transmitter with No Pre-Emphasis



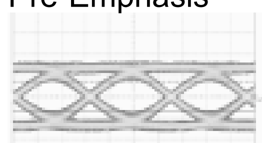
Receiver with No Pre-Emphasis



Transmitter with Pre-Emphasis



Receiver with Pre-Emphasis



Digital Systems Engineering, William J. Dally EE273, L8, Feb 06, 2002

Stratix GX Programmable Pre-Emphasis

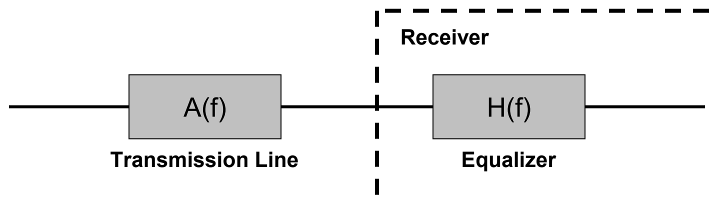
- Support for 0% to 25% Pre-Emphasis on Transmitter Channels
  - Maximum Limit for $V_{OD(peak\text{-}to\text{-}peak)}$ Is 1,600 mV

Original VOD	V_{OD} with Pre-Emphasis *(1)*				
	5%	10%	15%	20%	25%
400	420	440	460	480	500
480	504	528	552	576	600
600	630	660	690	720	750
800	840	880	920	960	1000
960	1008	1056	1104	1152	1200
1,000	1050	1100	1150	1200	1250
1,200	1260	1320	1380	1440	1500
1,400	1470	1540			
1,440	1512	1584			
1,500	1575				
1,600					

(1) Calculated as a Percentage of Original V_{OD} Setting

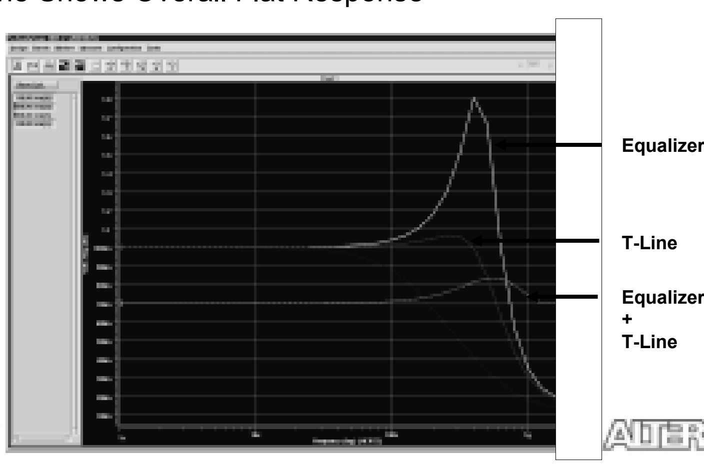
Programmable Equalization

- Receiver Uses Programmable Equalization to Boost High-Frequency Gain
  - Negates Effect of High-Frequency Losses
- Stratix GX Equalizer Compensates for 20” or 40” of FR4 Trace
  - Boosts Signals Up to 9 dB



Equalization Effect

- Equalizer Successfully Compensates for Transmission Line Attenuation
- Blue Line Shows Overall Flat Response



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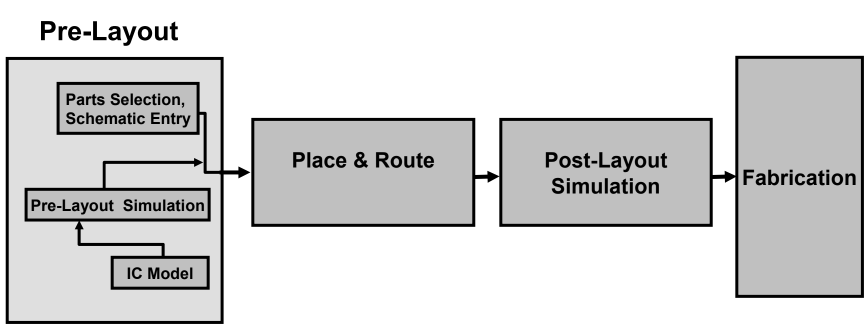
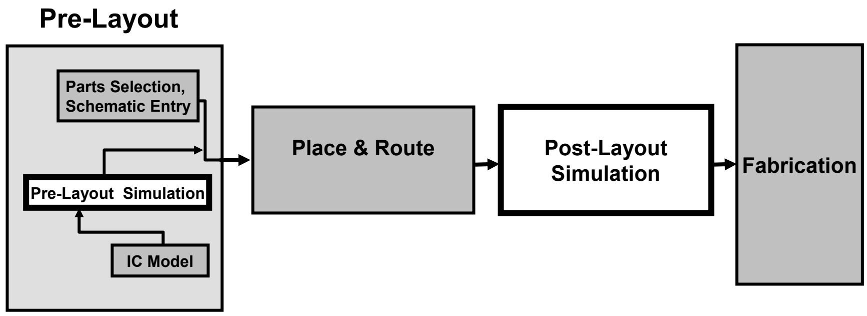
PCB Design Flow



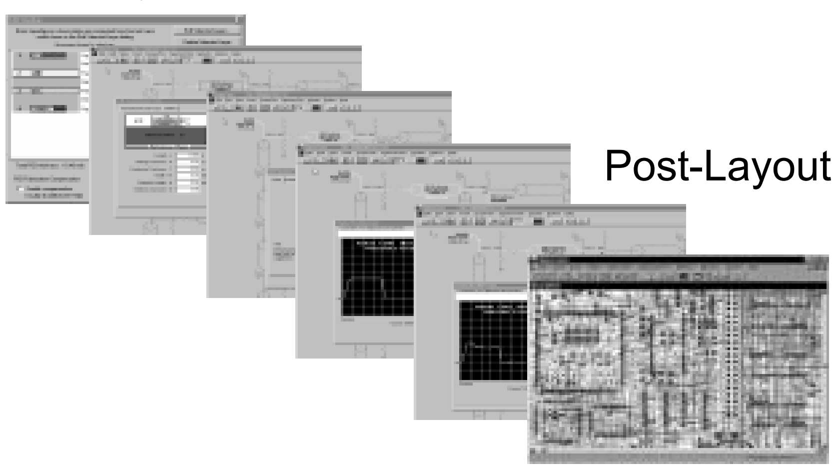
PCB Design Flow



Two Types of Simulation

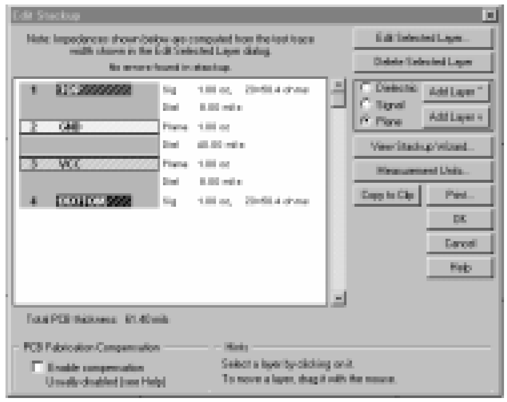
Pre-Layout

Post-Layout



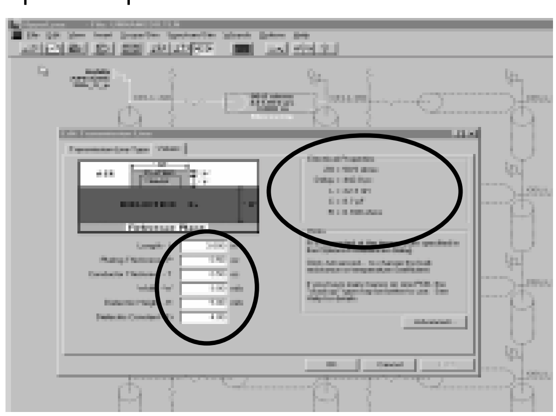
Pre-Layout Simulation

- Examine Stackup of 4-Layer Board
- Tool Calculates Impedance



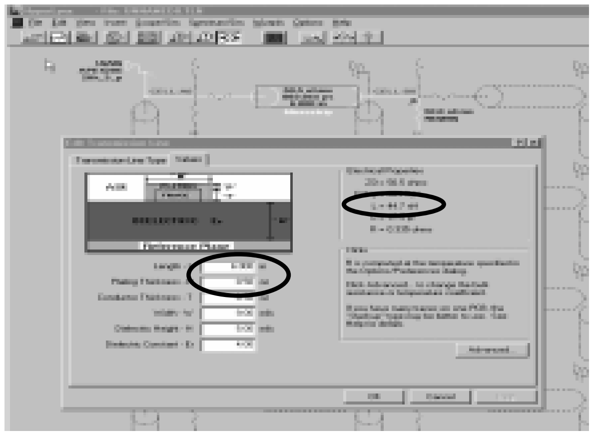
Pre-Layout Simulation

- Determine Delay, L, C & R Values from Stackup
- Find New Electrical Parameters after Changing Dimensions
  - Microstrip vs. Stripline



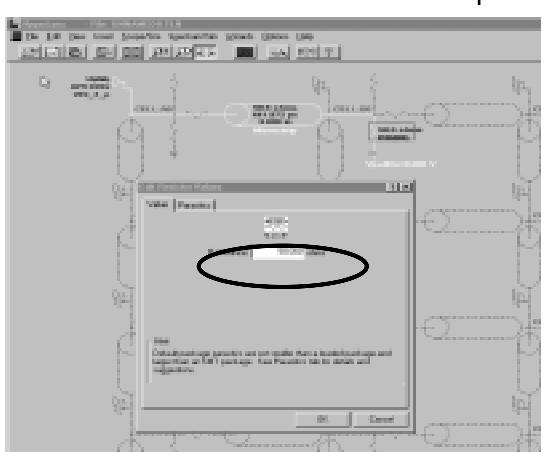
Pre-Layout Simulation

- New Length, Tool Reports New Electrical Properties



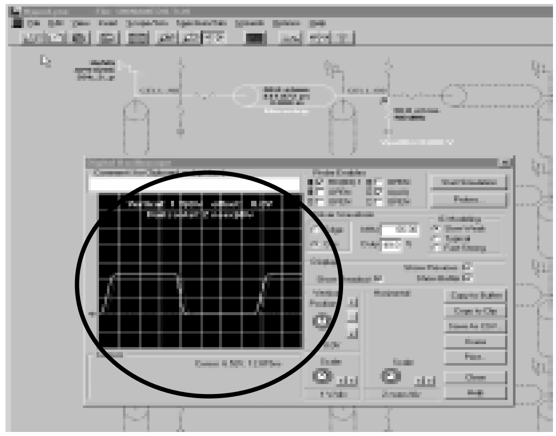
Pre-Layout Simulation

- Set 50-Ω Termination Resistor for 50-Ω Impedance Board



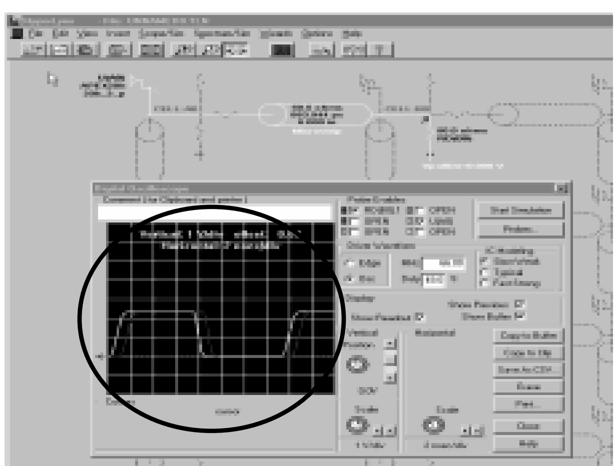
Pre-Layout Simulation

- Examine Simulation Waveform Output
- Blue & Red Traces Show Different Probe Points



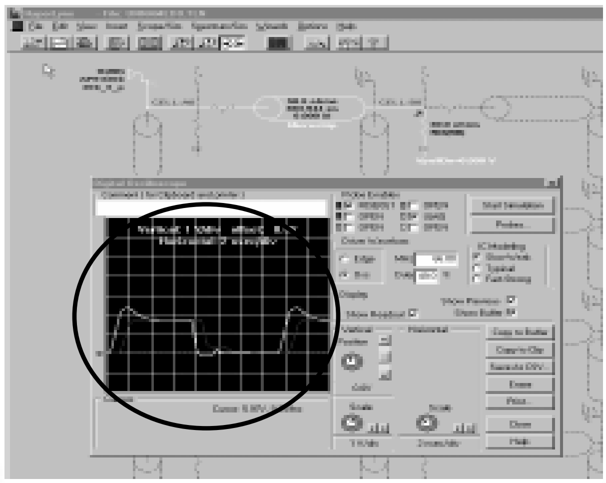
Pre-Layout Simulation

- Different Line Length Causes Different Delay



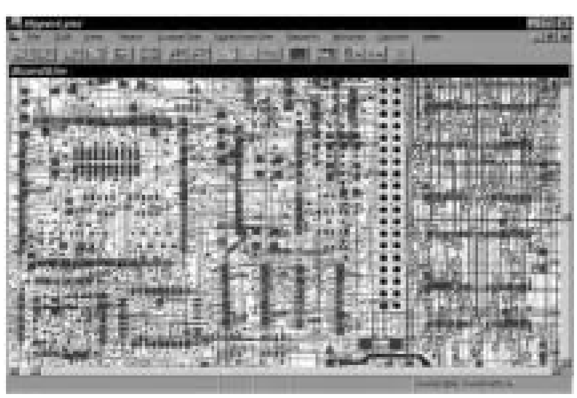
Pre-Layout Simulation

- 30-Ω Termination Resistor Causes Signal Integrity Issues



Post-Layout Simulation

- Pull Board Layout into Simulation Tool
- Can Simulate Based on Exact Layout



Altera Simulation Tools

- Altera Provides IBIS Models on www.altera.com
- Encrypted Spice Models Available by Request

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- *H. Johnson & M. Graham, High Speed Board Design, Prentice Hall, Inc., 1993*
- *Stephen Hall, Garrett Hall, & James McCall, High-Speed Digital System Design, John Wiley & Sons, Inc., 2000*
- *William J. Dally & John W. Poulton, Digital Systems Engineering, Cambridge University Press, 1998*
- *Altera Application Note 224: High-Speed Board Layout Guidelines*

Summary

- Keys to Success with High-Speed Board Design
  - Understanding Basic Theory
  - Considering Signaling Issues During Design
  - Maintaining Good Communication with Layout Engineer
  - Using Published Guidelines
  - Simulating Design before & after Layout
  - Using Device Features to Ensure High Signal Quality