



# Altera Solution Brief

## DO-254 Compliance Tool Set

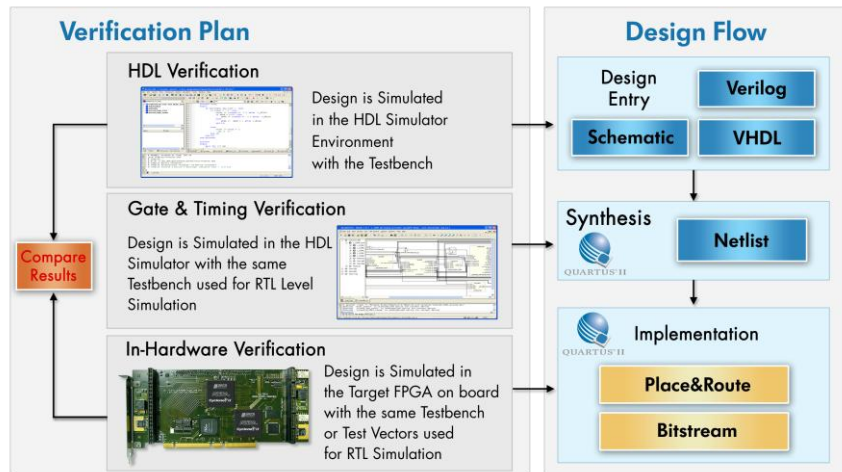
### Overview

The Aldec DO-254 Compliance Tool Set (CTS) provides support for the “Design Assurance Guidance for Airborne Electronic Hardware” (DO-254/ED80) Chapter 6.2 “Verification Process” and Chapter 11.4 “Tool Assessment and Qualification Process”. The Aldec DO-254 Compliance Tool Set (CTS) supports a fast and reliable verification process for assurance levels A-D with a focus on increased coverage, testability, and visibility in the Altera device together with design requirements traceability.

### The Challenge

Verifying FPGA and PLD designs in hardware, while tracing the output results back to the original design requirements, is a significant challenge with today’s DO-254 verification solutions. With HDL simulation, it is possible to comprehensively simulate the entire design with an exhaustive testbench. With in-hardware testing however, it is difficult to achieve a similar level of verification. Typically, traditional hardware testing methods with a logic analyzer allow for examining only a small portion of the design logic in the target Altera device

on the system board. Checking corner-stone cases can be challenging because they require manipulating the real I/O data from the target device. Usually only a small percentage of the Altera device I/O pins are accessible on the final system board, limiting the testability of the device. But with the Aldec DO-254 CTS, all of the I/O pins are available, allowing the whole design to be verified in the target device. Traditional in-hardware testing, with all of its limitations, is not adequate to fulfill the verification process of the DO-254 specification for Level A and B compliance; these levels require catastrophic failure analysis of the design in the target Altera device.



### Aldec DO-254 CTS Solution

The Aldec DO-254 CTS consists of a world-class HDL Simulation tool suite combined with an In-Hardware Simulation system that supports the customer’s specific Altera FPGA or PLD target device. In the verification flow, testing requirements are checked first in the HDL simulator and later in the target hardware. With Aldec’s solution, the HDL testbench achieving 100% functional coverage can be reused for in-hardware testing of the target device at-speed. The golden set of waveform vectors validated in the HDL simulation are compared with the set of waveform vectors generated in the target device. If any mismatches are found, they can be easily investigated using the graphical waveform viewer. In-hardware testing provides assurance that the design works in the target Altera device just as it did during HDL simulation, with traceability of the hardware outputs back to the design requirements. In addition, in-hardware testing independently assesses the outputs of the Quartus synthesis and place-and-route design software and the HDL simulation tool, fulfilling the DO-254 requirements for tool assessment of these tools. The Aldec DO-254 CTS allows customers to manage their verification and tool assessment challenges with a powerful, easy-to-use solution.