AN 447: Interfacing Cyclone III and Cyclone IV Devices with 3.3/3.0/2.5-V LVTTL/LVCMOS I/O Systems

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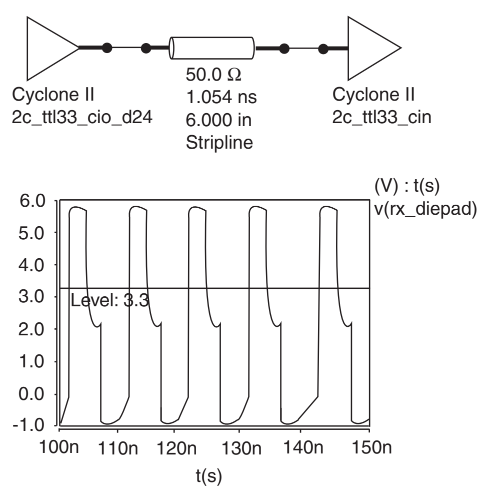
Altera® Cyclone® III and Cyclone IV devices are compatible with and support 3.3/3.0/2.5-V LVTTL/LVCMOS I/O standards. This application note provides background information for LVTTL/LVCMOS I/O standard signal integrity issues and describes guidelines for interfacing 3.3/3.0/2.5-VLVTTL/LVCMOS I/O standards in Cyclone III and Cyclone IV devices.

Background

Cyclone III and Cyclone IV devices are designed to 1.2-V to 3.3-V interface voltage levels to accommodate requirements for flexible I/O interface implementation. Proper design consideration must be observed when the device is driven by a 2.5-V (or higher) system. This condition is attributed to transmission line effects, in which large voltage deviation can happen at the receiving end and potentially damage the input buffer. I/O standards that do not require any termination, such as LVTTL or LVCMOS, are at risk.

The example in Figure 1 uses Cyclone II devices with a 3.3-V LVTTL interface at the highest drive current setting and no termination. The simulation shows that an excessively large overshoot is present at the receiver when driven from a high current driver via an unterminated transmission line.

Figure 1. Cyclone II Device 3.3-V LVTTL Output Interfacing with Cyclone II Device 3.3-V LVTTL Input and Simulation Waveform



The requirements on the absolute maximum DC input voltage and maximum allowed overshoot/undershoot voltage for Cyclone III and Cyclone IV devices might not be met if the signal integrity issues are not properly addressed when using Cyclone III and Cyclone IV devices in interfacing with 3.3/3.0/2.5-V LVTTL/LVCMOS systems.

☞ You must design the I/O interfaces within the specifications recommended in "Design Guideline" to ensure device reliability and proper operation,

For the values of the absolute maximum DC input voltage and maximum allowed overshoot/undershoot voltage, refer to the *Cyclone III Device Data Sheet* and *Cyclone III LS Device Data Sheet* chapters in volume 2 of the *Cyclone III Device Handbook* andthe *Cyclone IV Device Data Sheet* chapter in volume 3 of the *Cyclone IV Device Handbook*.

Design Guideline

This section describes when and how to address the maximum DC and AC input voltage requirements of Cyclone III and Cyclone IV devices for a successful interface design.

Cyclone III and Cyclone IV devices support only one V_{CCIO} voltage level per I/O bank. Additional driver input voltage levels other than bank V_{CCIO} voltage are allowed for input signaling. Not all combinations require attention to the maximum input voltage.

Table 1 identifies the I/O standard voltage interface combinations that require attention and the recommended actions.

Table 1. Cyclone III and Cyclone IV Devices 3.3/3.0/2.5-V LVTTL/LVCMOS Receiver Level Requirements

Cyclone III and Cyclone IV Devices Receiver Bank V_{CCIO} *(1)*, *(2)*	**Driver Voltage Level**		
	2.5-V LVTTL/LVCMOS	**3.0-V LVTTL/LVCMOS**	**3.3-V LVTTL/LVCMOS**
2.5 V	No action required	Disable diode and apply series termination *or* use driver selection table *(3)*	Disable diode and apply series termination *or* use driver selection table *(3)*
3.0 V	No action required	No action required	No action required
3.3 V	Apply series termination or use driver selection table *(4)*	Apply series termination or use driver selection table *(4)*	Apply series termination or use driver selection table *(4)*

Notes to Table 1:

(1) This applies when the Cyclone III and Cyclone IV device I/O pin is assigned as input, bidirectional, or tristated output using the 3.3/3.0/2.5-V LVTTL/LVCMOS I/O standards. The Quartus II® software enables the PCI-clamp diode on this pin for each of these conditions by default. No attention is required when the Cyclone III and Cyclone IV device I/O pin is only used as output.

(2) Other I/O standards do not require attention on the maximum input voltage, such as 1.8/1.5/1.2-V LVTTL/LVCMOS, 3.0-V PCI/PCI-X, voltage-referenced, and differential I/O standards.

(3) The Cyclone III and Cyclone IV device I/O pin is over-driven by a higher external voltage. You must ensure that the DC current specification of the diode is met. For more information, refer to "PCI-Clamp Diode" on page 3. Alternatively, you can apply series termination to manage voltage overshoot. In such cases, Altera recommends that you disable the diode due to the possible presence of a high DC current.

(4) Diode clamped voltage can still exceed the maximum DC and AC specifications due to the high V_{CCIO} voltage level of the bank in which the I/O resides. You must manage the voltage overshoot. You can leave the diode enabled without concern for the DC current as the I/O pin is not over-driven.

You must perform the following tasks to manage voltage overshoot and input requirements as listed in Table 1:

- Use the internal PCI-clamp diode on the pin (this is enabled by default in the Quartus II software).
- Apply series termination.
- Select the appropriate driver to interface with Cyclone III and Cyclone IV devices and take advantage of the available slew rate control of the driver output.

☞ For details about each of these methods, refer to "PCI-Clamp Diode", "Termination", and "Driver Selection" on page 4. Additional details and background information are also available in the related appendices.

PCI-Clamp Diode

Cyclone III and Cyclone IV devices provide an optional PCI-clamp diode for each I/O pin. You can use this diode to protect I/O pins against voltage overshoot. The Quartus II software enables the PCI-clamp diode on the assigned input, bidirectional, or tristated output pins by default using the 3.3/3.0/2.5-V LVTTL/LVCMOS I/O standards. The diode can sufficiently clamp voltage overshoot to within the DC and AC input voltage specifications when the bank supply voltage (V_{CCIO}) is 2.5 V or 3.0 V. You can clamp the voltage for a 3.3-V V_{CCIO} to a level exceeding the DC and AC input voltage specifications with ± 5% supply voltage tolerance. The clamped voltage is expressed as the sum of the supply voltage (V_{CCIO}) and the diode forward voltage.

☞ Dual-purpose configuration pins support the diode in user mode if the specific pins are not used as configuration pins for the selected configuration scheme. Dedicated configuration pins do not support the on-chip diode.

The PCI-clamp diode in Cyclone III and Cyclone IV devices can support a maximum of 10-mA DC current. The diode sinks the DC current when driven by a voltage level that exceeds the bank V_{CCIO} plus the diode forward voltage. You must take the DC sink into consideration current when interfacing a 2.5-V V_{CCIO} Cyclone III or Cyclone IV device receiver with 3.0-V and 3.3-V LVTTL/LVCMOS I/O systems. "Appendix A: DC Current Measurement with PCI-Clamp Diode" on page 6 describes the method to measure DC current with simulation.

☞ 10-mA DC current limit refers to the current that the diode sinks and not the drive strength of the driver. This limit is only applicable when the PCI-clamp diode is enabled and when the 2.5-V Cyclone III and Cyclone IV device receiver interfaces with 3.0-V or 3.3-V LVTTL/LVCMOS I/O systems.

Ensure that the interface meets the DC and AC specifications when disabling the diode in the Quartus II software. You can also use the guideline discussed in "Driver Selection" on page 4 to select the appropriate driver with the specific characteristic that meets Cyclone III and Cyclone IV devices specifications without employing termination if your system has the flexibility to accommodate a selection of driver strengths. For more information on how to disable the PCI-clamp diode, refer to the *Assignment Editor* chapter in volume 2 of the *Quartus II Handbook.*

Termination

Transmission line effects that cause large voltage deviation at the receiver are associated with impedance mismatch between the driver and transmission line. You can significantly reduce voltage overshoot by matching the impedance of the driver to the characteristic impedance of the transmission line. You can use a series termination resistor placed physically close to the driver to match the total driver impedance to transmission line impedance.

Equation 1 describes the above condition and is used as a rule of thumb to match the transmission line impedance, Z_0:

Equation 1. Matching the Transmission Line Impedance *(Note 1)*

$$R_{driver} + R_{series} \approx Z_0$$

Note to Equation 1:

(1) R_{driver} represents the intrinsic impedance of the driver and R_{series} represents the resistance of the external series resistor.

Determine the appropriate series termination value using Equation 1 if the driver device manufacturer specifies the driver buffer output impedance. Simulate an IBIS model for the driver to determine the appropriate series termination resistor value for the interface if the output impedance value of the driver is not available.

"Appendix B: Series Termination" on page 8 shows a simulation example to manage overshoot by determining a suitable termination resistor value. This method, when appropriately applied, ensures the signal integrity of the interface and eliminates Cyclone III and Cyclone IV device receiver voltage overshoot concerns when appropriately applied.

Some drivers offer series on-chip termination (OCT) to minimize impedance mismatch to the transmission line. You can choose a driver with R_{driver} that closely matches the transmission line impedance in such cases. This provides sufficient impedance matching without the expense of additional external component.

☞ OCT affects the edge rates of the transmitted signal. You must evaluate if the timing impact causes a performance degradation of the interface.

Driver Selection

Another alternative in addressing signal integrity concerns in your interface is to select the appropriate driver. The output characteristics of a driver determines how much overshoot voltage is seen at the receiver when the interface is not terminated.

Table 3 on page 11 in "Appendix C: Driver Selection Table and Measurement Method" describes the requirements for a driver to successfully interface with Cyclone III and Cyclone IV devices without termination. You must select a driver that meets the current limits listed in Table 3 at the appropriate points in the I/V curve. The I/V curve of the driver is obtained from the IBIS file provided by the device manufacturer. The current limit from Table 3 takes the DC and AC requirements of the receiver and the use of the PCI-clamp diode into account. It allows you to select the appropriate driver without further analysis.

You can also use slew rate control to address signal integrity concerns, if it is available on the driver. Slew rate control allows you to reduce the edge rate of the output signal to help control voltage overshoot at the receiver. You must perform simulations to ensure that the specifications are met when using the slew rate feature.

Conclusion

Cyclone III and Cyclone IV devices are compatible with and support the 3.3/3.0/2.5-V LVTTL/LVCMOS interfaces. You can ensure device reliability and proper interface operation in the system by following the recommendations found in "Design Guideline" on page 2 to manage signal integrity issues and protect the pin. The DC and AC input voltage specifications must be met when designing interfaces with Cyclone III and Cyclone IV devices.

Appendix A: DC Current Measurement with PCI-Clamp Diode

The PCI-clamp diode is forward-biased when the driver voltage level exceeds the V_{CCIO} plus diode forward voltage. DC current exists when the diode is forward-biased. The amount of DC current depends on the driver output impedance, driver and receiver supply voltage, diode forward voltage, and a small resistance intrinsic to the transmission line.

Figure 2 shows the PCI-clamp diode for Cyclone III and Cyclone IV devices.

Figure 2. Cyclone III and Cyclone IV Device PCI-Clamp Diode

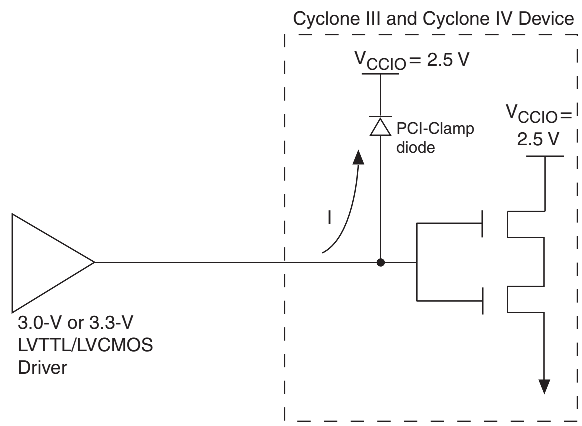
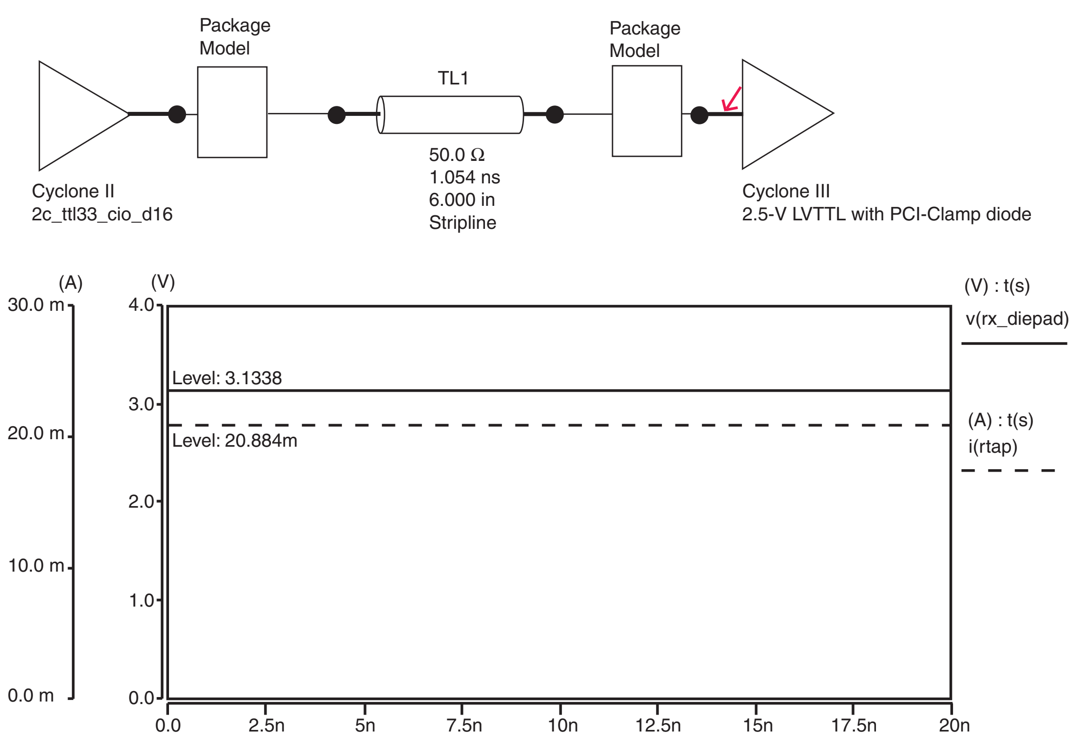


Figure 3 shows the setup to measure the DC current that flows into the PCI-clamp diode.

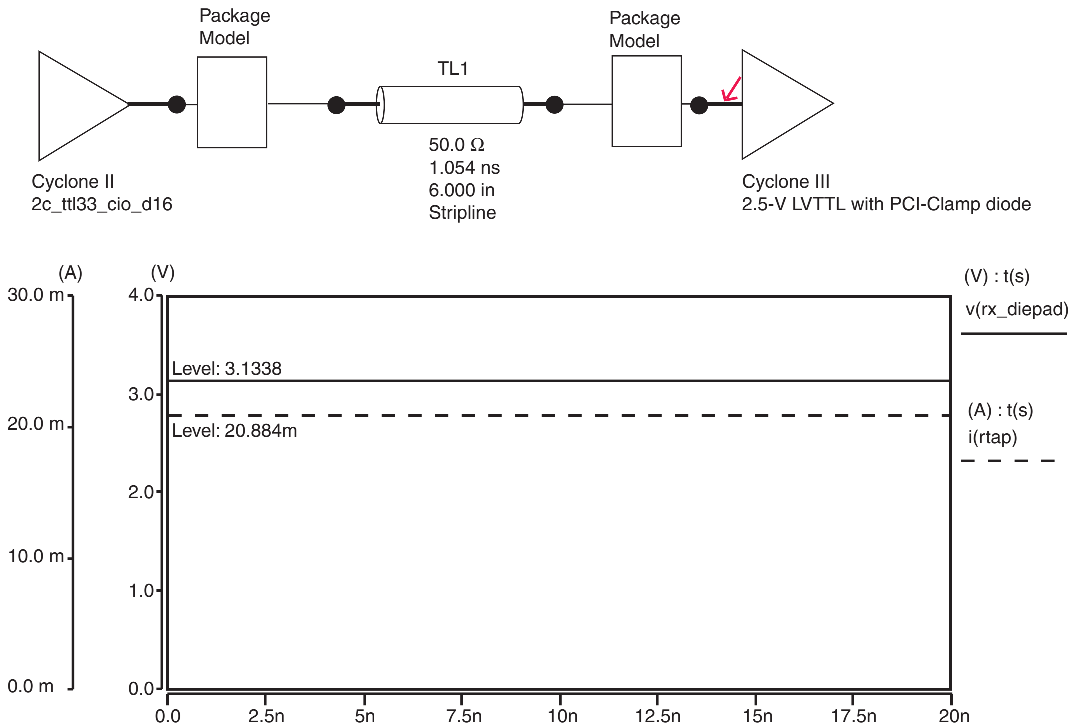
Figure 3. Simulation Setup and Result to Determine DC Current that Flows into the PCI-Clamp Diode



Set up the driver to drive static logic-high signal into the Cyclone III receiver with the PCI-clamp diode enabled. Apply the maximum supply voltage at the driver and the minimum V_{CCIO} at the Cyclone III receiver for the highest DC current. Take the current measurement from the Cyclone III device die pad denoted by the **red** pointer in Figure 3. You can obtain current measurements using a small sense resistor (in mili-Ω) placed in series to the transmission line.

A 20.88-mA DC current sink into PCI-clamp diode is measured as shown in Figure 4. The result significantly exceeds the 10-mA maximum current supported by the diode. For guidelines to interface 3.3/3.0/2.5-V LVTTL/LVCMOS I/O standards with Cyclone III and Cyclone IV devices, refer to Table 1 on page 2.

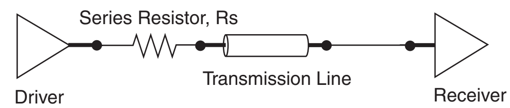
Figure 4. Simulation Setup Result



Appendix B: Series Termination

The series termination scheme works by introducing a resistor placed in series between the driver and receiver as shown in Figure 5. The driver impedance and series resistance become the total effective driver impedance. The transmission line impedance has to match the driver impedance to minimize reflection and manage overshoot.

Figure 5. Series Termination Scheme

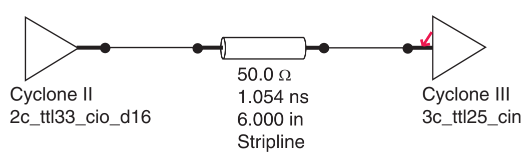


It is important to choose an appropriate resistor value for series termination. The termination might not effectively reduce or eliminate the overshoot if the resistance is too small. The driver might not sufficiently drive the transmission line and results in a stair-step response if the resistance is larger. You must perform a simulation to determine the suitable series resistor value for your interface within the allowable tolerance condition.

The following example shows how to determine the value of the series termination resistor to manage the voltage overshoot effectively. This example uses the terminator wizard feature in the HyperLynx Simulation Software by Mentor Graphics® Corporation. You can explore other appropriate methods via simulation to determine a suitable series resistor value for your interface.

Consider driving a Cyclone II 3.3-V LVTTL 16 mA to a Cyclone III 2.5-V LVTTL input. You can either disable the diode and apply the series termination or use the driver selection table as listed in Table 1 on page 2. Evaluate the series termination solution for this example. Set up the desired interface in the Schematic Editor as represented in Figure 6 and execute the terminator wizard.

Figure 6. Cyclone II 3.3-V LVTTL 16 mA Interfacing with Cyclone III 2.5-V LVTTL



The suggested 33-Ω series resistance is applied close to the Cyclone II driver (as shown in Figure 8) based on the terminator wizard results shown in Figure 7. The new setup is evaluated at different allowable conditions to ensure that DC and AC specifications are met and to identify the impact of introducing the resistor in the interface. Simulation results are shown in Figure 9.

Figure 7. Terminator Wizard Results From HyperLynx Simulation Software by Mentor Graphics Corporation

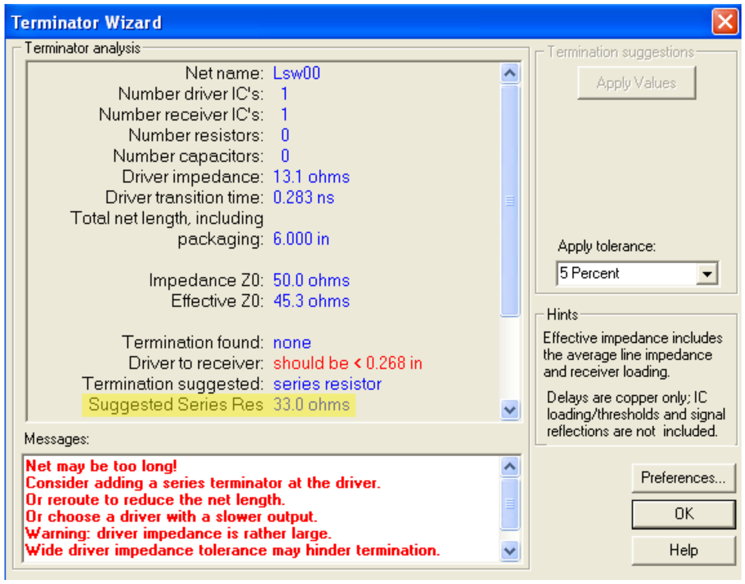


Figure 8. Cyclone II 3.3-V LVTTL 16 mA interfacing with Cyclone III 2.5-V LVTTL with Recommended 33.0-Ω Series Termination Resistor

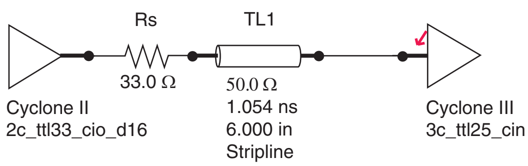
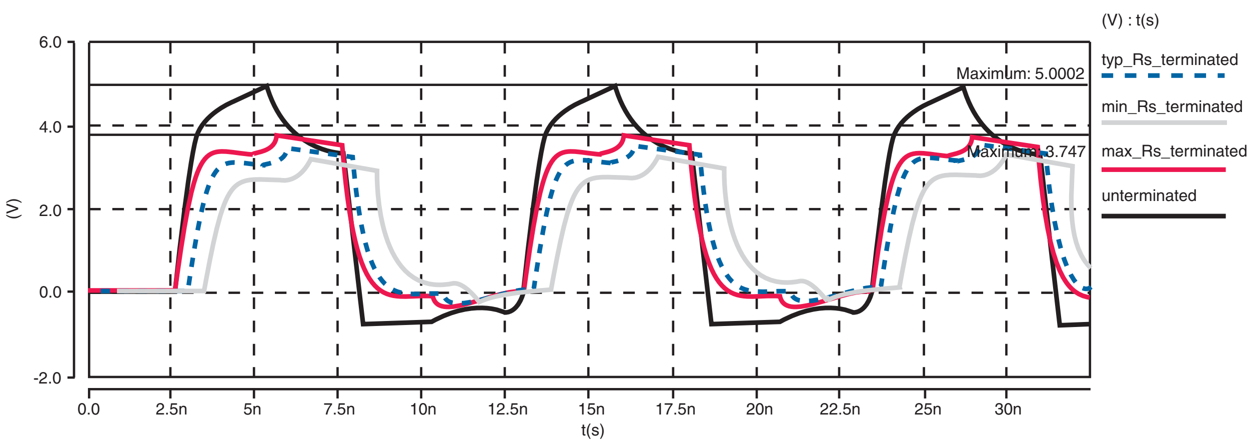


Figure 9. Simulation Waveform of 2c_ttl33_cio d16 Driving 3c_ttl25_cin Without Versus with Recommended Series Termination Across Typical, Minimum, and Maximum Conditions



Appendix C: Driver Selection Table and Measurement Method

A driver can drive a receiver without termination even if it produces overshoot, undershoot, and ringing in the interface as long as two key specifications are met:

- Voltage threshold
- Maximum input voltage of the receiver device

Conformance to the voltage threshold specification ensures the correct logic-low and logic-high switching. On the other hand, conformance to the maximum DC and AC input specifications ensures the reliability of the receiver device in the system over an extended period.

Current limits in Table 3 are used as a measurement to identify if a driver meets the Cyclone III and Cyclone IV device input specifications for the target I/O standard without requiring simulation. The current limits are the maximum allowable driver current values at the V_{OH} level defined in Table 2. An easy and convenient method to determine this is to perform this measurement on the driver pull-up I/V curve in the IBIS model. The pull-up I/V curve represents the current and voltage behavior of the driver when it is sourcing logic-high. Take the measurement at the driver maximum allowable operating condition, which is at a low temperature and high supply voltage, to account for the worst possible overshoot condition. The current limits do not represent the current strength of the driver. You must perform the measurement on the I/V curve at the maximum condition.

A driver can drive to a Cyclone III or Cyclone IV device without requiring termination if the measured current of the driver is less than the current limit in Table 3 for the desired interface setup. The limits ensure that the DC and AC maximum input voltage specifications and maximum DC current for diode are met, if the driver current value is within the limits.

Table 2. V_{OH} Level for Each I/O Standard

Driver I/O Standard	V_{OH} level
2.5-V LVTTL	2.0 V
3.0-V LVTTL	2.4 V
3.0-V LVCMOS	V_{CCIO} – 0.2 V
3.3-V LVTTL	2.4 V
3.3-V LVCMOS	V_{CCIO} – 0.2 V

Table 3 lists the maximum current limits of the drivers that interface with Cyclone III and Cyclone IV devices without termination in each I/O interface combination.

Table 3. Maximum Allowed Current Metrics Required to Drive Cyclone III and Cyclone IV Devices without Termination

Cyclone III and Cyclone IV Device Receiver Bank V_{CCIO} (V) *(1)*	Driver Voltage Level *(3)*				
	2.5-V LVTTL	**3.0-V LVTTL**	**3.0-V LVCMOS**	**3.3-V LVTTL**	**3.3-V LVCMOS**
2.5 +/- 5%	No maximum limit	26 mA	8 mA	15 mA (30 mA) *(2)*	4 mA (8 mA) *(2)*
3.0 +/- 5%	No maximum limit	No maximum limit	No maximum limit	No maximum limit	No maximum limit
3.3 +/- 5%	48 mA	26 mA	8 mA	30 mA	12 mA

Notes to Table 3:

(1) By default, the Quartus II software enables the PCI-clamp diode on any Cyclone III and Cyclone IV device I/O pin assigned as an input, or as bidirectional or tristated output for the 3.3/3.0/2.5-V LVTTL/LVCMOS I/O standards.

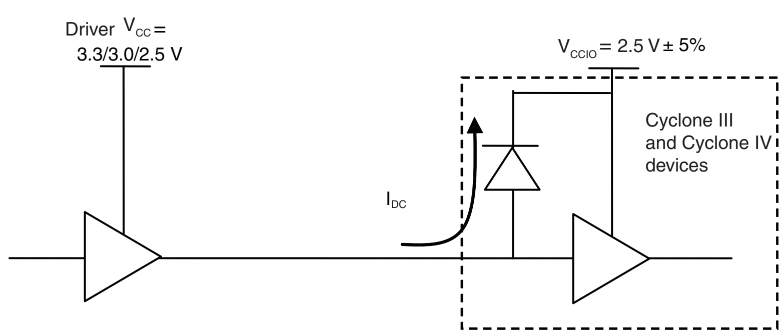
(2) The bracketed value represents the current limit for the driver when the PCI-clamp diode is manually disabled. This is only applicable for this interface combination, whereby disabling the diode offers slightly more margin for the driver. For other interface combinations, the diode has better margin for the driver when enabled.

(3) The current limit does not represent the current strength of a driver associated with a particular I/O standard. For more information on the current limits, refer to “Appendix C: Driver Selection Table and Measurement Method” on page 10.

There is a limitation on the I/V characteristic of the driver interfacing with Cyclone III and Cyclone IV device inputs powered by 2.5-V or 3.3-V voltage level without external termination.

Figure 10 shows the interfacing conditions with 2.5-V V_{CCIO} for Cyclone III and Cyclone IV devices.

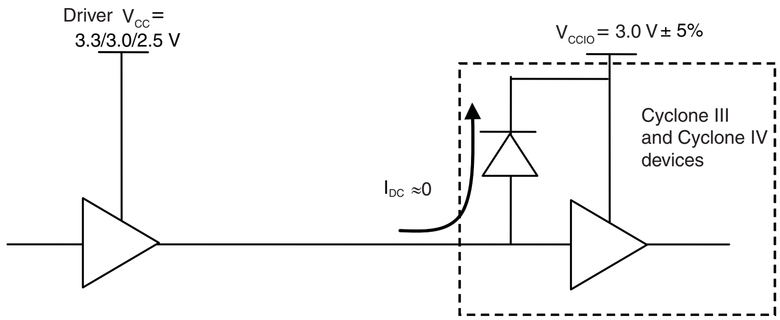
Figure 10. Cyclone III and Cyclone IV Device Input Setup with 2.5-V V_{CCIO}



The Cyclone III and Cyclone IV device on-chip PCI diode starts to sink the DC current I_{DC} when driven by a steady state voltage greater than the sum of the Cyclone III and Cyclone IV device V_{CCIO} and diode forward voltage as shown in Figure 10. The diode is forward-biased when the driver V_{CC} is 3.3 or 3.0 V and the I_{DC} must not exceed 10 mA. The amount of I_{DC} through the diode is determined by the potential voltage difference between the driver and the Cyclone III or Cyclone IV device pin and the current capability of the driver. The diode can limit the transient voltage level to below the specification limit when the driver V_{CC} is 2.5 V (effectively to 3.325 V, assuming V_{CCIO} is 2.625 V and diode forward voltage is 0.7 V).

Figure 11 shows the interfacing conditions with 3.0-V V_{CCIO} for Cyclone III and Cyclone IV devices.

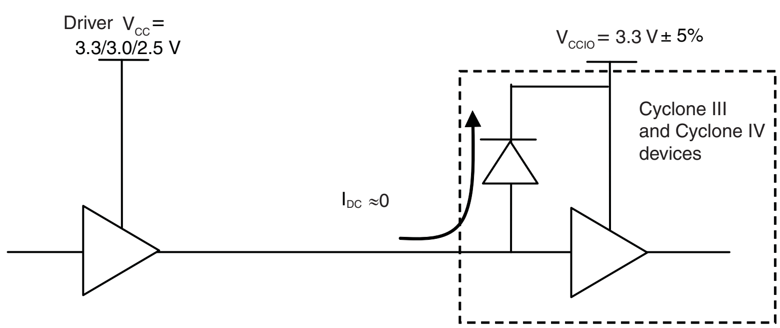
Figure 11. Cyclone III and Cyclone IV Device Input Setup with 3.0-V V_{CCIO}



The diode might not be forward-biased even when the driver V_{CC} is 3.3 V as the potential voltage difference between the driver V_{CC} and the Cyclone III or Cyclone IV device V_{CCIO} is less than the diode forward voltage. Therefore, there is no concern on I_{DC} through the diode when driven with an input voltage level of 3.3 V, 3.0 V, or 2.5 V as shown in Figure 11. The forward-bias of the diode occurs only momentarily during overshoot conditions to clamp the overshoot voltage level. In such cases, the diode is effective in limiting the transient voltage level to below the specification limit (effectively to 3.85 V, assuming V_{CCIO} is 3.15 V and diode forward voltage is 0.7 V).

Figure 12 shows the interfacing conditions with 3.3-V V_{CCIO} for Cyclone III and Cyclone IV devices.

Figure 12. Cyclone III and Cyclone IV Device Input Setup with 3.3-V V_{CCIO}



I_{DC} is almost zero at a steady input voltage level as the diode might not be forward-biased as shown in the setup in Figure 12. At a higher driver V_{CC} level such as 3.465 V, the diode clamps transient voltage level at 4.165 V (assuming diode forward voltage is 0.7 V). The percentage of high time for an overshoot of 4.15 V can be as high as 18.52% over a 10-year period. You must ensure that the duration of the overshoot is below the specified limit. The use of a lower driver current capability reduces the voltage overshoot level. These examples use the driver selection method in Table 3 on page 11 to evaluate an interface from a Cyclone series device to the Cyclone III and Cyclone IV device receiver using the 3.3-V LVTTL I/O standard via the transmission line that was not terminated. The current strength of 8 mA for the Cyclone device is chosen for this interface evaluation. Perform the following steps to perform the evaluation:

1. Obtain the IBIS model for the driver.

   The model used as the driver is `1c_ttl33_io_d8` from the **cyclone.ibs** file. You can perform a DC sweep simulation the HSPICE model and set the buffer to drive logic-high if the IBIS model is not available for the driver.

   IBIS models for all Altera devices are obtained from Altera IBIS Models page on the Altera website.

2. Open the IBIS file using the HyperLynx Visual IBIS Editor.

   The editor provides a graphical view of IBIS model data, which provides a measurement of the I/V values in graphical format.

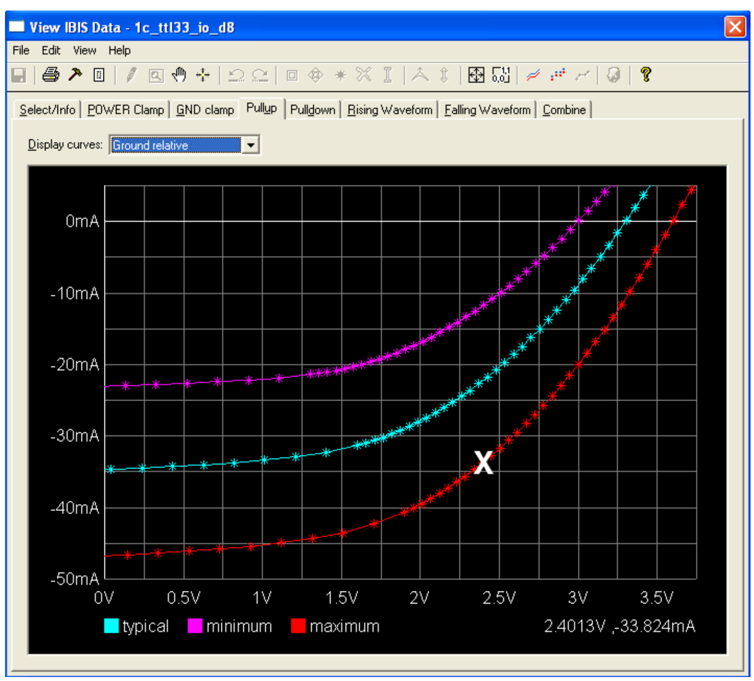
3. Run the graphical view mode.

   Navigate to the `1c_ttl33_io_d8` model data from tree-view pane on the left column in the editor. Right-click on the model denoted by `[Model] 1c_ttl33_io_d8` and select **View Data**. A dialog box appears with multiple tabs for each data characteristic available for the model.

4. Select the pull-up I/V curve.

   Select the **Pullup** tab in the dialog window. In the **Display Curves** list, select **Ground relative** as shown in Figure 13.

Figure 13. Current Limit Measurement for IBIS Pull-Up Data Using Graphical Viewer HyperLynx Visual IBIS Editor



5. Identify the appropriate V_{OH} level and perform the current measurement.

   From Table 2 on page 10, the V_{OH} for the 3.3-V LVTTL driver is at 2.4 V. Look for the maximum I/V curve and make the visual approximation current measurement at 2.4 V. As shown in Figure 13, the measured current is 33.8 mA.

6. Identify allowed current limit.

   From Table 3 on page 11, the current limit is 30 mA for a 3.3-V LVTTL driver to a 3.3-V Cyclone III and Cyclone IV device receiver bank. The measured current exceeds the current limit from Table 3 on page 11. In conclusion, the Cyclone driver operating at 3.3-V LVTTL with 8 mA setting is not able to drive directly to a Cyclone III and Cyclone IV device input at 3.3-V V_{CCIO} supply without termination.

From the preceding example, a Cyclone device operating as the driver for the setup might not meet the DC and AC input voltage specification of Cyclone III and Cyclone IV devices. You can apply series termination to resolve the problem, as recommended in Table 1 on page 2.

Appendix D: Cyclone III or Cyclone IV Device to Another Cyclone III or Cyclone IV Device Interface Matrix

A Cyclone III or Cyclone IV device is able to drive into another Cyclone III or Cyclone IV device without termination for certain drive strengths using the 3.3/3.0/2.5-V LVTTL/LVCMOS I/O standards.

Table 4 lists the drive strength settings for a Cyclone III and Cyclone IV device driver that can drive into a Cyclone III or Cyclone IV device without termination and meets the maximum DC and AC input specifications.

Table 4. Interface Matrix from a Cyclone III or Cyclone IV Device to Another Cyclone III or Cyclone IV Device Without Additional Solution

Cyclone III and Cyclone IV Device Receiver Bank V_{CCIO} (V) *(2)*	Cyclone III and Cyclone IV Device Driver I/O Standard *(1)*														
	2.5-V LVTTL				3.0-V LVTTL				3.0-V LVCMOS				3.3-V LVTTL		3.3-V LVCMOS
	4 mA	8 mA	12 mA	16 mA	4 mA	8 mA	12 mA	16 mA	4 mA	8 mA	12 mA	16 mA	4 mA	8 mA	2 mA
2.5 +/- 5%	✓	✓	✓	✓	✓	✓	—	—	✓	—	—	—	✓	*(3)*	*(3)*
3.0 +/- 5%	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
3.3 +/- 5%	✓	✓	—	—	✓	✓	—	—	✓	—	—	—	✓	✓	✓

Notes to Table 4:

(1) A check indicates that the drive strength setting for the I/O standard can drive directly into a Cyclone III and Cyclone IV device receiver without terminating at the corresponding bank V_{CCIO} or violating the DC and AC input voltage specifications.

(2) The Quartus II software enables the PCI-clamp diode for pins assigned as 3.3/3.0/2.5-V LVTTL/LVCMOS I/O standards by default.

(3) Cyclone III and Cyclone IV devices with 3.3-V LVTTL with 8 mA setting or 3.3-V LVCMOS with 2 mA setting are unable to drive another Cyclone III or Cyclone IV device without termination at 2.5 V with the PCI-clamp diode enabled. However, both interfaces can work without violating the specifications by disabling the PCI-clamp diode at the 2.5-V Cyclone III and Cyclone IV device receiver pin.

Document Revision History

Table 5 lists the revision history for this application note.

Table 5. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
November 2009 v2.0	■ Updated all Cyclone IV device references. ■ Removed "Introduction" heading. ■ Removed "Referenced Documents" section.	—
June 2009 v1.2	■ Updated "Introduction" on page 1. ■ Updated "Background" on page 1. ■ Updated "Design Guideline" on page 2. ■ Updated Table 1 on page 2, Table 3 on page 10, Table 4 on page 14. ■ Updated "PCI-Clamp Diode" on page 3. ■ Updated "Termination" on page 4. ■ Updated "Conclusion" on page 5. ■ Updated "Appendix A: DC Current Measurement with PCI-Clamp Diode" on page 5, "Appendix C: Driver Selection Table and Measurement Method" on page 9, "Appendix D: Cyclone III Device Family to Cyclone III Device Family Interface Matrix" on page 14. ■ Updated Figure 2 on page 5, Figure 10 on page 10, Figure 11 on page 11, Figure 12 on page 12. ■ Updated "Referenced Documents" on page 14.	Updated to include Cyclone III LS devices information.
April 2008 v1.1	■ Added Figure 10, Figure 11, and Figure 12. ■ Added new note on configuration pins under PCI-Clamp Diode section. ■ Added new paragraph under Appendix C: Driver Selection Table and Measurement Method section.	—
March 2007 v1.0	Initial release.	—

101 Innovation Drive
San Jose, CA 95134
www.altera.com
Technical Support
www.altera.com/support