CF+ Interface Using MAX II CPLDs

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Introduction

This document details the implementation of a CompactFlash+ (CF+) interface using an Altera® MAX® II CPLD.

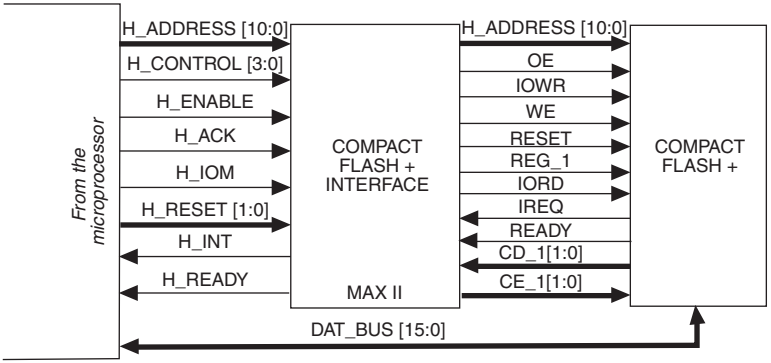
CompactFlash

CompactFlash cards are used to store and transport several forms of digital information (data, audio, pictures) and software between a wide span of digital systems. The CompactFlash association introduced the CF+ concept to enhance the operation of CompactFlash cards with I/O devices and magnetic disk data storage apart from flash memory. The CF+ card is a small form factor card that includes compact flash storage cards, magnetic disk cards, and various I/O cards that are available in the market, such as serial cards, ethernet cards, and wireless cards. The CF+ card includes an embedded controller that manages data storage, retrieval and error correction, power management, and clock control. CF+ cards can be used with passive adapters in PC-Card type-II or type-III sockets.

Nowadays, many consumer products such as cameras, PDAs, printers, and laptops have a socket that accepts CompactFlash and CF+ memory cards. In addition to storage devices, this socket can also be used to interface I/O devices that use the CF+ interface.

This design example uses a CF+ device, which functions in two modes: PC Card ATA using I/O mode and PC Card ATA using memory mode. The third optional mode, True IDE mode, is not considered. The MAX II CPLD operates as the host controller and acts as a bridge between the host and the CF+ card.

Figure 1. The Different Interfacing Signals of the CF+ Interface and the CF+ Device *Note (1)*



Note to Figure 1:
(1) A brief description of the interfacing signals is provided in Tables 1 and 2.

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The basic block diagram for implementing the CF+ interface is shown in Figure 1. The CF+ card interfacing signals are listed in Table 1. The signals that form the host interface are described in Table 2.

The CF+ card interface is enabled by the host by asserting the H_ENABLE signal. When the CompactFlash card is inserted in the socket, the two pins (CD_1 [1:0]) go low, indicating to the interface that the card has been inserted properly. In response to this action, an interrupt signal H_INT is generated by the interface, depending on the status of CD_1 pins and the chip enable signal (H_ENABLE).

Table 1. Description of CF+ Interface Signals (Part 1 of 2)

Signal	Direction	Description
HOST_ADDRESS [10:0]	Output	These address lines select the following: the I/O port address registers, the memory mapped port address registers, its configuration control and status registers.
CE_1 [1:0]	Output	This is a 2-bit active-low card select signal.
IORD	Output	This is an I/O read strobe generated by the host interface to gate the I/O data on the bus from the CF+ card.
IOWR	Output	This is an I/O write pulse strobe used to clock the I/O data on the card data bus on the CF+ card.
OE	Output	Active-low output enable strobe.

Table 1. Description of CF+ Interface Signals (Part 2 of 2)

Signal	Direction	Description
READY	Input	In memory mode, this signal is kept high when the CF+ card is ready to accept a new data transfer operation and low when the card is busy.
IREQ	Input	In the I/O mode operation, this signal is used as an interrupt request. It is strobed low.
REG_1	Output	This signal is used to distinguish between common memory and attribute memory accesses. High for common memory and low for attribute memory. In I/O mode, this signal should be active-low when the I/O address is on the bus.
WE	Output	Active-low signal for writing into the card configuration registers.
RESET	Output	This signal resets or initializes all registers in the CF+ card.
CD_1 [1:0]	Input	This is a 2-bit active-low card detect signal.

The H_READY signal is also asserted whenever the required conditions are met. This signal indicates to the processor that the interface is ready to accept the data from the processor. The 16-bit data bus to the CF+ card is connected directly to the host.

When the host receives an interrupt signal, it responds to it by generating an acknowledgment signal, H_ACK, for the interface to indicate that it has received the interrupt and is ready to perform further functions. This signal acts as an impetus; all operations of the interface, host, or the processor and CompactFlash card are synchronized to this signal. The interface also checks for H_RESET signal; this signal is generated by the host to indicate that all the initial conditions must be reset. The interface in turn generates the RESET signal to the CompactFlash card indicating to it to reset all its control signals to its default condition. The H_RESET signal can either be hardware or software generated. The software reset is indicated by the MSB of the Configuration Option Register within the CF+ card.

The host generates a 4-bit control signal H_CONTROL to indicate the desired function of the CF+ card to the CF+ interface. The interface decodes the H_CONTROL signal and issues various control signals to read and write data, and configuration information. Every card operation is synchronized to the H_ACK signal. At the positive edge of the H_ACK, the CPLD checks for the reset signal, and correspondingly issues the HOST_ADDRESS, chip enable (CE_1), output enable (OE), write enable (WE), REG_1, and RESET signals. Each of these signals have a predefined value for all the operations mentioned above. These are standard protocols, as defined by the CompactFlash association.

Table 2. Description of Host Interface Signals

Signal	Direction	Description
H_INT	Output	Active-low interrupt signal from interface to host indicating insertion of card.
H_READY	Output	Ready signal from interface to host indicating CF+ is ready to accept new data.
H_ENABLE	Input	Chip enable
H_ACK	Input	Acknowledgment to the interrupt request made by the interface.
H_CONTROL [3:0]	Input	A 4-bit signal selecting between I/O and memory READ/WRITE operations.
H_RESET [1:0]	Input	A 2-bit signal for hardware and software reset.
H_IOM	Input	Differentiates memory mode and I/O mode.

The H_IOM signal is held low in common memory mode and high in I/O mode. The common memory mode allows writing and reading of both 8-bit and 16-bit data. Also, the Configuration Registers in the CF+ card configuration option register, Card Status Register, and Pin Replacement Register are read from and written into. A 4-bit wide H_CONTROL [3:0] signal issued by the host differentiates between all these operations. The CF+ interface decodes H_CONTROL and issues the control signals to the CF+ card according to the CF+ specifications. Data is made available on the 16-bit data bus after the control signals are issued.

In the I/O mode, the software reset (generated by making the MSB of the Configuration Option Register in the CF+ card high) is checked. Byte and word access operations are executed by the interface in a manner similar to those in the memory mode detailed above.

Implementation

This design may be implemented using an EPM240 device. The design source code is compiled, and can be programmed into the MAX II CPLD. Map the host and CF+ interfacing ports, mentioned in Figure 1 on page 2, to suitable GPIOs. This design utilizes about 54% of the total LEs in an EPM240 device and uses 45 I/O pins.

Source Code

This design example has been implemented in Verilog. The source code, testbench, and complete Quartus II project are available at:

www.altera.com/literature/an/an492_design_example.zip

Conclusion

As illustrated through this design example, MAX II CPLDs are a great choice to implement interfaces to memory devices such as the CF+. Their low-cost, low-power, and easy power-on features make them the ideal programmable logic devices for memory device interfacing applications.

Additional Resources

- MAX II CPLD Homepage:
www.altera.com/products/devices/cpld/max2/mx2-index.jsp
- MAX II Device Literature:
www.altera.com/literature/lit-max2.jsp
- MAX II Power-Down Designs:
www.altera.com/support/examples/max/exm-power-down.html
- MAX II Application Notes:
  - *AN 422: Power Management in Portable Systems Using MAX II CPLDs*
  - *AN 428: MAX II CPLD Design Guidelines*

Document Revision History

Table 3 shows the revision history for this application note.

Table 3. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
December 2007 v1.0	Initial release.	—

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