

Introduction

MAX® II devices have an internal oscillator as part of the user flash memory (UFM). The internal oscillator can be used to meet the clocking requirements of many designs and eliminate the requirement for an external clock circuitry. This application note describes the instantiation of the internal oscillator and its usage.

Internal Oscillators

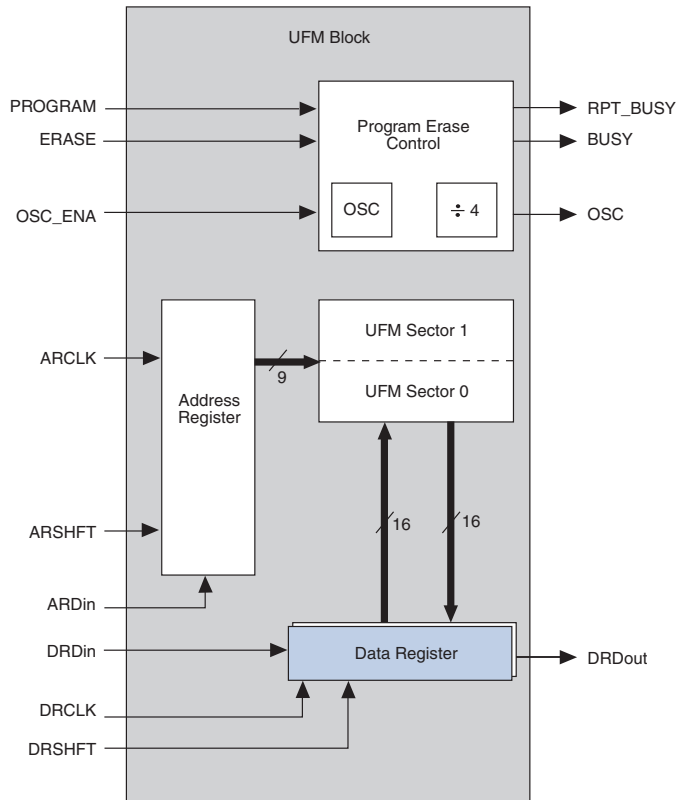
Most designs require a clock for normal operation. With an internal oscillator, MAX II devices do not require an external clocking circuitry. For example, the internal oscillator can be used to meet the clocking requirement of an LCD controller, SM bus controller, or any other interfacing protocol, or to implement a pulse width modulator. This helps minimize component count, board space, and thus reduces the total cost of the system.

The internal oscillator has the following features:

- The undivided internal oscillator works in the frequency range of 13.33 MHz to 22.22 MHz. The oscillator's output frequency, *OSC*, which is one-fourth of the undivided frequency, is in the range of 3.3 MHz to 5.5 MHz.
- The internal oscillator can be instantiated without instantiating the UFM. This is done by using the MAX II oscillator megafunction in the Quartus® II software.

Figure 1 shows the internal oscillator as part of the UFM.

Figure 1. Internal Oscillator as Part of the UFM Note (1)



Note to Figure 1:

- (1) The internal oscillator is part of the Program Erase Control block, which controls the programming and erasing of the UFM. The Data Register holds the data to be sent or retrieved from the UFM. The Address Register holds the address from which data is retrieved or the address to which the data is written.

Table 1 describes the signals used in the MAX II oscillator megafunction.

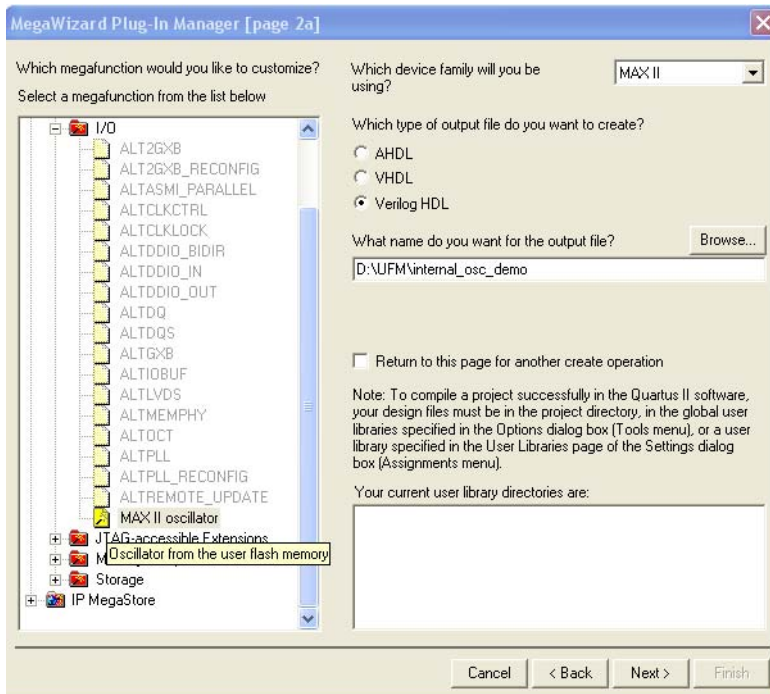
<i>Table 1. Pin Description</i>	
Signal	Description
OSC_ENA	Signal used to enable the internal oscillator.
OSC	Output of the internal oscillator. This signal is low when the oscillator is not enabled.

Using the Internal Oscillator in MAX II CPLDs

The internal oscillator has a single input, OSC_ENA, and a single output, OSC. An input pin, OSC_ENA, is used to activate the internal oscillator. When activated, a frequency of 3.3 MHz to 5.5 MHz is made available at the output. If the oscillator enabling signal, OSC_ENA, is driven low, the output of the oscillator is a constant low.

You can use the MAX II oscillator megafunction in the MegaWizard® Plug-In Manager to instantiate the oscillator, as explained in the following steps:

1. Open the project in which the internal oscillator is to be instantiated.
2. On the Tools menu, click **MegaWizard Plug-In Manager**.
3. On page 1 of the MegaWizard Plug-In Manager, select **Create a new custom megafunction variation** and then click **Next**.
4. On page 2a of the MegaWizard Plug-In Manager, select **MAX II** and the file output type (**Figure 2**).

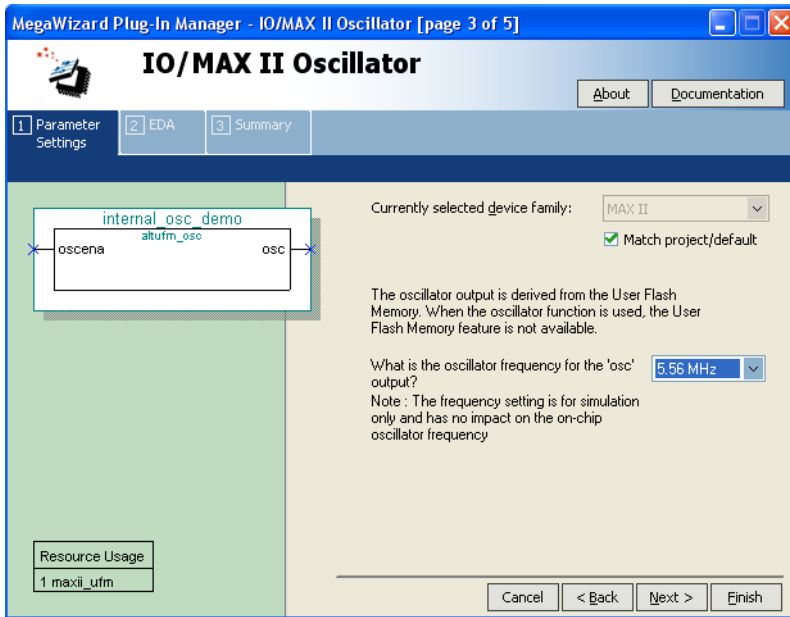
Figure 2. Selecting the `altufm_osc` Megafunction in the MegaWizard Plug-In Manager

- In the Megafunctions list, double-click **I/O** and then click **MAX II oscillator**. Type the output file name and then click **Next**. The oscillator output frequency can now be selected (Figure 3).



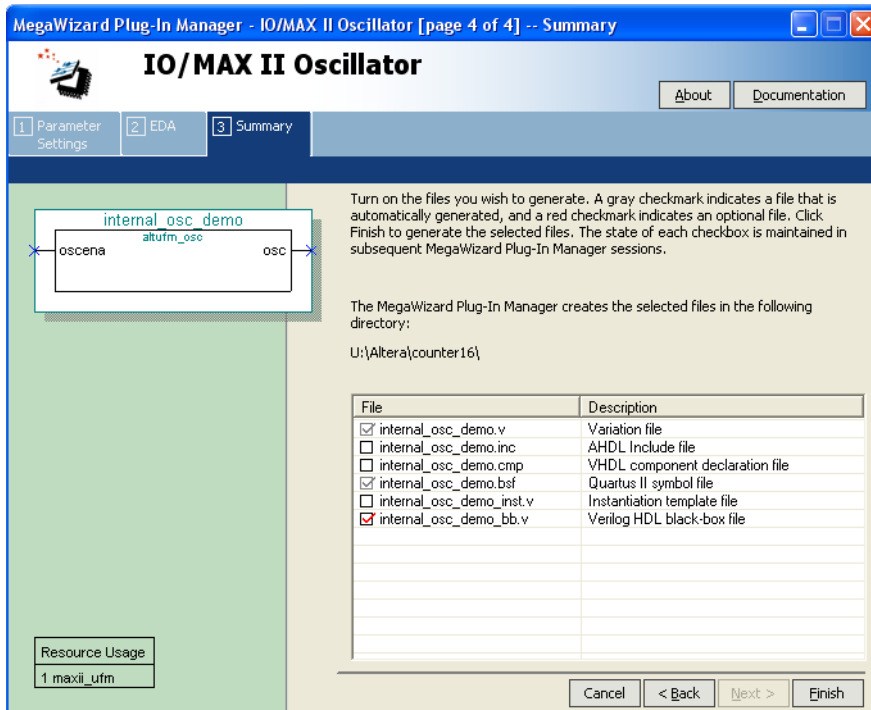
Note that this frequency setting is only for simulation and has no impact on the on-chip oscillator frequency. This is determined only by the CPLD, and is in the range of 3.3 MHz to 5.5 MHz.

Figure 3. Page 3 of the OSC Megafunction MegaWizard Plug-In Manager



6. In the **Simulation Libraries**, the model files that must be included are listed, as shown in [Figure 4](#). Click **Next**.

Figure 5. Summary Page of the OSC Megafunction MegaWizard Plug-In Manager



Implementation

This design example can be implemented with an EPM240G device or with any other MAX II CPLD, all of which have the internal oscillator feature. Implementation involves demonstration of the internal oscillator function by assigning the oscillator output to a counter and thereby driving GPIO pins on the MAX II CPLD. These are then made to drive the LEDs to create a scrolling effect, thereby demonstrating the internal oscillator.

The following details the implementation of this design example on the MDN-B2 demo board. Table 2 lists the EPM240G pin assignments for this design example.

EPM240G Pin Assignments			
Signal	Pin	Signal	Pin
d2	Pin 69	d3	Pin 40
d5	Pin 71	d6	Pin 75
d8	Pin 73	d10	Pin 73
d11	Pin 75	d12	Pin 71
d4_1	Pin 85	d4_2	Pin 69
d7_1	Pin 87	d7_2	Pin 88
d9_1	Pin 89	d9_2	Pin 90
sw9	Pin 82	—	—

Assign the unused pins **As input tri-stated** in the Quartus II software.

Design Notes

To demonstrate this design on the MDN-B2 demo board, perform the following steps:

1. Turn on the power to the demo board (using slide switch SW1).
2. Download the design onto the MAX II CPLD through the JTAG header JP5 on the demo board and a conventional programming cable (ByteBlaster™ II or USB-Blaster™). Keep SW4 on the demo board pressed before and during the start of the programming process. Once completed, turn off the power and remove the JTAG connector.
3. Observe the scrolling LED sequence on the red LEDs and the bi-color LEDs. Pressing SW9 on the demo board disables the internal oscillator, and the scrolling LEDs will freeze at their current positions.

Source Code

This design example has been implemented in Verilog and successful operation has been demonstrated using the MDN-B2 demo board, as described in this document. The source code, testbench, and complete Quartus II project are available at:

www.altera.com/literature/an/an496_design_example.zip

Conclusion

MAX II CPLDs offer a unique internal oscillator feature in addition to low power programmable logic solutions and a host of other features. As illustrated by this design example, they make an excellent choice to implement designs that require clocking, thereby saving on-board space and costs associated with external clocking circuitry.

Additional Resources

- MAX II CPLD Homepage:
www.altera.com/products/devices/cpld/max2/mx2-index.jsp
- MAX II Device Literature:
www.altera.com/literature/lit-max2.jsp
- MAX II Power-Down Designs:
www.altera.com/support/examples/max/exm-power-down.html
- MAX II Application Notes:
 - *AN 422: Power Management in Portable Systems Using MAX II CPLDs*
 - *AN 428: MAX II CPLD Design Guidelines*

Document Revision History

Table 3 shows the revision history for this application note.

Date and Document Version	Changes Made	Summary of Changes
December 2007 v1.0	Initial release.	—



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