

## Introduction

Powering components off and on—with minimal system intervention (also known as blink)—is a valuable power savings technique. Altera® MAX® II CPLDs are well suited for this due to their simple power sequencing and proprietary features. This application note illustrates a simple method for blinking an LED by using the auto stop and auto start capability of MAX II CPLDs.

## Power Saving Using Auto Stop and Auto Start

Many consumer and industrial application systems do not require the CPLD to be powered on at all times. In fact, it is preferable to have a system in which the CPLD powers on intermittently, as and when required only, and remains off for most of the cycle. MAX II CPLDs are designed to tolerate any possible power-on sequence. They also have one of the industry's lowest power-up timing characteristics (typically 200 microseconds for the EPM240 device, depending on the density of logic in the design).

This makes the MAX II CPLDs the perfect target device for such a system. The CPLD can be turned off when a task is complete and switched back on again for its next task. The self power down is caused by the CPLD itself, while the auto power up is caused by an external circuitry such as a simple RC circuit designed for the required delay. The entire scheme finds context in power savings, typically in battery operated systems which may be used for functions that are cyclical or periodic in nature (such as sampling for parameters in a telemetering system), where the power can be turned off when the CPLD can afford to take a break.

The CPLD generates two signals, power down and its complement to cause self power down by triggering an external circuit to shutdown the LDO supplying power to the CPLD. After the CPLD is off, the external circuit powers it back on after the designed delay of the external RC circuit. An LED glows upon power on and switches off after the CPLD is powered down. [Figure 1](#) illustrates implementing a power-down circuit using a MAX II CPLD.

Figure 1. Implementing a Power-Down Circuit with a MAX II CPLD

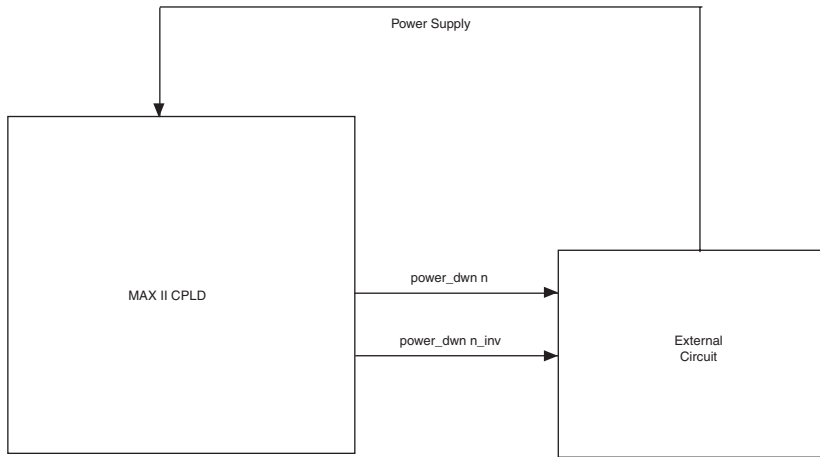
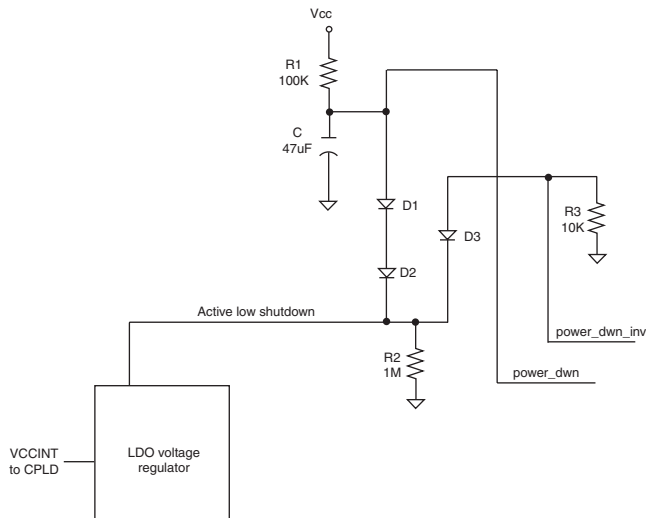


Figure 2 illustrates the external circuitry shown in Figure 1.

Figure 2. External Circuitry for a Power-Down Circuit with a MAX II CPLD



This section discusses the self-power-down and auto-power-up capability of the MAX II CPLD. An LED indicates power to the CPLD. When the CPLD is on, the `power_dwn` signal is low (`power_dwn_inv` is high). The shutdown pin on the LDO is inactive (active low) and the LDO (shown in [Figure 2](#)) continues to remain on. Capacitor C is kept in its discharged condition.

When the CPLD switches off, the `power_dwn` signal goes high (`power_dwn_inv` goes low). This causes the LDO to shutdown, and thereby switching off the CPLD. The I/O pins on the CPLD get tri-stated, releasing the pull down on the capacitor. The capacitor starts charging with the time constant  $R1 \cdot C$ . It charges until the voltage across it remains less than the threshold potential of the shutdown pin on the LDO (enhanced by voltage drops across diodes D1 and D2). When the threshold is reached, the LDO turns on and, consequently, the CPLD turns on. This cycle continues to repeat itself.

You can implement the steps in this application note with an EPM240G device, or any other MAX II CPLD, simple external RC circuitry, and a power supply that is capable of shut-down. Implementation involves using this example's source code and allocating the appropriate signal and control lines to the general purpose I/O (GPIO) lines of the MAX II CPLD along with its support circuitry. The demo board MDN-B2 is a board with such support circuitry built-in. An LED on the demo board is made to indicate the power status of the MAX II CPLD. The demo board also facilitates power measurements by allowing measurement of voltage drops across a 1- $\Omega$  resistor in series with the CPLD core power supply.

The following details the implementation of this example on the MDN-B2 demo board. [Table 1](#) lists the EPM240G pin assignments for the example.

<i>Table 1. Example Implementation Using the MDN-B2 Demo Board</i>	
EPM240G Pin Assignments	
Signal	Pin
<code>power_on_led</code>	69
<code>power_dwn_inv</code>	12
<code>power_dwn</code>	14



Unused pins are assigned as **input tri-stated** in the Quartus II software's device and pin option settings prior to compilation.

## Design Notes

To demonstrate this design on the MDN-B2 demo board, complete the following:

1. Turn on the power to the demo board (using the slide switch SW1).
2. Download the design on to the MAX II CPLD through the JTAG header JP5 on the demo board and a conventional programming cable (ByteBlaster™ II or USB-Blaster™). Keep SW4 on the demo board pressed before and during the start of the programming process. Once complete, turn off the power and remove the JTAG connector.
3. Switch on power to the demo board (using the slide switch SW1) and observe VCCINT and VCCIOs being cyclically powered down and powered up.
4. Observe the LEDs D2 glow each time the power to CPLD is restored.
5. Measure the voltage drops across R52 for the 2.5 V power supply (pads TP1 and TP2) and across R27 for the 1.8 V power supply (pads TP3 and TP4).

## Source Code

This design has been implemented in Verilog and successful operation has been demonstrated using the MDN-B2 demo board, as referenced in the documentation. The source code, test bench, and complete Quartus II project are available at:

[www.altera.com/literature/an/an498\\_design\\_example.zip](http://www.altera.com/literature/an/an498_design_example.zip)

## Conclusion

MAX II CPLDs are an excellent choice when implementing low power applications and when extending battery life is important. MAX II CPLD's low power and unique feature of quick and easy power on, without the requirement of any power-up sequence, allows them to self power down during idle states and between tasks. This, in combination with the auto start functionality to regain power quickly, greatly increases the CPLD's ability to save power.

## Additional Resources

The following are additional resources for this application note:

- MAX II CPLD home page:  
<http://www.altera.com/products/devices/cpld/max2/mx2-index.jsp>

- MAX II Device Literature page:  
<http://www.altera.-com/literature/lit-max2.jsp>
- MAX II Power-Down Designs:  
<http://www.altera.com/support/examples/max/exm-power-down.html>
- MAX II Application Notes:  
*AN 428: MAX II CPLD Design Guidelines*  
*AN 422: Power Management in Portable Systems Using MAX II CPLDs*

## Document Revision History

Table 2 shows the revision history for this application note.

<i>Table 2. Document Revision History</i>		
Date and Document Version	Changes Made	Summary of Changes
December 2007, v1.0	Initial release.	—



101 Innovation Drive  
San Jose, CA 95134  
[www.altera.com](http://www.altera.com)  
Technical Support:  
[www.altera.com/support](http://www.altera.com/support)  
Literature Services:  
[literature@altera.com](mailto:literature@altera.com)

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