

## Introduction

This document details the implementation of a NAND Flash Memory Interface using an Altera® MAX® II CPLD. You can use the design with both Samsung and AMD NAND Flash memories.

## Flash Memory

Flash memory is a non-volatile form of semiconductor memory that can be electrically programmed and reprogrammed. It stores information in arrays of cells, with each cell storing one bit of information. The cells have a dual gate structure in which a floating gate exists between a control gate and the silicon substrate of a MOSFET. A silicon-dioxide insulator is used to isolate this floating gate. This is the basic storage mechanism of a flash memory device.

NOR flash and NAND flash are two variations of flash memory devices. A NOR-type flash memory allows random access, whereas NAND-type flash memory is a sequential access device. These two types vary largely in their interface. NOR-type flash memories incorporate dedicated address lines and data lines, whereas NAND-type memories have no dedicated address lines.

Comparison of a NOR-type with a NAND-type yields significant advantages, such as lower cost per bit due to smaller cell area, higher density, better endurance, and lower erasing and programming time for a NAND-type. These advantages make the NAND Flash memory a better choice for use in products, such as: USB flash drives, mp3 players, digital audio recording, data storage in digital Telephone Answering Devices (TAD), digital cameras, and in memory cards like CompactFlash and MemoryStick.

This document details the implementation of a NAND Flash Memory Interface in an Altera MAX II CPLD. You can use the design with both SAMSUNG and AMD NAND Flash memories. The AMD Am30LV0064D and Samsung K9F4008W0A flash devices are used in the example.

The AMD NAND Flash device (Am30LV0064D) is a 64-Mbit mass storage device suited for high density applications in which data is sequential and requires fast write capability. The initial page read access time is 7  $\mu$ s with subsequent byte accesses of less than 50 ns.

The Samsung NAND FLASH device (K9F4008W0A) is a 512 K × 8-bit storage device suited for applications that do not require the high performance levels or the capacity of larger density flash memories. It supports 32-byte Frame read operations with a random access time of 15 μs and a sequential access time of 120 ns.

## NAND Flash Interface Using MAX II

Figure 1 shows the interface block diagram. The commands from the system arrive at the inputs of the NAND Flash interface in coded form. Each operation performed is coded in a different format and issues through the 3-bit wide control bus. Refer to Table 2 on page 4.

The pin descriptions for the interface are given in Table 1. Enabling or disabling (in the case of ALE, CLE, SE, and WE) is done separately with the help of enable/disable signal inputs. These commands are decoded correctly by the NAND Flash interface block (Altera MAX II CPLD) and translated as output enabling or disabling signals, which ensures the desired operation of the NAND Flash.

The actual operation performed by a NAND Flash is governed by the commands written into its command register through the I/O bus. (Refer to Table 3 on page 4. Refer to Table 4 on page 5.). The address of the data that is read or written, together with the data, are issued through the same bus.

Figure 1 shows the different interfacing signals of the NAND Flash device. The signals followed by a '#' are asserted when low.

Figure 1. Interfacing Signals of the NAND Flash Device

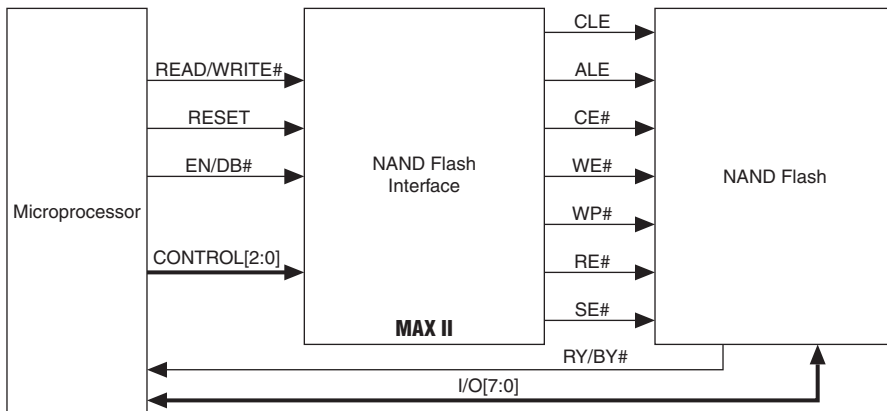


Table 1 describes the interfacing signals.

<b>Table 1. Description of the Signals Present in the Block Diagram of Figure 1 (Part 1 of 2)</b>		
<b>Signal</b>	<b>Size</b>	<b>Description</b>
READ/WRITE#	1-bit	Input from the microprocessor to distinguish between a write and a read operation: <ul style="list-style-type: none"> <li>● READ/WRITE# 0: Write operation.</li> <li>● READ/WRITE# 1: Read operation.</li> </ul>
RESET	1-bit	Input from the microprocessor to reset the NAND Flash device.
CONTROL [2 : 0]	3-bit	3-bit control bus. The microprocessor sends 3 bits of information to the NAND Flash interface (Altera Max II device) where it is suitably decoded. The appropriate interfacing signals are enabled or disabled depending on the condition of the EN/DB# input.
EN/DB#	1-bit	Control bit used in conjunction with the control bits to perform the required operation. <ul style="list-style-type: none"> <li>● EN/DB# 1: Enables the interfacing signal selected by the control bits.</li> <li>● EN/DB# 0: Disables the interfacing signal selected by the control bits.</li> </ul>
I/O [7 : 0]	8-bit	Bidirectional 8-bit multiplexed bus used to send data/command/address to their respective registers in the NAND Flash device. The data read from the NAND Flash device is also available on these lines.
RY/BY#	1-bit	Output from the NAND Flash device, indicating the status of the device. <ul style="list-style-type: none"> <li>● RY/BY# 0 : Device is still busy performing an operation.</li> <li>● RY/BY# 1 : Device is ready to accept the next command.</li> </ul>
CLE	1-bit	Active high Command Latch Enable. Use to select the Command Register or the Data Register of the device. When high, the command on the I/O lines is latched into the command register on the rising edge of WE#. (1)
ALE	1-bit	Active high Address Latch Enable. Use to select the Address Register or the Data Register of the device. When high, the address on the I/O lines is latched into the address register on the rising edge of WE#. A low signal will cause the device to reset. This signal must remain high for the entire address sequence. (1)
CE#	1-bit	Active low Chip Enable. Use to choose between the active mode and the standby mode of the device. <ul style="list-style-type: none"> <li>● CE# 0 : Active mode selected.</li> <li>● CE# 1 : Standby mode is selected if no operation is currently in progress.</li> </ul> <p>The CE signal is ignored if a program or erase operation is in progress.</p>
WE#	1-bit	Active low Write Enable. Use to write command/address/data into their respective registers in the device. The information on the I/O lines is latched into the respective registers on the rising edge of WE#.
WP#	1-bit	Active low Write Protect. <p>WP# 0 : Device is write protected.</p> <p>WP# 1 : Device is not write protected.</p>
RE#	1-bit	Active low Read Enable. Use to read data/status to/from the device. The information is available on the I/O lines on the rising edge of RE#.

**Table 1. Description of the Signals Present in the Block Diagram of Figure 1 (Part 2 of 2)**

Signal	Size	Description
SE#	1-bit	Active low Spare area Enable. Required only when an AMD device is used. Not required for a Samsung device. <ul style="list-style-type: none"> <li>SE# 0 : 16 bytes of Spare area on each page is enabled.</li> <li>SE# 1 : Spare area is disabled.</li> </ul>

**Notes to Table 1:**

- (1) Data Register is selected by making both CLE and ALE low. The data on the I/O lines is latched into the Data Register on the rising edge of WE#.

**Table 2. Operations Performed by the Interface on Different Combinations of the Control Signals**

Control Signal [2:0]	EN/DB#	Operation performed
000	—	Command Latch Enabled (CLE = 1) irrespective of the condition on EN/DB#.
001	—	Read Data / status / device depend on the command sent on the I/O lines.
010	—	Write Data / command /address depending on the command sent on the I/O lines.
011	1 0	ALE is asserted (high). ALE is disabled (low).
100	1 0	SE# is asserted (low). SE# is disabled (high). (1)
101	1 0	WP# is asserted (low). WP# is disabled (high).
110	1 0	CE# is asserted (low). CE# is disabled (high).
111	1 0	The status of the flash device is sent on the RY/BY# line. RY/BY# line does not reflect the status of the flash device

**Note to Table 2:**

- (1) This operation is only applicable for AMD flash devices. This command enables/disables the 16 bytes of spare area on each page depending on the condition of the EN/DB# line.

Tables 3 and 4 provide information on the various commands supported by the AMD NAND Flash device (Am30LV0064D) and the Samsung NAND Flash device (K9F4008W0A).

**Table 3. Am30LV0064D COMMAND SET**

Operation	Cycle 1	Cycle 2	Valid During Busy
Read data	00h/01h	—	No
Gapless Read (1)	02h	—	No

Operation	Cycle 1	Cycle 2	Valid During Busy
Read Spare Area	50h	—	No
Read ID	90h	—	No
Read Status	70h	—	Yes
Input Data (2)	80h	—	No
Page Program (2)	10h	—	No
Block Erase (3)	60h	D0h	No
Erase Suspend (1)	B0h	—	Yes
Erase Resume (1)	D0h	—	No
Reset	FFh	—	Yes

**Notes to Table 3:**

- (1) Superset Command supported by the AMD NAND Flash device only.
- (2) Programming data into the flash array is a two step process and requires two separate command sequences to be performed. The data to be programmed must be loaded into the data registers using the Input data command sequence. After the data is loaded the Page Program command is performed to transfer the information from the data registers to the flash array.
- (3) Block Erase is also a two command procedure. In the first command cycle the address of the block to be erased is issued to the device. In the second command cycle the flash device begins the erase operation when it encounters a rising edge on the WE# signal.

Programming of the Flash device occurs on a Page basis (512 bytes + 16 bytes of spare area), whereas the erasure takes place on a Block basis (8 K byte + 256 bytes).

Erase Suspend and Erase Resume are provided to allow time critical tasks to be performed. These tasks can only be performed on the block that is not being currently erased. Gapless Read is used to read out data in a special high-performance mode. This allows reading from multiple pages with only a 7  $\mu$ s latency on the first page transfer.



Further information on the AMD NAND Flash device can be obtained at [www.spansion.com/datasheets/22203c4.pdf](http://www.spansion.com/datasheets/22203c4.pdf).

Operation	Cycle 1	Cycle 2	Valid During Busy
Read Data	00h	—	No
Read ID	90h	—	No
Read Status	70h	—	Yes

**Table 4. K9F4008W0A COMMAND SET**

Operation	Cycle 1	Cycle 2	Valid During Busy
Frame Program (1)	80h	10h	No
Block Erase (2)	60h	D0h	No
Reset	FFh	—	Yes

**Notes to Table 4:**

- (1) Frame Program is a two command procedure: Loading of the data that has to be programmed starts with the Frame Program setup command (80h). The Frame Program confirm command (10h) initiates the programming process.
- (2) Block erase is also a two command procedure: The address of the block to be erased is loaded with the Erase setup command (60h). The Flash device initiates the internal erasing process when the Erase confirm command (D0h) is loaded.

Programming of the flash device takes place on a Frame basis (32 bytes), whereas the erasure takes place on a block basis (4 K byte). The device also supports partial frame programming.



Further information on the Samsung NAND Flash device can be obtained at: [www.datasheet4u.com/html/K/9/F/K9F4008W0A-\\_Samsungsemiconductor.pdf.html](http://www.datasheet4u.com/html/K/9/F/K9F4008W0A-_Samsungsemiconductor.pdf.html)

## Implementation

You can implement this design using an EPM240 or any other MAX II CPLD. The design source code is compiled and can be programmed into a MAX II CPLD. Host interfacing ports and NAND Flash device interfacing ports are shown in [Figure 1 on page 2](#). This NAND Flash interface design is illustrated to work with the AMD NAND Flash device Am30LV0064D and the Samsung NAND Flash device K9F4008W0A.

## Source Code

The design example is implemented in Verilog HDL. The source code, test bench, and complete Quartus II project are available at:

[www.altera.com/literature/an/an500\\_design\\_example.zip](http://www.altera.com/literature/an/an500_design_example.zip)

## Conclusion

As illustrated through this design example, MAX II CPLDs are a great choice to implement interfaces to memory devices such as the NAND Flash. Their low power and easy power-on feature make them ideal programmable logic devices to implement such memory device interfacing applications.

## Additional Resources

The following list contains additional resources:

- MAX II CPLD homepage:  
[www.altera.com/products/devices/cpld/max2/mx2-index.jsp](http://www.altera.com/products/devices/cpld/max2/mx2-index.jsp)
- MAX II Device Literature:  
[www.altera.com/literature/lit-max2.jsp](http://www.altera.com/literature/lit-max2.jsp)
- MAX II Power-Down Designs:  
[www.altera.com/support/examples/max/exm-power-down.html](http://www.altera.com/support/examples/max/exm-power-down.html)
- MAX II App Notes:  
AN 428: MAX II CPLD Design Guidelines  
AN 422: Power Management in Portable Systems Using MAX II CPLDs

## Revision History

Table 5 shows the revision history to this application note.

<i>Table 5. Revision History</i>		
Date and Version	Changes Made	Comments
December 2007, v1.0	Initial Release	—



101 Innovation Drive  
San Jose, CA 95134  
[www.altera.com](http://www.altera.com)  
Literature Services:  
[literature@altera.com](mailto:literature@altera.com)

Copyright © 2007 Altera Corporation. All rights reserved. Altera, The Programmable Solutions Company, the stylized Altera logo, specific device designations, and all other words and logos that are identified as trademarks and/or service marks are, unless noted otherwise, the trademarks and service marks of Altera Corporation in the U.S. and other countries. All other product or service names are the property of their respective holders. Altera products are protected under numerous U.S. and foreign patents and pending applications, maskwork rights, and copyrights. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera Corporation. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

