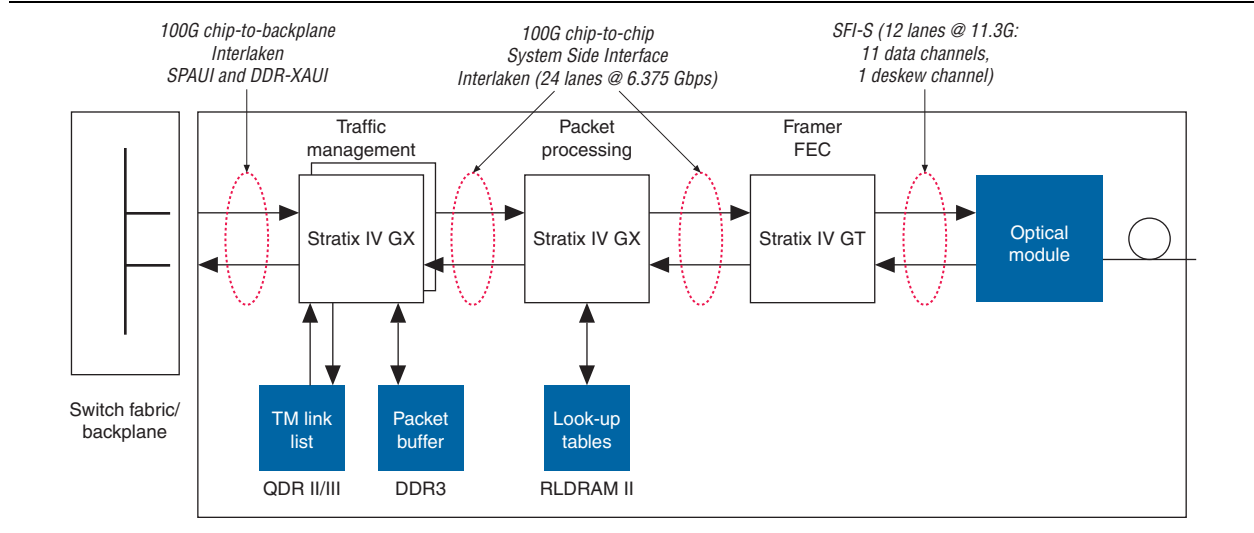


## Introduction

This application note describes the transceiver features in Stratix® IV GT devices that implement the Scalable SERDES Framing Interface (SFI-S) protocol. The transceiver configuration and clocking scheme for this protocol implementation are also described.

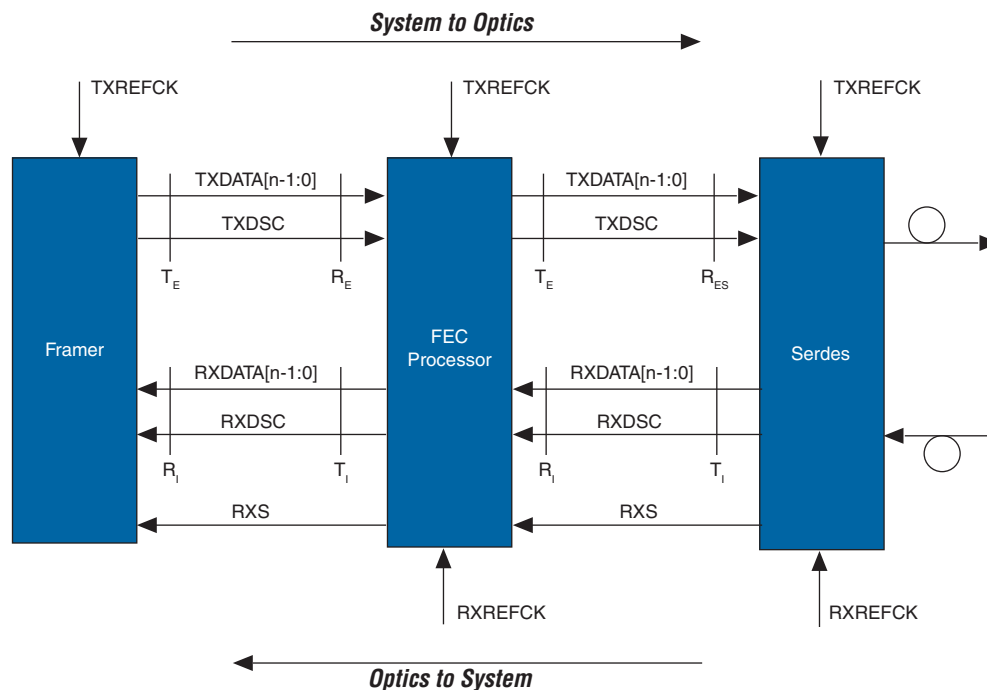
SFI-S is a high-speed serial communication protocol for 40 Gbps/100 Gbps optical interface systems. The protocol defines multi-lane data channels and a deskew channel with each channel running between 9.95 Gbps and 11.3 Gbps. The number of data channels can vary from 4 to 20, depending on the aggregate bandwidth requirements. Figure 1 shows an example of a 100 Gbps line card application using the SFI-S protocol.

**Figure 1.** Example 100 Gbps Line Card Application



The SFI-S protocol defines a system interface model between the different components, as shown in [Figure 2](#).

**Figure 2.** SFI-S System Reference Model (*Note 1*)



**Note to Figure 2:**

(1) From *Scalable Serdes Framer Interface (SFI-S): Implementation Agreement for Interfaces Beyond 40G for Physical Layer Devices*. Optical Internetworking Forum, OIF-SFI-S-01.0, November 2008 ([www.oiforum.com](http://www.oiforum.com)).


The TXDATA/TXDSC and RXDATA/RXDSC signals represent the data channels and the deskew channel on the transmitter and receive sides, respectively. RXS is the receive status signal that indicates whether RXDATA is derived from the optical receive signal. The source device on the receive interface must generate this signal. It is optional for the sink device in the receive interface to use this signal. TXREFCK and RXREFCK are the input reference clocks with a frequency equal to 1/16th of the serial data rate. Some implementations use a single reference clock source to connect to the TXREFCK and RXREFCK clocks.

The SFI-S protocol follows the CEI 11G SR Electrical specification. Other key requirements of the SFI-S Implementation Agreement (reference 1) include the following:

- Maximum transmit channel-to-channel skew—5.5 unit intervals (UI) measured at points marked by  $T_I$  and  $T_E$  in [Figure 2](#).
- Maximum total wander—5.65 UI measured at points marked by  $T_I$  and  $T_E$  in [Figure 2](#).
- Recommended deskew capability for downstream receivers—84 UI between lanes (refer to Appendix A in reference 1).

## Stratix IV GT Support


Stratix IV GT devices provide the transceiver features required to implement an SFI-S application. You can use a Stratix IV GT device in place of any of the components shown in the SFI-S System Reference Model.

-  The number of transceiver channels capable of running at 10 Gbps and above varies between device packages. For more information about the number of transceivers available in a given device package, refer to the [Stratix IV Device Family Overview](#) chapter in volume 1 of the *Stratix IV Device Handbook*.

A Stratix IV GT device provides a CMU PLL that generates high-speed and low-speed clocks to the transmitter channels. The CMU PLL supports the data rate range to 11.3 Gbps. Each receiver channel has a dedicated clock and data recovery (CDR) unit to recover clock and data from the serial data.

The Stratix IV GT devices support the required input clock frequency value of 1/16th the serial data rate required by the SFI-S protocol. For example, for the SFI-S data rate of 11.3 Gbps, a Stratix IV GT device supports a 706.25-MHz input reference clock frequency. Depending on your implementation, you can provide the same or different input reference clocks to the CMU PLL and to the RXCDR through the dedicated `refclk` pins.

You can implement the `RXS` signal using the FPGA fabric I/O pins configured in the LVCMOS I/O standard.

-  For more information about transceiver architecture, refer to the [Stratix IV Transceiver Architecture](#) chapter in volume 2 of the *Stratix IV Device Handbook*. For Stratix IV GT device resources, refer to the [Stratix IV Device Family Overview](#) chapter in volume 1 of the *Stratix IV Device Handbook*.

## Transceiver Configuration to Meet Relaxed Skew Requirements

Appendix A of the SFI-S Implementation Agreement (reference 1) recommends that receivers tolerate up to 84 UI skew between the lanes. If your implementation follows this recommendation, you can use the Basic  $\times 4$  configuration available through the ALTGX MegaWizard<sup>®</sup> Plug-In Manager to implement a 12-channel SFI-S design in three transceiver blocks. In this configuration, the transmit phase compensation FIFO and the byte serializer are synchronized, eliminating the transmit skew from these blocks between the four transmitter channels in the transceiver block. The CMU0 channel in each transceiver block provides high-speed serial and low-speed parallel clocks through the  $\times 4$  clock lines. Because independent CMU0 channels are used for clock generation, the skew between the transmitter channels from the phase compensation FIFO and byte serializer from each transceiver block is 40 UI and 20 UI, respectively. The skew on the  $\times 4$  clock line is less than 2 UI (1 UI = 1/11.3 Gbps). The total transmitter channel-to-channel skew between twelve channels is approximately 62 UI.

To configure a transceiver in basic  $\times 4$  mode, select the following options on the **General** tab in the ALTGX MegaWizard Plug-In Manager:

- Which protocol will you be using?: **Basic**
- Which subprotocol will you be using?:  **$\times 4$**

- What is the operation mode?: **Transmitter and Receiver**
- What is the number of channels?: **12**
- What is the effective data rate?: **11300**
- What is the input clock frequency?: **706.25 MHz**

Select the following options on the **Ports/Cal Blk** tab:

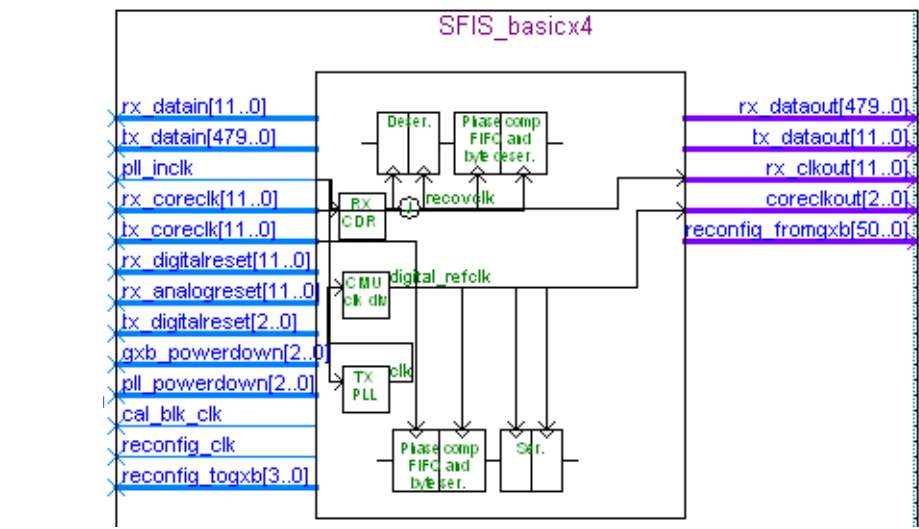
- Enable the rx\_coreclk and tx\_coreclk ports

Select the following option on the **Basic/8B10B** tab:

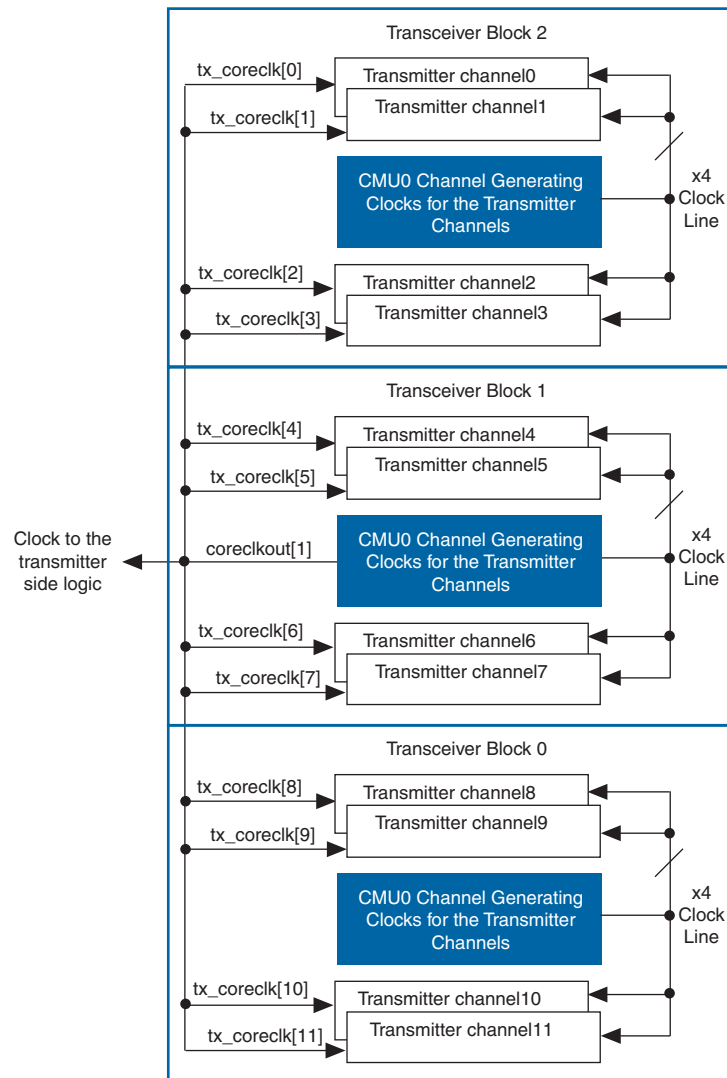
- **Enable Low Latency PCS mode**

Figure 3 and Figure 4 show the basic ×4 instance generated by the ALTGX MegaWizard Plug-In Manager with 12 transceiver channels and the placement of these channels after compilation.

**Figure 3.** Basic ×4 Transceiver Instance with 12 Transceiver Channels



**Figure 4.** Placement of Transceiver Channels and the CMU PLLs for the Basic ×4 Instance with 12 Channels



To minimize the number of clock resources used, enable the `tx_coreclk` and `rx_coreclk` ports in the ALTGX MegaWizard interface. These clock ports allow you to use one clock for the write side of the TX phase compensation FIFO for the transmitter channels and one clock for the read side of the phase compensation FIFO for the receiver channels. To use these clock ports with the circuit shown in Figure 4, connect `coreclkout[1]` to the `tx_coreclk[11:0]` and `rx_coreclk[11:0]` ports of the ALTGX instance.

To compile designs using the `tx_coreclk` and `rx_coreclk` ports, you must provide a GXB 0 PPM core clock setting in the Quartus II Assignment Editor. For more information about this assignment, refer to the “FPGA Fabric-Transmitter Interface Clocking” and “FPGA Fabric-Receiver Interface Clocking” sections in the *Stratix IV Transceiver Clocking* chapter in volume 2 of the *Stratix IV Device Handbook*.

## Reference

This application note refers to the following document:

1. *Scalable Serdes Framer Interface (SFI-S): Implementation Agreement for Interfaces Beyond 40G for Physical Layer Devices*. Optical Internetworking Forum, OIF-SFI-S-01.0, November 2008. ([www.oiforum.com](http://www.oiforum.com))

## Document Revision History

Table 1 lists the revision history for this application note.

**Table 1.** Document Revision History

Date and Document Version	Changes Made	Summary of Changes
January 2010 v2.0	Removed information on transmitter and receiver interface clocking. Also made other minor editorial changes.	—
June 2009 v1.0	Initial release.	—



101 Innovation Drive  
San Jose, CA 95134  
[www.altera.com](http://www.altera.com)  
Technical Support  
[www.altera.com/support](http://www.altera.com/support)

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