

Introduction

Although the 5.0-V interface has been a standard for decades, the move towards advanced process technology requires a shift to lower voltage levels. In today's market, printed circuit boards (PCBs) are assembled with a mixture of 5.0-V, 3.3-V, 2.5-V, and 1.8-V devices. To accommodate this mixture seamlessly, it is essential that these devices interface with systems of differing supply voltages.

Altera's MultiVolt™ I/O interface meets the increasing demand for compatibility with devices of different voltages. The MultiVolt interface separates the power supply voltage from the output voltage, enabling Altera® devices to interface with other devices using different voltage levels on the same PCB. Altera has taken further steps by incorporating support for hot-socketing, which refers to inserting or removing cards or boards from a back plane during operation. Hot-socketing is a common requirement for high-reliability systems. Altera offers a variety of devices that support hot-socketing.

This application note discusses several features that allow you to implement Altera devices in multiple voltage systems without damaging the device or the system, including:

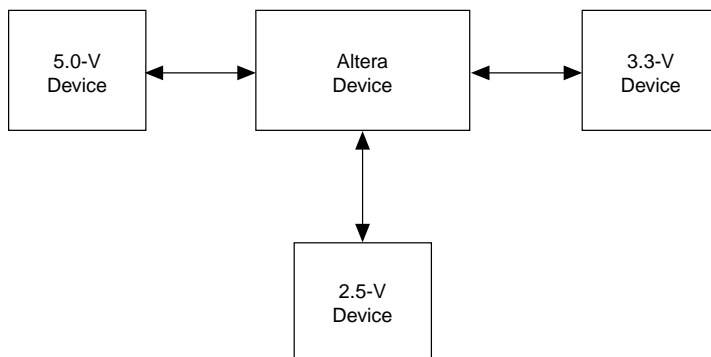
- MultiVolt Interface
- Hot-Socketing
- Power-Up Sequence
- Power-On Reset (POR)

MultiVolt Interface

Advanced-process devices require 3.3-V, 2.5-V, or 1.8-V power supplies. However, other devices on a board may still use 5.0-V or 3.3-V supplies. A programmable logic device (PLD) must interface with these other devices. In the future, even lower voltage levels will be required for smaller process geometries.

To accommodate the need to interface with a variety of devices, Altera has developed the broadest range of MultiVolt I/O interfaces. The MultiVolt I/O interface allows devices to communicate in a mixed-voltage design environment. The device core and I/O pins can be powered-up with separate supply voltages. The VCCINT pins power the device core and the VCCIO pins power the I/O buffers for most devices. All device VCCIO pins that have MultiVolt capability should be supplied from the same voltage level (e.g., 5.0 V, 3.3 V, 2.5 V, or 1.8 V). See [Figure 1](#).

Figure 1. MultiVolt I/O Interface Feature for Altera Devices Note (1)



Note to Figure 1:

- (1) The Altera device can interact with each voltage one at a time, but not simultaneously (except APEX™ 20KE and MAX® 7000B devices, which can have different V_{CCIO} levels simultaneously).

5.0-V Device Compatibility

5.0-V devices—FLEX® 10K, MAX 9000, MAX 7000S, MAX 7000, FLEX 8000, and 5.0-V FLEX 6000 devices—support interfaces to 3.3-V and 5.0-V devices.

3.3-V Device Compatibility

When using 3.3-V devices—FLEX 10KA, 3.3-V FLEX 6000, MAX 7000A, and MAX 3000A devices—the V_{CCINT} pins must be connected to a 3.3-V power supply. The V_{CCIO} pins can be connected to either a 2.5-V or 3.3-V power supply, depending on the output requirements. When the V_{CCIO} pins are connected to a 3.3-V power supply, the output high is 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. The device can also drive other 3.3-V tolerant, 2.5-V devices. Inputs for the above devices can always be driven by 2.5-V, 3.3-V, or 5.0-V systems, except for EPF10K50V and EPF10K130V devices, which can only be driven by 3.3-V and 5.0-V systems.

2.5-V Device Compatibility

The V_{CCINT} pins on 2.5-V APEX 20K, ACEX™ 1K, FLEX 10KE, and MAX 7000B devices must be connected to a 2.5-V power supply. The V_{CCIO} pins can be connected to either a 2.5-V or 3.3-V power supply, depending on the output requirements. When the V_{CCIO} pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the V_{CCIO} pins are connected to a 3.3-V power supply, the output high is 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. The device can also drive other 3.3-V tolerant, 2.5-V devices.



The APEX 20K device family incorporates a wider variety of I/O standards. This device family is covered in [Application Note 117 \(Using Selectable I/O Standards in Altera Devices\)](#).

Table 1 summarizes Altera MultiVolt I/O support.

Table 1. Altera MultiVolt I/O Support <i>Notes (1), (2)</i>										
Device	V_{CCINT} (V)	V_{CCIO} (V)	Input Signal (V)				Output Signal (V)			
			1.8	2.5	3.3	5.0	1.8	2.5	3.3	5.0
FLEX 10K, FLEX 8000, FLEX 6000 (5.0 V), MAX 7000S, MAX 9000	5.0	5.0			✓	✓				✓
		3.3			✓	✓			✓	✓
EPF10K50V, EPF10K130V	3.3	3.3			✓	✓			✓	✓
FLEX 10KA, FLEX 6000 (3.3 V), MAX 7000A, MAX 3000A	3.3	3.3		✓	✓	✓			✓	✓
		2.5		✓	✓	✓		✓		
FLEX 10KE	2.5	3.3		✓	✓	✓			✓	✓
		2.5		✓	✓	✓		✓		
ACEX 1K	2.5	3.3		✓	✓	✓			✓	✓
		2.5		✓	✓	✓		✓		
APEX 20K (3)	2.5	3.3		✓	✓				✓	
		2.5		✓	✓			✓		
APEX 20KE (3), (4)	1.8	3.3	✓	✓	✓				✓	
		2.5	✓	✓	✓			✓		
		1.8	✓	✓	✓		✓			
MAX 7000B	2.5	3.3	✓	✓	✓				✓	
		2.5	✓	✓	✓			✓		
		1.8	✓	✓	✓		✓			

Notes to Table 1:

- (1) All FLEX 10K devices support 3.3-V I/O pins with a 5.0-V core, except 84-pin plastic J-lead chip carrier (PLCC) and 240-pin quad flat pack (QFP) packages. All MAX 7000S devices—except EPM7032S and EPM7064S devices in the 44-pin PLCC and thin quad flat pack (TQFP) packages—support 3.3-V I/O pins with a 5.0-V core.
- (2) The EPF8282V I/O pins are not 5.0-V tolerant. Altera does not recommend driving 5.0-V signals to these 3.3-V devices.
- (3) APEX 20K and APEX 20KE I/O pins are not 5.0-V tolerant.
- (4) For more information on APEX 20KE MultiVolt support, see *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

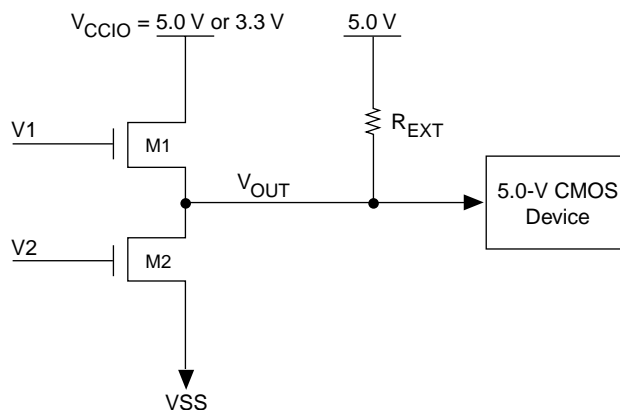
5.0-V TTL Compatibility

Altera 5.0-V tolerant devices are 5.0-V TTL compatible. For example, a 3.3-V device can drive a 5.0-V device, and in return, can be driven by a 5.0-V device. Additionally, when the V_{CCIO} pins on a 5.0-V device are connected to 3.3 V, the I/O pins can still be driven by 5.0-V signals because the I/O buffers are still 5.0-V tolerant.

5.0-V CMOS Compatibility

Altera's 5.0-V devices with NMOS-only output buffers meet 5.0-V TTL levels. When the voltage at the output pin exceeds approximately 3.8 V, the NMOS pull-up transistor goes to cut-off mode. Therefore, you can use an external pull-up resistor to pull up the signal to 5.0 V. See Figure 2.

Figure 2. 5.0-V Altera Device Compatibility with 5.0-V CMOS Devices *Note (1)*

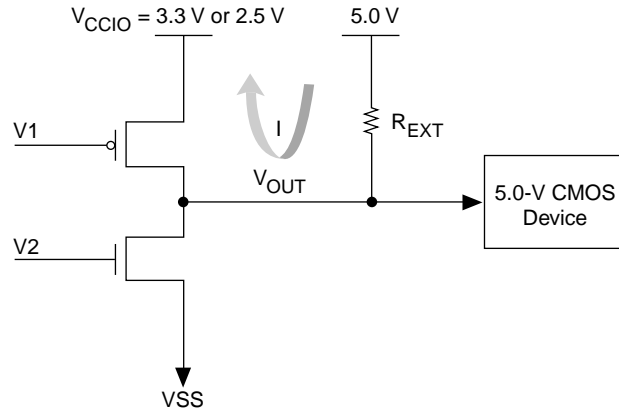


Note to Figure 2:

- (1) When $V_{OUT} \geq 3.8$ V, transistor M1 is cut-off. As a result, the external resistor (R_{EXT}) can pull up the output node (V_{OUT}) to a full rail level of 5.0 V.

To make Altera low-voltage device outputs compatible with 5.0-V CMOS devices, configure the output pins as open-drain pins and use an external pull-up resistor. The low-voltage devices have a CMOS driver; if $V_{OUT} > V_{CCIO}$, the PMOS pull-up transistor still conducts if the pin is driving high, preventing an external pull-up resistor from pulling the signal to 5.0 V (see Figure 3). 5.0-V tolerant, 3.3-V and 2.5-V devices can also drive 5.0-V CMOS devices.

Figure 3. CMOS Output Buffer for Altera Low-Voltage Devices *Note (1)*

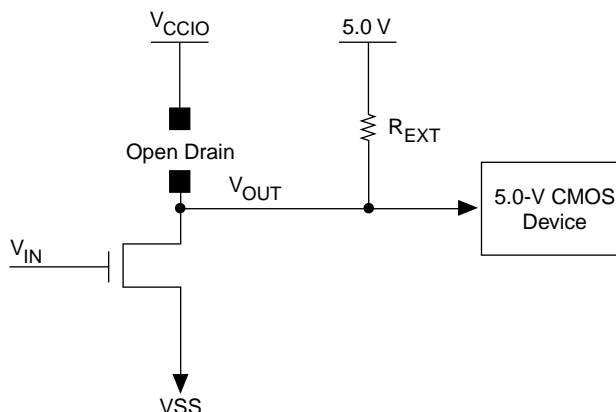


Note to Figure 3:

- (1) When $V_{OUT} > V_{CCIO}$, the current will flow as shown above. As a result, the V_{OUT} node cannot be pulled to 5.0 V.

To pull the output of a low-voltage device up to the V_{IH} (input high) level of a 5.0-V CMOS device, use an open-drain pin driving a trace that is pulled up to 5.0 V through an external pull-up resistor (see Figure 4). Choose a pull-up resistor that is small enough for a sufficient signal rise time, but large enough that it does not violate the I_{OL} (output low) specifications of devices driving that trace.

Figure 4. Low-Voltage Altera Device Compatibility with 5.0-V CMOS Devices *Note (1)*



Note to Figure 4:

- (1) To pull the V_{OUT} to the rail of 5.0 V, ensure that the output is an open drain. Therefore, the external pull-up resistor (R_{EXT}) pulls V_{OUT} to 5.0 V.

The open-drain pin never drives high, only low or tri-state. When the open-drain pin is active, it drives low. When the open-drain pin is inactive, the pin is tri-stated and the trace pulls up to 5.0 V by the external resistor. The device operates successfully because a 5.0-V input is within its input specification.

Hot-Socketing

Hot-socketing, hot-swap, or hot plug-in refers to inserting or removing a board or device into or out of a system board while system power is on. For a system to support hot-socketing, plug-in or removal of a board must not damage the system or interrupt system operation.

Hot-Socketing in Altera Devices

The following Altera 3.3-V, 2.5-V, 1.8-V and 1.8-5 devices are designed to support hot-socketing without special design requirements:

- Mercury™
- APEX™ II
- APEX 20K
- ACEX 1K
- FLEX 10KA
- FLEX 10KE (except EPF10K100B devices)
- 3.3-V FLEX 6000
- MAX® 7000AE
- MAX 7000B
- MAX 3000A

The following features have been implemented in Altera devices to ease the hot-socketing process:

- Devices can be driven before power-up with no damage to the device.
- Devices do not drive out before or during power-up.
- Signal pins do not drive the V_{CCIO} or V_{CCINT} power supplies.

Devices Can Be Driven before Power-Up

Devices that do not support hot-socketing may be damaged if the pins are driven before the device is powered-up. For Altera devices that support hot-socketing, the device I/O pins, dedicated input pins, and dedicated clock pins can be driven before or during power-up without damaging the device.

Devices Do Not Drive Out before or during Power-Up

Devices that do not support hot-socketing may interrupt system operation or cause contention by driving out before or during power-up. In Altera devices that support hot-socketing, I/O pins are tri-stated before and during power-up and configuration, and will not drive out.

Signal Pins Cannot Drive the V_{CCIO} or V_{CCINT} Power Supply

Devices that do not support hot-socketing may be powered-up through their signal pins (when plugged into a live board) causing the power supplies to short-out. This irregular power-up can damage both the driving and driven devices and can disrupt card power-up.

For Altera devices that support hot-socketing, there is no current path from the I/O, dedicated input, or dedicated clock pins to the V_{CCIO} or V_{CCINT} pins before and during power-up; therefore, these devices cannot be powered-up through the I/O pins. Some Altera devices have weak pull-up resistors; these resistors are activated as the device is powered by the V_{CCIO} and V_{CCINT} pins. As a result, Altera devices that support hot-socketing may be inserted into (or removed from) a powered-up system board without damage or without interfering with the operation of the system board. During hot-socketing, these devices will not affect signal integrity of the back plane.

The DC operating conditions in each device data sheet specify the device input leakage current. For most devices, this leakage current is 10 μA . During hot-socketing, DC leakage current into an I/O pin may be higher. Table 2 shows this value for Altera devices that support hot-socketing.

Table 2. Hot-Socket DC Leakage Current for Altera Devices

Device	Condition	Max	Unit
ACEX 1K FLEX 10KA, FLEX 10KE, FLEX 6000 (3.3 V)	$V_{CC} = 0 \text{ V}$ $V_{IN} \leq 5.75 \text{ V}$ (1)	300 (2)	μA
MAX 7000AE, MAX 3000A	$V_{CC} = 0 \text{ V}$ $V_{IN} \leq 3.6 \text{ V}$ (3)	300 (2)	μA
	$V_{CC} = 0 \text{ V}$ $V_{IN} \leq 5.75 \text{ V}$ (1), (4)	300 (2)	μA
APEX 20K MAX 7000B	$V_{CC} = 0 \text{ V}$ $V_{IN} \leq 4.1 \text{ V}$ (5)	300 (2)	μA

Notes to Table 2:

- (1) These devices are 5.0-V tolerant.
- (2) Includes current from the weak pull-up resistors in the I/O cell.
- (3) The OE1 and GCLRn pins in MAX 7000AE and MAX 3000A devices may be driven up to 3.6 V during hot-socketing. After VCCINT and VCCIO reach the recommended operating conditions, these pins are 5.0-V tolerant.
- (4) All other pins in MAX 7000AE and MAX 3000A devices may be driven up to 5.75 V during hot-socketing.
- (5) These 2.5-V devices are 3.3-V tolerant.

A possible concern regarding hot-socketing is the potential for latch-up. Latch-up can occur when electrical subsystems are hot-socketed into an active system. During hot-socketing, the signal pins may be connected and driven by the active system before the power supply can provide current to the device's V_{CC} and ground planes. This condition can lead to latch-up and cause a low-impedance path from V_{CC} to ground within the device. As a result, the device expends a large amount of current, possibly causing electrical damage. All Altera devices are immune to latch-up when operated within device specifications, including hot-socketing.

Power-Up Sequence

Altera devices are designed to operate in multiple-voltage environments where it may be difficult to control power sequencing. Therefore, the devices are designed to accommodate any possible power-up sequence. The following sections address the power-up sequence for different voltage levels.

When V_{CCIO} and V_{CCINT} are supplied from different power sources to an Altera device, a delay between V_{CCIO} and V_{CCINT} may occur. Normal operation does not occur until both power supplies are in their recommended operating range.

When V_{CCINT} is powered-up, the IEEE Std. 1149.1 Joint Test Action Group (JTAG) circuitry is active. If TMS and TCK are connected to V_{CCIO} and V_{CCIO} is not powered-up, the JTAG signals are left floating. Thus, any transition on TCK can cause the state machine to transition to an unknown JTAG state, leading to incorrect operation when V_{CCIO} is finally powered-up. To disable the JTAG state during the power-up sequence, TCK should be pulled low to ensure that an inadvertent rising edge does not occur on TCK.



For more information, refer to *Application Note 100 (In-System Programmability Guidelines)*.

3.3-V, 2.5-V, or 1.8-V APEX, FLEX & MAX Devices

Because APEX 20K, ACEX 1K, FLEX 10KA, FLEX 10KE, MAX 7000B, 3.3-V FLEX 6000, MAX 7000AE, and MAX 3000A devices can be used in a multi-voltage environment, they are designed specifically to tolerate any possible power-up sequence (where appropriate). V_{CCINT} and V_{CCIO} can supply power in either sequence. 5.0-V, 3.3-V, 2.5-V, or 1.8-V input signals can drive these devices before V_{CCINT} or V_{CCIO} is applied without special precautions; the only exception is that the OE1 and nGCLR pins on MAX 7000AE and MAX 3000A devices must not exceed 3.6 V until V_{CCIO} and V_{CCINT} reach the recommended operating level. You can change the V_{CCIO} supply voltage from 3.3 V to 2.5 V or vice-versa while the board is powered-up. However, you must ensure that the V_{CCINT} and V_{CCIO} power supplies stay within the correct device operating conditions.

FLEX and configuration devices can power-up in either order, but you must ensure that the nSTATUS and CONF_DONE pull-up resistors are connected to the same voltage as the configuration device. This connection avoids driving signals into a configuration device that is not powered.

2.5-V and 1.8-V devices are the only Altera devices that can have a V_{CCIO} voltage level higher than the V_{CCINT} level.

5.0-V FLEX & MAX Devices

When V_{CCIO} powers-up, MAX devices can drive out without the core being powered-up. This power-up sequence does not damage MAX devices and their functionality is not affected, but it may interfere with the function of the system that contains MAX devices.

Because of possible interference with system functionality, Altera does not recommend driving 5.0-V MAX device input signals or relying on the output of the device before V_{CCINT} is powered-up.

FLEX and configuration devices can power-up in either order, but you must ensure that the `nSTATUS` and `CONF_DONE` pull-up resistors are connected to the same voltage as the configuration device. This connection avoids driving signals into a configuration device that is not powered.

Power-On Reset

The state of a system at power-up is an important consideration in designing a circuit. When power is applied to an Altera device, the POR event occurs only if V_{CC} reaches the recommended operating range within a certain period of time (specified as a maximum V_{CC} rise time). A POR event does not occur if these conditions are not met because slower rise times can cause incorrect device initialization and functional failure. The maximum V_{CC} rise time for FLEX 10K, FLEX 8000, and FLEX 6000 devices is 100 ms and should be monotonic (during V_{CC} rise time, the slope is zero or positive). For MAX devices, the maximum V_{CC} rise time is infinite as long as it is monotonic.

Altera's device registers are cleared or set (MAX 7000AE, MAX 7000B, and MAX 3000A devices) during power-on reset. If you are using the *NOT-Gate Push-Back* option in the Quartus™ and MAX+PLUS® II software, the registers power-up active-high. The *NOT-Gate Push-Back* option is an advanced logic synthesis option, which allows the compiler's logic synthesizer module to push an inversion (i.e., a NOT gate) back through a register and implement it on that register's D input.

Once the V_{CCINT} power supply reaches the specified operating range, it must remain at that range. If V_{CCINT} does not remain in the range, the operation is not guaranteed until V_{CCINT} re-enters the specified operating range.

APEX, ACEX & FLEX Devices

Before the V_{CC} supply reaches the recommended operating range, the I/O pins are tri-stated, with the exception of APEX 20K, ACEX 1K, and FLEX 10KE devices that have pull-up resistors at the I/O pins. During POR, the registers are cleared and the tri-state is released. Once the V_{CC} power supply reaches a stable and reliable operating voltage and after $\overline{nCONFIG}$ has gone high, the actual device configuration begins. During configuration, the I/O pins are tri-stated.

MAX Devices

Before the V_{CC} supply reaches the recommended operating range for MAX 7000AE, MAX 7000B, and MAX 3000A devices, the I/O pins are tri-stated. During POR, the registers are cleared or set. After POR, the tri-state is released and the I/O pins are in user mode and function as programmed (if the device has been previously programmed successfully).

For other MAX 7000—including MAX 7000E, MAX 7000S, and MAX 7000A—and MAX 9000 devices, the I/O pins are undefined until V_{CC} reaches the recommended operating range. During POR, the registers are cleared and the tri-state is released. After POR, the I/O pins are in user mode and function as programmed.



The power-up state of latches is undefined in all Altera devices except MAX 5000 devices. In MAX 5000 devices, latches power-up low.

During POR, the device configures I/O pins, clears device registers, and releases tri-states.

Conclusion

PCBs often contain a mix of 5.0-V, 3.3-V, 2.5-V, and 1.8-V devices. The MultiVolt interface enables the device core to run at a specific voltage (5.0 V, 3.3 V, 2.5 V, or 1.8 V), while keeping the I/O pins compatible with 5.0-V, 3.3-V, 2.5-V, or 1.8-V logic levels. Altera's MultiVolt interface allows you to incorporate newer generation devices with devices of varying voltage levels seamlessly. Altera has taken further steps by designing devices which allow V_{CCINT} and V_{CCIO} to power-up in either sequence and by incorporating support for hot-socketing.



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