

Introduction

High-speed serial data transmission has gained increasing popularity in the data communications industry. Because one serial channel can support the bandwidth of multiple conventional single-ended I/O standards, the number of I/O pins and board traces are substantially reduced. This trace reduction simplifies board design and minimizes parallel data bus skew.

The high-speed differential interface (HSDI) circuitry in Mercury™ devices allows designers to transmit high-bandwidth data using LVDS. The HSDI block is an embedded dedicated circuit for receiving and transmitting high-speed data streams between Mercury devices and high-speed interface devices. The HSDI block has two modes: source-synchronous mode and clock-data recovery (CDR) mode. This application note discusses the source-synchronous mode of the HSDI block.



For more information on the CDR mode of the HSDI block, refer to *AN 130: CDR in Mercury Devices*.

Source-synchronous mode includes the following features:

- 840 megabits per second (Mbps) on up to 18 input and 18 output dedicated HSDI channels
- Differential input and output clocks
- LVDS, LVPECL, and PCML I/O standard support
- Phase-locked loop (PLL) lock detection available internal and external to the device
- Flexible clocking schemes that allow the HSDI block to be used in a wide variety of applications
- Serializer/deserializer (SERDES) communicates to the logic array directly
- Compatible with the Altera® APEX® 20KE, National Semiconductor and Texas Instruments LVDS interfaces
- Supports 4-, 7- to 12-, 14-, 16- 18-, and 20-bit parallel internal data operating modes

Compatibility

The Mercury HSDI circuitry is compatible with the APEX 20KE LVDS interface and other industry-standard differential interfaces. Mercury devices enhance the specifications in source-synchronous mode with the addition of LVPECL, pseudo-current mode logic (PCML), and an increased number of channels, increasing total bandwidth.

The source-synchronous HSDI circuitry is compatible with the LVDS interface in APEX 20KE, National Semiconductor, and Texas Instruments devices. To be pipeline-compatible with other devices in the industry, the Mercury HSDI circuitry includes a two-cycle serial data latency at the SERDES circuitry. This means that the most significant bit (MSB) is the third data bit after the rising edge of the transmitted clock with the data.

Terminology

Because the HSDI block contains many new features, commonly used terminology is listed in [Table 1](#).

Term	Definition
HSDI	High-speed differential interface, a superset of the LVDS interface in APEX 20KE devices
LVDS	Low-voltage differential signaling, a differential I/O standard for high-speed serial data transmission specified by the EIA/TIA-644 specification
LVPECL	Low-voltage positive emitter coupled logic, a differential I/O standard
PCML	Pseudo-current mode logic
Source-synchronous mode	A mode of operation for the HSDI block to exchange serial data with non-CDR differential devices. This is compatible with the APEX 20KE device LVDS mode
Receiver	Receiver: differential input data channels
Transmitter	Transmitter: differential output data channels
HSDI_PLL1 HSDI_PLL2	High-frequency PLLs in the HSDI block. The transmitter uses HSDI_PLL1, and the receiver uses HSDI_PLL2
Serializer	The HSDI transmitter circuitry that converts the internal parallel data to serial data
Deserializer	The HSDI receiver circuitry that converts serial data to parallel data
<i>W</i>	Frequency multiplication factor for the HSDI PLL signals
<i>J</i>	Bus width of the parallel logic array data interfacing with the HSDI block
UI	Unit Interval, or one cycle of the serial data. The UI can be converted to seconds by using the following equation: Time = UI x period
Lock signal	Signal indicating whether the HSDI PLL signals (HSDI_PLL1, HSDI_PLL2) are locked to the input clock

LVDS, LVPECL & PCML I/O Standards

Mercury devices support LVDS, LVPECL, and PCML differential I/O standards (see [Table 2](#)). This section gives an overview and defines the electrical specifications for each standard.

Data Rate	I/O Standard		
	LVDS	LVPECL	PCML
≤ 840 Mbps	(1)	✓	✓

Note to [Table 2](#):

- (1) You can use the CDR circuit to achieve the 840-Mbps data rates for DC coupled LVDS applications. You must AC-couple the clock to a 2.2-V common mode voltage (V_{CM}) using the AC-coupling schemes in [AN 134: Using Programmable I/O Standards in Mercury Devices](#). The data channels should be DC-coupled. The byte alignment relative to the clock is lost when using the CDR circuit. Therefore, a byte-alignment circuit is required. Most Mercury source-synchronous designs already include byte-alignment logic because they usually use double-data rate (DDR) or single data rate (SDR) clocks. The CDR run length requirement is waived if the reference clock and the receiver data have the same source and have the same frequency.

LVDS

The LVDS I/O standard is a high-speed, low-voltage swing, low-power, and general-purpose I/O interface standard. This standard is process- and technology-independent and requires differential input but does not require an input reference voltage. Typical applications for LVDS are high-bandwidth data transfer, backplane driver, and clock distribution.

Two key industry standards support LVDS: the IEEE 1596.3 SCI-LVDS standard, and the ANSI/TIA/EIA-644 (American National Standards Institute/Telecommunications Industry Association/Electronic Industries Association) standard. The standards have similar features, but the IEEE standard supports only up to 250 MHz maximum clock input frequency. The ANSI/TIA/EIA-644 standard specifies a recommended maximum data rate of 655 Mbps and a theoretical maximum of 1.923 gigabits per second (Gbps). Mercury devices are designed to meet the ANSI/TIA/EIA-644 standard up to 840 Mbps. [Figure 1](#) shows the current-mode LVDS driver.

Figure 1. Current-Mode LVDS Driver

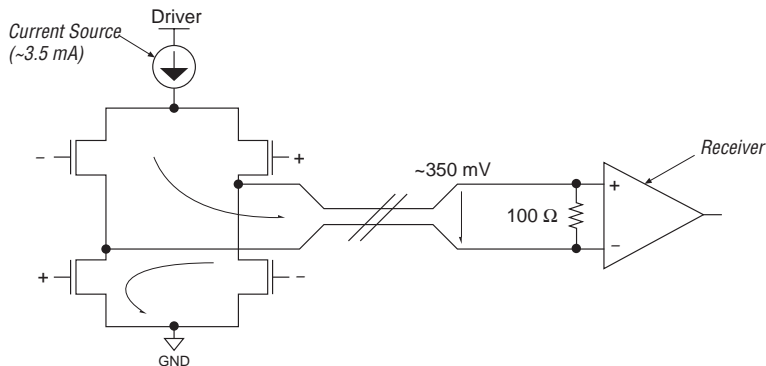


Table 3 shows the electrical specifications for the LVDS I/O standard.

Table 3. LVDS I/O Specifications						
Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{OD}	Differential output voltage	$R_L = 100 \Omega$	250	510	600	mV
ΔV_{OD}	Change in V_{OD} between high and low	$R_L = 100 \Omega$			50	mV
V_{OS}	Output offset voltage	$R_L = 100 \Omega$	1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between high and low	$R_L = 100 \Omega$			50	mV
V_{TH}	Differential input threshold		-100		100	mV
V_{IN}	Receiver input voltage range		0		2.4	V
R_L	Receiver differential input resistor		90	100	110	Ω

LVPECL

The LVPECL I/O standard is used for video graphic, telecommunications, data communication, and clock distribution applications. LVPECL has a larger differential output voltage swing than LVDS. [Table 4](#) shows the LVPECL specifications.

Table 4. LVPECL Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{IL}	Low-level input voltage		0		2,000	mV
V_{IH}	High-level input voltage		400		2,470	mV
V_{OL}	Low-level output voltage		1,400		1,650	mV
V_{OH}	High-level output voltage		2,275		2,470	mV
V_{ID}	Differential input voltage		400	600	1,200	mV
V_{OD}	Differential output voltage		525	1,050	1,200	mV
t_R	Rise time (20 to 80%)		85		325	ps
t_F	Fall time (20 to 80%)		85		325	ps
t_{DSKEW}	Differential skew				25	ps
R_L	Receiver differential input internal resistor			100		Ω

PCML

The PCML I/O standard is a high-speed differential I/O standard that can be used for telecommunications applications. Several companies consider PCML as the best I/O standard to use with their protocols. PCML is suitable for data communication across backplanes and cables. [Table 5](#) shows the PCML I/O standard specifications

Table 5. PCML Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465
V_{IL}	Low-level input voltage				$V_{CCIO} - 0.4$
V_{IH}	High-level input voltage		V_{CCIO}		
V_{OL}	Low-level output voltage				$V_{CCIO} - 0.4$
V_{OH}	High-level output voltage		V_{CCIO}		
V_T	Output termination voltage			V_{CCIO}	
V_{ID}	Differential input voltage		400		800
V_{OD}	Differential output voltage		400	700	800
t_R	Rise time (20 to 80%)				200
t_F	Fall time (20 to 80%)				200
t_{DSKEW}	Differential skew				25
R_1	Output load		90	100	110
R_2	Receiver differential input resistor		45	50	55

HSDI Architecture

The HSDI architecture is dedicated circuitry that contains up to 18 receiver and 18 transmitter channels and two high-performance PLLs.

- HSDI dedicated circuitry is located in the top-most I/O band
- EP1M120 devices contain eight receiver channels and eight transmitter channels
- EP1M350 devices contain 18 receiver channels, 18 transmitter channels, and 100 Flexible-LVDS™ channels
- HSDI_PLL1 and HSDI_PLL2 are located at the center of the HSDI block

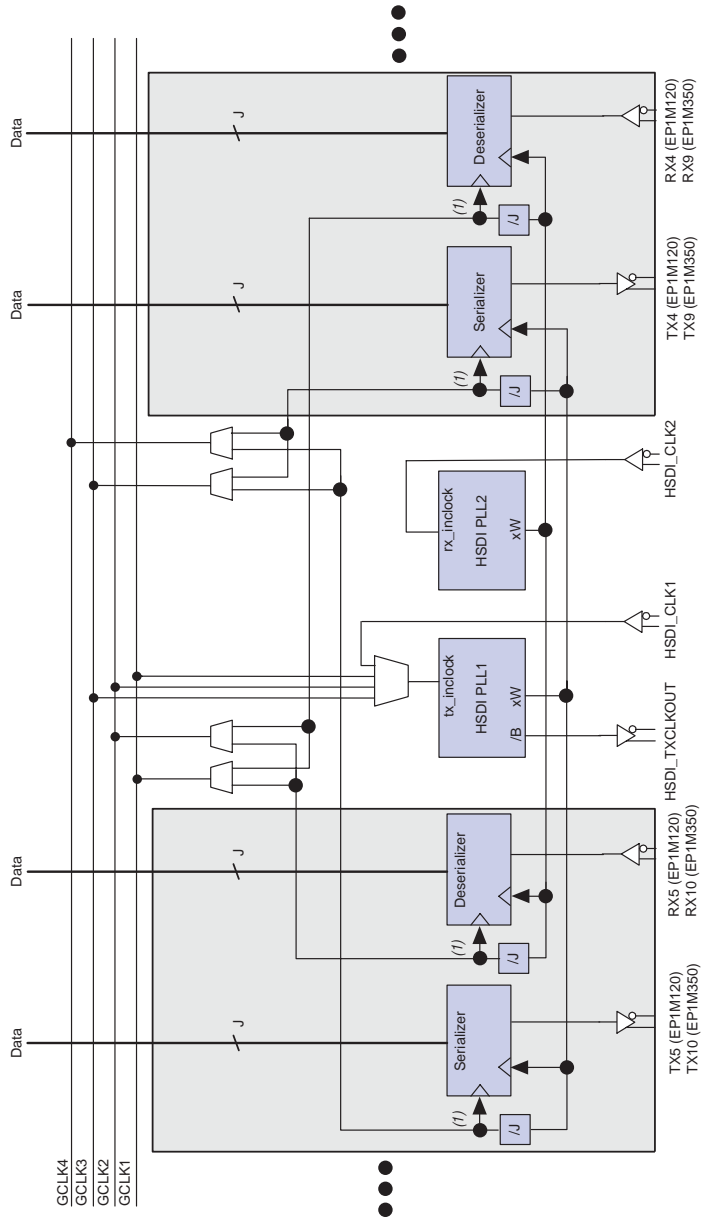
Table 6 shows the Mercury device density and number of HSDI channels.

Table 6. Number of HSDI Channels Available in Mercury Devices

Device	Density (LEs)	Number of HSDI Channels
EP1M120	4,800	8
EP1M350	14,400	18

The source-synchronous HSDI architecture is shown in [Figure 2](#).

Figure 2. HSDI Block Diagram



Note to Figure 2:

- (1) The J clock dividers for the two center channels adjacent to the HSDI PLLs (channels 4 and 5 for EP1M120 devices and channels 9 and 10 for EP1M350 devices) can drive the Mercury device global clocks. Be sure to use the center channels for the transmitter and receiver circuitry to allow access to global clock links.

Source-Synchronous Mode

The source-synchronous mode is used for exchanging high-speed serial data between Mercury devices and other devices that are not equipped with CDR capability. The clock is sent with transmitted data from one device to the next.

In source-synchronous mode, interfacing is supported at up to 840 Mbps. Serial channels are transmitted and received along with a low-speed clock. The device receiving the data then multiplies the clock by a multiplication factor (W), which can be a value of 1 to 12, 14, 16, 18, or 20. The serialization/deserialization rate (J) can be any number from 4, 7, 8, 9 to 12, 14, 16, 18, or 20, and does not have to equal the clock multiplication value. For example, an 840-Mbps LVDS channel can be received along with a 84-MHz clock. In this example, the HSDI_PLL2 multiplies the input clock by 10 to generate the 840-MHz clock internally, which clocks the serial shift register. For more detail, see “HSDI Receiver (Deserializer)” on page 9 and “HSDI Transmitter (Serializer)” on page 11.

Below is a list of rules and guidelines for using source-synchronous mode in Mercury devices:

- PLL reference clocks are mandatory and cannot be interrupted.
- All receiver and HSDI_CLK2 pins must be assigned to use the same I/O standard. All transmitter pins, HSDI_CLK1, and HSDI_TXCLKOUT must be assigned to use the same I/O standard.
- When any of differential receiver and transmitter buffers are used by the HSDI circuitry, the other I/O pins in that I/O band cannot be used for other standards.
- All receiver channels are clocked by HSDI_PLL2.
- All transmitter channels are clocked by HSDI_PLL1.
- HSDI_PLL2 is always driven by HSDI_CLK2 only.
- HSDI_CLK1 or a global clock can drive HSDI_PLL1. However, typical operation is to have HSDI_PLL1 driven by a global clock.
- HSDI was designed with no SERDES bypass to allow for higher performance; ($J = 1$) mode is not supported.
- 622.08-Mbps data with 622.08-MHz clock ($W = 1$) with parallel interface to logic array is supported.
- High-speed PLLs have no user-controlled phase delays.
- HSDI_TXCLKOUT is driven by the output of the B divider from HSDI_PLL1. B can be set to 1 to 12, 14, 16, 18, or 20.

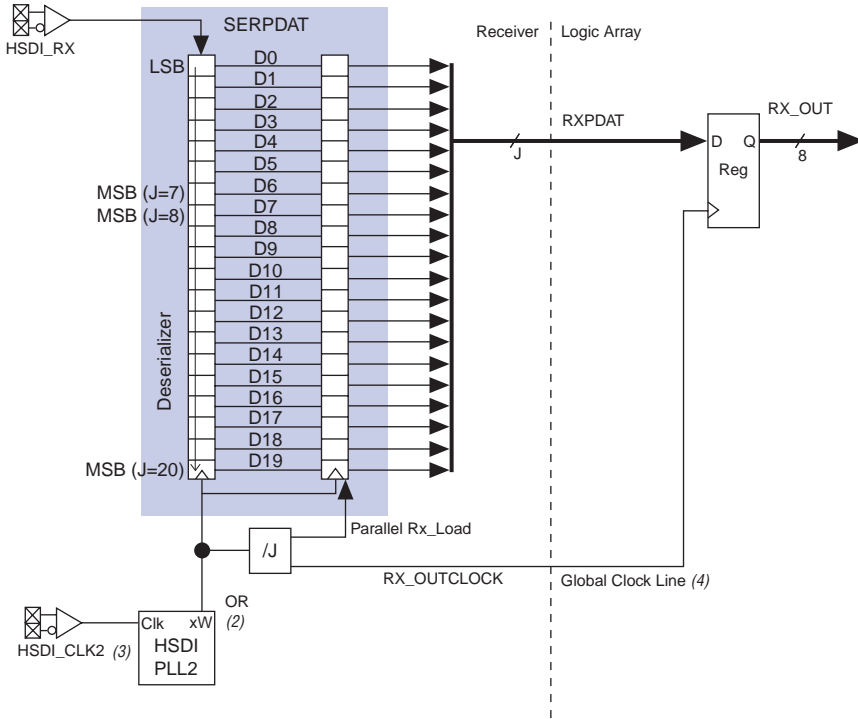
- Unlike the APEX 20KE device, the HSDI_TXCLKOUT duty cycle is not designed for 50% if W and J are equal and odd (e.g., 7). Therefore, the 40 to 60% output duty cycle does not include odd values of W and J .
- Design with one of the center channels for both the transmitter and receiver.

HSDI Receiver (Deserializer)

At the receiver (HSDI_RX), high-speed serial data enters the Mercury device through the serial channels. At the same time, HSDI_CLK2 feeds HSDI_PLL2, which is associated with the receiver channels. The serial data is converted to parallel data at the deserializer, which has to be driven by a clock at the same phase and frequency as the serial data. HSDI_PLL2 generates the internal clock that is used for synchronization by the deserializer.

The deserializer generates J -bit wide parallel data from the serial data. The parallel data is then driven into row or column-interconnect lines that feed logic. [Figure 3](#) shows the deserializer circuitry for a single receiver channel.

Figure 3. Deserializer Circuitry Notes (1), (2)

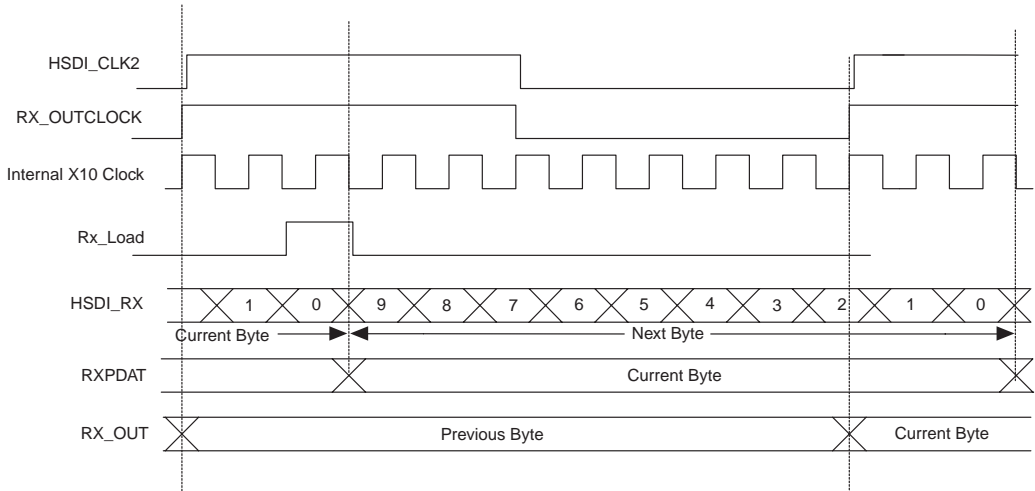


Notes to Figure 3:

- (1) EP1M350 devices have 18 individual receiver channels. EP1M120 devices have eight individual receiver channels.
- (2) $W = 1$ to 12, 14, 16, 18, or 20. W does not have to equal J .
- (3) This clock pin drives an HSDI PLL only.
- (4) The J clock dividers for the two center channels adjacent to the HSDI PLLs (channels 4 and 5 for EP1M120 devices and channels 9 and 10 for EP1M350 devices) can drive the Mercury device global clocks. Be sure to use the center channels for the transmitter and receiver circuitry to allow access to global clock links.

The receiver timing diagram for 1-to-10 serial-to-parallel conversion is shown in Figure 4. To be compatible with the APEX 20KE LVDS interface, a two-cycle serial data latency is present at the serializer and a 2.5 cycle latency at the deserializer.

Figure 4. Receiver Timing Waveform



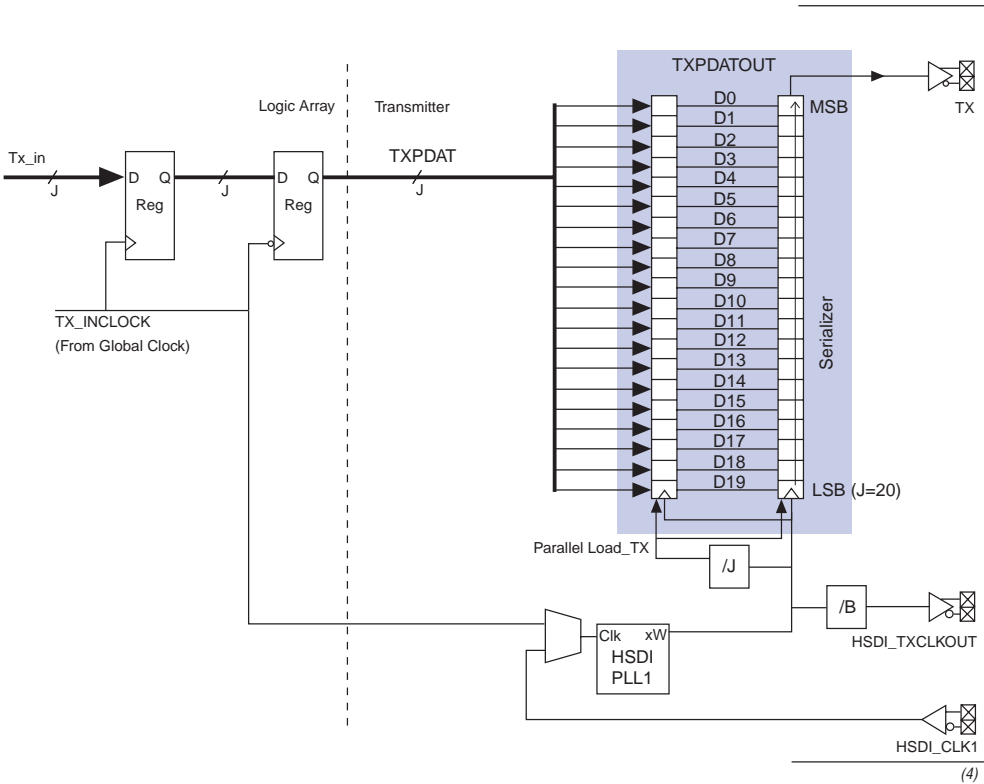
HSDI Transmitter (Serializer)

At the transmitter, parallel data is converted into high-speed serial data by the serializer and then transmitted off-chip through the transmitter data channels (HSDI_TX). HSDI_PLL1 generates the clocks for the serializer and compensates the delay mismatch of two different paths—transmitter data (HSDI_TX) and transmitter output clock (HSDI_TXCLKOUT)—such that the HSDI_TX and HSDI_TXCLKOUT are in-phase. HSDI_CLK1 or three of the four global clocks can drive HSDI_PLL1.

Unlike general purpose PLLs, HSDI_PLL1 and HSDI_PLL2 do not compensate for the global clock tree delay. Therefore, the outputs of HSDI_PLL1 and HSDI_PLL2 and the global clock may not be in-phase. Similar to the APEX 20KE device, the HSDI to logic array synchronization in source-synchronous mode is guaranteed by logic element (LE) placement. You can place LEs in the top three rows of the device. The Quartus® II software places logic in the top row by default. If there are fitting problems, the software may use the second or third row.

Figure 5 shows the serializer circuitry for a single transmitter channel.

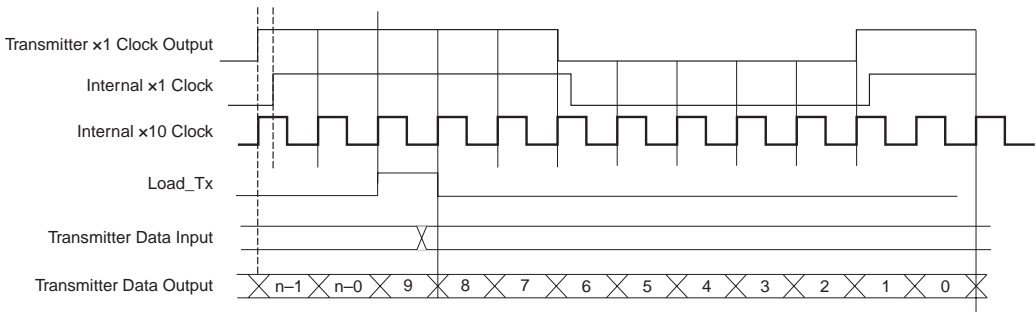
Figure 5. Serializer Circuitry Notes (1), (2), (3)



Notes to Figure 5:

- (1) EP1M350 devices have 18 individual transmitter channels. EP1M120 devices have eight individual transmitter channels.
- (2) $W = 1$ to 12, 14, 16, 18, or 20.
 $B = 1$ to 12, 14, 16, 18, or 20.
 $J = 4, 7$ to 12, 14, 16, 18, or 20.
- (3) The J clock dividers for the two center channels adjacent to the HSDI PLLs (channels 4 and 5 for EP1M120 devices and channels 9 and 10 for EP1M350 devices) can drive the Mercury device global clocks. Be sure to use the center channels for the transmitter and receiver circuitry to allow access to global clock links.
- (4) This clock pin drives the HSDI PLL only.

Figure 6 shows the transmitter timing waveform.

Figure 6. Transmitter Timing Waveform ($J = 10$)

Source-Synchronous Mode HSDI Timing Budget

This section discusses the timing budget, waveforms, and specifications for the source-synchronous mode high-speed signaling in Mercury devices.

LVDS, LVPECL, and PCML allow data to be transmitted at very high speeds, resulting in better overall system performance. To take advantage of fast system performance, designers must understand how to analyze timing for these high-speed signals. Timing analysis for the HSDI block is different from traditional synchronous timing analysis techniques. Rather than focusing on clock-to-output and setup times, source-synchronous mode HSDI timing analysis is based on the skew between the data and the clock signals.

High-speed differential data transmission requires designers to use these timing parameters provided by Altera and other vendors. Designers must consider board skew, cable skew, and clock jitter. This section defines the source-synchronous mode differential timing parameters for Mercury devices, and it explains how to use these timing parameters to determine a design's maximum performance.

Timing Definition

Timing specifications are used to describe the high-speed modules (see [Table 7](#)). High-speed I/O timing requirements are defined in [Table 8](#)

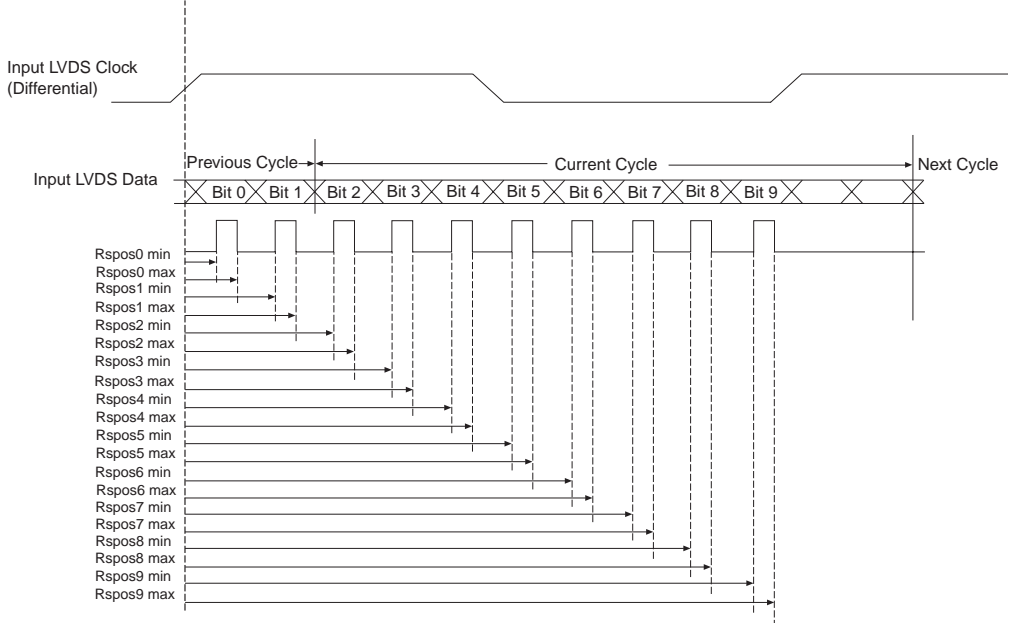
LVDS Timing Specification	Terminology
t_C	LVDS receiver/transmitter input and output clock period.
$f_{LVDSCLK}$	LVDS receiver/transmitter input and output clock frequency.
Time unit interval (TUI)	The TUI is the data-bit timing budget allowed for skew, propagation delays, and data sampling window. (TUI = $1/(\text{receiver input clock frequency} \times \text{multiplication factor}) = t_C/W$).
f_{LVDSDR}	Maximum LVDS data transfer rate ($f_{LVDSDR} = 1/\text{TUI}$).
Channel-to-channel skew (TCCS)	TCCS is the timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement.
Sampling window (SW)	This parameter defines the period of time during which the data must be valid in order to be correctly captured. The setup and hold times determine the ideal strobe position within the sampling window.
Input jitter (peak-to-peak)	Peak-to-peak input jitter on LVDS PLLs.
Output jitter (RMS)	RMS output jitter on LVDS PLLs.
f_{LOCK}	Lock time for LVDS transmitter and receiver PLLs.

Symbol	Conditions	Commercial			Unit
		-5, -6, -7 Speed Grade			
		Min	Typ	Max	
$f_{LVDSCLK}$	$W = 8$	37.5		105	MHz
	$W = 7$	42.9		120	MHz
	$W = 4$	75		210	MHz
Device operation	$J = 8$	300		840	Mbps
	$J = 7$	300		840	Mbps
	$J = 4$	300		840	Mbps
TCCS	All			300	ps
SW	All			200	ps
Input jitter (peak-to-peak)	All			2.1% of t_C	UI
Output jitter (RMS)	All			0.35% of t_C	UI
Duty cycle	All	45		55	%
f_{LOCK}	All			10	us

Input Timing

The functional descriptions for serialization and deserialization are described in previous sections of this application note. [Figure 7](#) illustrates the essential operation and the timing relationship between the input clock and serial input data.

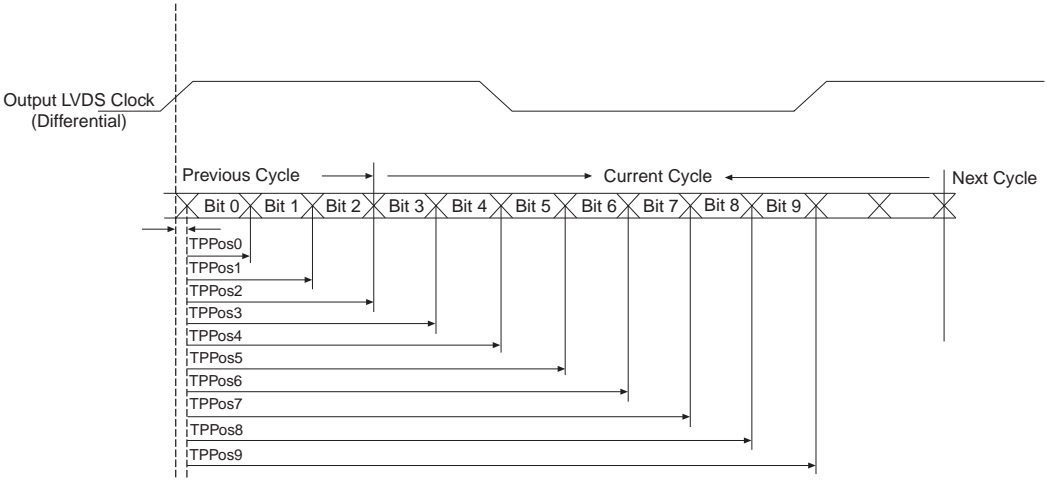
Figure 7. Input Timing Waveform



Output Timing

The output timing waveform in [Figure 8](#) illustrates the relationship between the output LVDS clock and the serial output data stream.

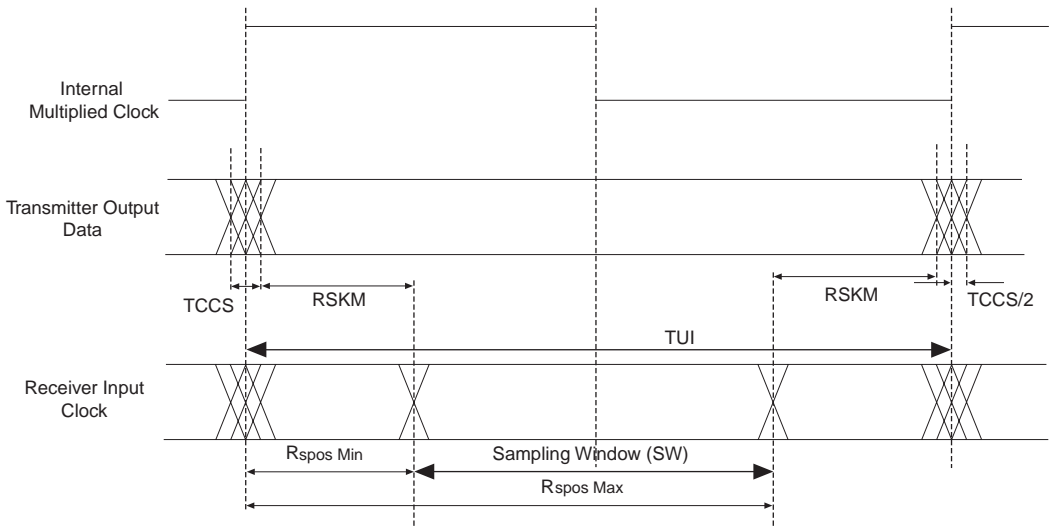
Figure 8. Output Timing Waveform



LVDS Timing Budget

Changes in a system’s environment, such as temperature, inter-symbol interference by the media [e.g., cable, connector, or printed circuit board (PCB)], or the receiver’s inherent setup, hold, and internal skew, all collaborate to reduce the margin in the design. The timing margin between a receiver’s clock input and data input sampling window is known as RSKM. Figure 9 shows the timing budget of an LVDS data bit period.

Figure 9. LVDS Timing Budget



RSKM is defined by the total margin left after accounting for the SW and TCCS. The RSKM equation is shown below:

$$\text{RSKM} = (\text{TUI} - \text{SW} - \text{TCCS}) / 2$$

The RSKM parameter is large enough to allow for clock jitter and cable and board skew, and to provide extra margin for designs. To meet a system's requirements, designers must ensure that jitter and system skew cannot exceed RSKM. The equation for an application's margin is shown below:

$$\text{Margin} = \text{RSKM} - (\text{input clock jitter} + \text{system skew})$$

System skew is the difference in propagation delays of signals between devices. It includes skew introduced from cables, connectors, and differences in signal lengths on PCB traces. The input clock jitter is the jitter on the transmit clock that will be received by the Mercury LVDS PLL.

Sample Calculation

For this example, the system clock is running at 77.76 MHz, RSKM = 400 ps, media skew is 100 ps, and jitter introduced is 91 ps. Margin is calculated using the following formula:

$$\text{Margin} = \text{RSKM} - (\text{input clock jitter} + \text{system skew}) = 400 - (100 + 91) = 209 \text{ ps.}$$

Switching Characteristics

This section shows the timing specifications that are applied when receiving or transmitting data at various speeds. Timing specifications for other frequencies or SERDES factors are easily constructed.

Receiver Timing Specification

Tables 9 through 12 show the required time that data is stable at the receiver input pins. Data is required to be stable from R_{sposn} (minimum) to R_{sposn} (maximum).



For more information on LVDS transmitter switching characteristics, see the bit positions calculator on the Altera web site at www.altera.com.

Specifications are for $f_{IN} = 66 \text{ MHz}$, de-multiplexer ratio of 7, data rate = 462 Mbps

Symbol	Parameter	Min	Typ	Max	Unit
R_{spos0}	Receiver input strobe position for bit 0	0.73	1.08	1.43	ns
R_{spos1}	Receiver input strobe position for bit 1	2.90	3.25	3.60	ns
R_{spos2}	Receiver input strobe position for bit 2	5.06	5.41	5.76	ns
R_{spos3}	Receiver input strobe position for bit 3	7.23	7.58	7.93	ns
R_{spos4}	Receiver input strobe position for bit 4	9.39	9.74	10.09	ns
R_{spos5}	Receiver input strobe position for bit 5	11.55	11.90	12.25	ns
R_{spos6}	Receiver input strobe position for bit 6	13.72	14.07	14.42	ns

Specifications are for $f_{IN} = 77.76$ MHz, de-multiplexer ratio of 8, data rate = 622.08 Mbps.

Table 10. LVDS Receiver Switching Characteristics for 1 to 8 Mode

Symbol	Parameter	Min	Typ	Max	Unit
Rspos0	Receiver input strobe position for bit 0	0.50	0.80	1.10	ns
Rspos1	Receiver input strobe position for bit 1	2.11	2.41	2.71	ns
Rspos2	Receiver input strobe position for bit 2	3.72	4.02	4.32	ns
Rspos3	Receiver input strobe position for bit 3	5.33	5.63	5.93	ns
Rspos4	Receiver input strobe position for bit 4	6.93	7.23	7.53	ns
Rspos5	Receiver input strobe position for bit 5	8.54	8.84	9.14	ns
Rspos6	Receiver input strobe position for bit 6	10.15	10.45	10.75	ns
Rspos7	Receiver input strobe position for bit 7	11.76	12.06	12.36	ns

Specifications are for $f_{IN} = 100$ MHz, de-multiplexer ratio of 10, data rate = 840 Mbps.

Table 11. LVDS Receiver Switching Characteristics for 1 to 10 Mode

Symbol	Parameter	Min	Typ	Max	Unit
Rspos0	Receiver input strobe position for bit 0	0.38	0.60	0.82	ns
Rspos1	Receiver input strobe position for bit 1	1.57	1.79	2.01	ns
Rspos2	Receiver input strobe position for bit 2	2.76	2.98	3.20	ns
Rspos3	Receiver input strobe position for bit 3	3.95	4.17	4.39	ns
Rspos4	Receiver input strobe position for bit 4	5.14	5.36	5.58	ns
Rspos5	Receiver input strobe position for bit 5	6.33	6.55	6.77	ns
Rspos6	Receiver input strobe position for bit 6	7.52	7.74	7.96	ns
Rspos7	Receiver input strobe position for bit 7	8.71	8.93	9.15	ns
Rspos8	Receiver input strobe position for bit 8	9.90	10.12	10.34	ns
Rspos9	Receiver input strobe position for bit 9	11.09	11.31	11.53	ns

Specifications are for $f_{IN} = 50$ MHz, de-multiplexer ratio of 20, data rate = 840 Mbps.

Table 12. LVDS Receiver Switching Characteristics for 1 to 20 Mode

Symbol	Parameter	Min	Typ	Max	Unit
Rsp0s0	Receiver input strobe position for bit 0	0.38	0.60	0.82	ns
Rsp0s1	Receiver input strobe position for bit 1	1.57	1.79	2.01	ns
Rsp0s2	Receiver input strobe position for bit 2	2.76	2.98	3.20	ns
Rsp0s3	Receiver input strobe position for bit 3	3.95	4.17	4.39	ns
Rsp0s4	Receiver input strobe position for bit 4	5.14	5.36	5.58	ns
Rsp0s5	Receiver input strobe position for bit 5	6.33	6.55	6.77	ns
Rsp0s6	Receiver input strobe position for bit 6	7.52	7.74	7.96	ns
Rsp0s7	Receiver input strobe position for bit 7	8.71	8.93	9.15	ns
Rsp0s8	Receiver input strobe position for bit 8	9.90	10.12	10.34	ns
Rsp0s9	Receiver input strobe position for bit 9	11.09	11.31	11.53	ns
Rsp0s10	Receiver input strobe position for bit 10	12.28	12.50	12.72	ns
Rsp0s11	Receiver input strobe position for bit 11	13.47	13.69	13.91	ns
Rsp0s12	Receiver input strobe position for bit 12	14.66	14.88	15.10	ns
Rsp0s13	Receiver input strobe position for bit 13	15.85	16.07	16.29	ns
Rsp0s14	Receiver input strobe position for bit 14	17.04	17.26	17.48	ns
Rsp0s15	Receiver input strobe position for bit 15	18.23	18.45	18.67	ns
Rsp0s16	Receiver input strobe position for bit 16	19.42	19.64	19.86	ns
Rsp0s17	Receiver input strobe position for bit 17	20.61	20.83	21.05	ns
Rsp0s18	Receiver input strobe position for bit 18	21.80	22.02	22.24	ns
Rsp0s19	Receiver input strobe position for bit 19	22.99	23.21	23.43	ns

Transmitter Timing Specification

Tables 13 through 16 show the required time the transmitter data will be stable. The transmitter data will be stable from TPP_{0sn} (maximum) to $TPP_{0sn} + 1$ (minimum).

Specifications are for $f_{IN} = 66$ MHz, multiplexer ratio of 7, data rate = 462 Mbps.

Table 13. LVDS Transmitter Switching Characteristics for 7 to 1 Mode

Symbol	Parameter	Min	Typ	Max	Unit
TPPos0	Receiver input strobe position for bit 0	-0.20	0.00	0.20	ns
TPPos1	Receiver input strobe position for bit 1	1.96	2.16	2.36	ns
TPPos2	Receiver input strobe position for bit 2	4.13	4.33	4.53	ns
TPPos3	Receiver input strobe position for bit 3	6.29	6.49	6.69	ns
TPPos4	Receiver input strobe position for bit 4	8.46	8.66	8.86	ns
TPPos5	Receiver input strobe position for bit 5	10.62	10.82	11.02	ns
TPPos6	Receiver input strobe position for bit 6	12.79	12.99	13.19	ns

Specifications are for $f_{IN} = 77.76$ MHz, multiplexer ratio of 8, data rate = 622.08 Mbps.

Table 14. LVDS Transmitter Switching Characteristics for 8 to 1 Mode

Symbol	Parameter	Min	Typ	Max	Unit
TPPos0	Receiver input strobe position for bit 0	-0.20	0.00	0.20	ns
TPPos1	Receiver input strobe position for bit 1	1.41	1.61	1.81	ns
TPPos2	Receiver input strobe position for bit 2	3.02	3.22	3.42	ns
TPPos3	Receiver input strobe position for bit 3	4.62	4.82	5.02	ns
TPPos4	Receiver input strobe position for bit 4	6.23	6.43	6.63	ns
TPPos5	Receiver input strobe position for bit 5	7.84	8.04	8.24	ns
TPPos6	Receiver input strobe position for bit 6	9.45	9.65	9.85	ns
TPPos7	Receiver input strobe position for bit 7	11.05	11.25	11.45	ns

Specifications are for $f_{IN} = 100$ MHz, de-multiplexer ratio of 10, data rate = 840 Mbps.

Table 15. LVDS Transmitter Switching Characteristics for 10 to 1 Mode (Part 1 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
TPPos0	Receiver input strobe position for bit 0	-0.20	0.00	0.20	ns
TPPos1	Receiver input strobe position for bit 1	0.99	1.19	1.39	ns
TPPos2	Receiver input strobe position for bit 2	2.18	2.38	2.58	ns
TPPos3	Receiver input strobe position for bit 3	3.37	3.57	3.77	ns

Table 15. LVDS Transmitter Switching Characteristics for 10 to 1 Mode (Part 2 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
TPPos4	Receiver input strobe position for bit 4	4.56	4.76	4.96	ns
TPPos5	Receiver input strobe position for bit 5	5.75	5.95	6.15	ns
TPPos6	Receiver input strobe position for bit 6	6.94	7.14	7.34	ns
TPPos7	Receiver input strobe position for bit 7	8.13	8.33	8.53	ns
TPPos8	Receiver input strobe position for bit 8	9.32	9.52	9.72	ns
TPPos9	Receiver input strobe position for bit 9	10.51	10.71	10.91	ns

Specifications are for $f_{IN} = 50$ MHz, de-multiplexer ratio of 20, data rate = 840 Mbps.

Table 16. LVDS Transmitter Switching Characteristics for 20 to 1 Mode

Symbol	Parameter	Min	Typ	Max	Unit
TPPos0	Receiver input strobe position for bit 0	-0.20	0.00	0.20	ns
TPPos1	Receiver input strobe position for bit 1	0.99	1.19	1.39	ns
TPPos2	Receiver input strobe position for bit 2	2.18	2.38	2.58	ns
TPPos3	Receiver input strobe position for bit 3	3.37	3.57	3.77	ns
TPPos4	Receiver input strobe position for bit 4	4.56	4.76	4.96	ns
TPPos5	Receiver input strobe position for bit 5	5.75	5.95	6.15	ns
TPPos6	Receiver input strobe position for bit 6	6.94	7.14	7.34	ns
TPPos7	Receiver input strobe position for bit 7	8.13	8.33	8.53	ns
TPPos8	Receiver input strobe position for bit 8	9.32	9.52	9.72	ns
TPPos9	Receiver input strobe position for bit 9	10.51	10.71	10.91	ns
TPPos10	Receiver input strobe position for bit 10	11.70	11.90	12.10	ns
TPPos11	Receiver input strobe position for bit 11	12.90	13.10	13.30	ns
TPPos12	Receiver input strobe position for bit 12	14.09	14.29	14.49	ns
TPPos13	Receiver input strobe position for bit 13	15.28	15.48	15.68	ns
TPPos14	Receiver input strobe position for bit 14	16.47	16.67	16.87	ns
TPPos15	Receiver input strobe position for bit 15	17.66	17.86	18.06	ns
TPPos16	Receiver input strobe position for bit 16	18.85	19.05	19.25	ns
TPPos17	Receiver input strobe position for bit 17	20.04	20.24	20.44	ns
TPPos18	Receiver input strobe position for bit 18	21.23	21.43	21.63	ns
TPPos19	Receiver input strobe position for bit 19	22.42	22.62	22.82	ns

Flexible-LVDS Interface

In addition to 18 channels of high-speed I/O circuitry at 840 Mbps each, the Mercury EP1M350 device offers 100 additional channels that, in conjunction with internal PLLs, can transmit or receive DDR data at 400 Mbps. Flexible-LVDS pins are located in the bottom three I/O bands. The Flexible-LVDS pins have true differential input and output LVDS, LVPECL, and PCML buffers and do not require any external components except for 100 Ω termination resistors on receiver channels. These pins do not contain dedicated SERDES circuitry. Therefore, internal logic is used to perform SERDES functions.

For the EP1M120 and EP1M350 devices, the SERDES cannot be bypassed on the high-speed (HSDI_TX and HSDI_RX) pins. The Flexible-LVDS pins on the EP1M350 device should be used for these applications.

Flexible-LVDS Interface Implementation

Utilizing shift registers, internal global PLLs, and I/O cells, data is converted from serial to parallel, or parallel to serial, and received or transmitted. Figures 10 and 11 show block diagrams of the Flexible-LVDS receiver and transmitter interfaces.

Figure 10. Flexible-LVDS Receiver Interface

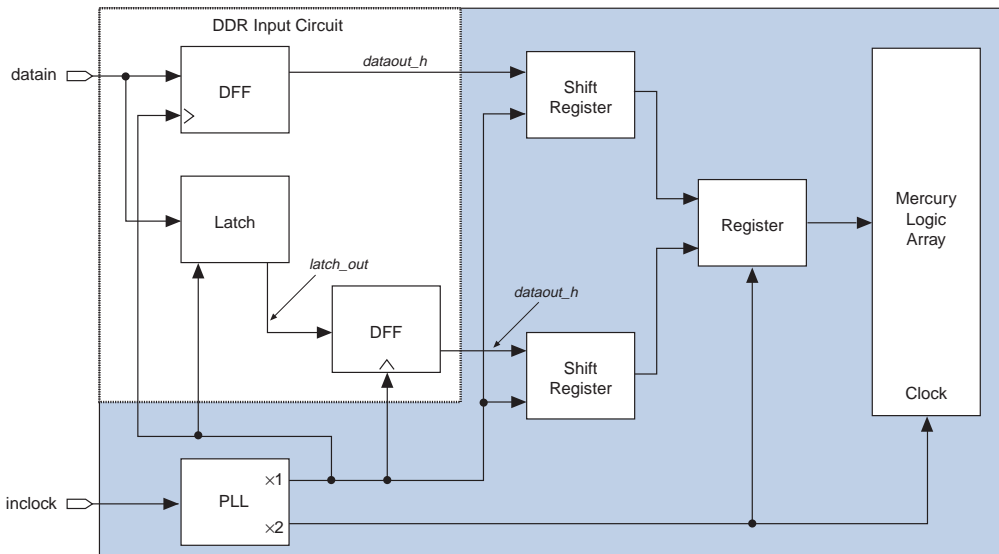
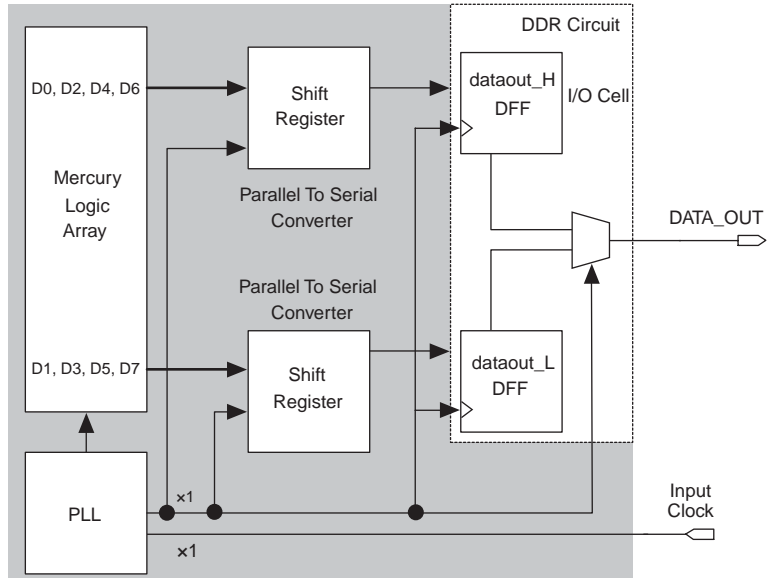


Figure 11. Flexible-LVDS Transmitter Interface



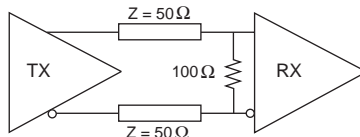
Board Termination Schemes

This section defines the termination schemes for LVDS, LVPECL, and PCML.

LVDS

LVDS buffers send 3.5-mA (typically) through a 100 Ω termination, which matches the trace impedance. The termination should be located as close to the receiver input as possible. Figure 12 shows the termination scheme used for LVDS. The 100 Ω termination can be programmed internally.

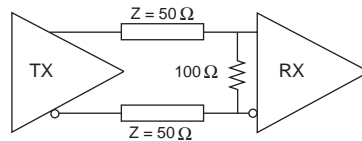
Figure 12. LVDS Termination Scheme



LVPECL

LVPECL can be used to communicate between multiple Mercury devices on a board or between Mercury devices and other devices on the board that support the LVPECL standard. Figure 13 shows the termination scheme for LVPECL. The $100\ \Omega$ termination can be programmed internally.

Figure 13. LVPECL Termination Scheme

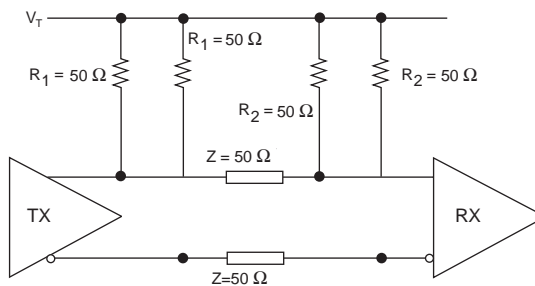


For non-Mercury transmitters with DC coupling, the LVPECL termination schemes suggested by the chip vendor should be used.

PCML

PCML uses two parallel $50\ \Omega$ termination resistors at the transmitter and two $50\ \Omega$ parallel termination resistors at the receiver. The termination voltage V_T is the same as the V_{CCIO} voltage ($3.3\ \text{V}$). See Figure 14.

Figure 14. PCML I/O Board Termination Scheme



Board Design Considerations

This section will help you maximize performance from the Mercury high-speed I/O module and ensure first-time success in implementing a functional design with optimal signal quality. This information should be used in conjunction with the device data sheet, pin table, and [AN 224: High-Speed Board Layout Guidelines](#). Designers should have a basic knowledge of high-speed PCB layout techniques. The critical issues of controlled impedance of traces and connectors, differential routing, and termination techniques must all be considered to get the best performance from a device.

When used in source-synchronous mode, the Mercury high-speed module generates signals that travel over the media at frequencies as high as 840 Mbps, and have a rise/fall time of approximately 200 ps.

Board design should be based on controlled differential impedance. All parameters such as trace width, trace thickness, and distance between two differential traces should be calculated and compared.

Longer traces have more inductance and capacitance. Shorter traces should be used to prevent signal integrity problems.

The following list offers some general board design guidelines:

- Place the termination resistors as close to the receiver input pins as possible.
- Use surface mount components.
- Avoid 90 degree or 45 degree corners.
- Use high-performance connectors, such as HS-3 connectors, for backplane designs. High-performance connectors are provided by third-party vendors such as Teradyne Corp and Tyco Electronics.
- Design backplane and card traces such that the trace impedance matches the connector's and/or the termination's impedance.
- Use common geometric (width and thickness) values for differential pair traces.
- Keep an equal number of vias for both signal traces.
- Keep the trace lengths between two traces equal to avoid possible skew between the two signals, which will result in misplaced crossing points.
- Vias cause discontinuities, so limit them as much as possible.
- Use 0.001-, 0.01-, and 0.1- μ F bypass capacitor values between the HSDI power and ground planes.
- To avoid possible noise coupling, keep high-speed transistor-to-transistor logic (TTL) signals away from differential signals.
- Do not route TTL clock signals on areas under or above the differential signals unless shielded by a power or GND plane.

Software Support

In Mercury devices, the source-synchronous LVDS mode is implemented using the `altlvds` megafunction available with the Quartus II software. The Quartus II Help documents how to use this megafunction.

Applications

The flexibility of the source-synchronous mode allows it to support many different applications. A few of these applications are described in this section.

- RapidIO™ support
- POS-PHY Level IV
- Source synchronous LVDS with ×1 clocking

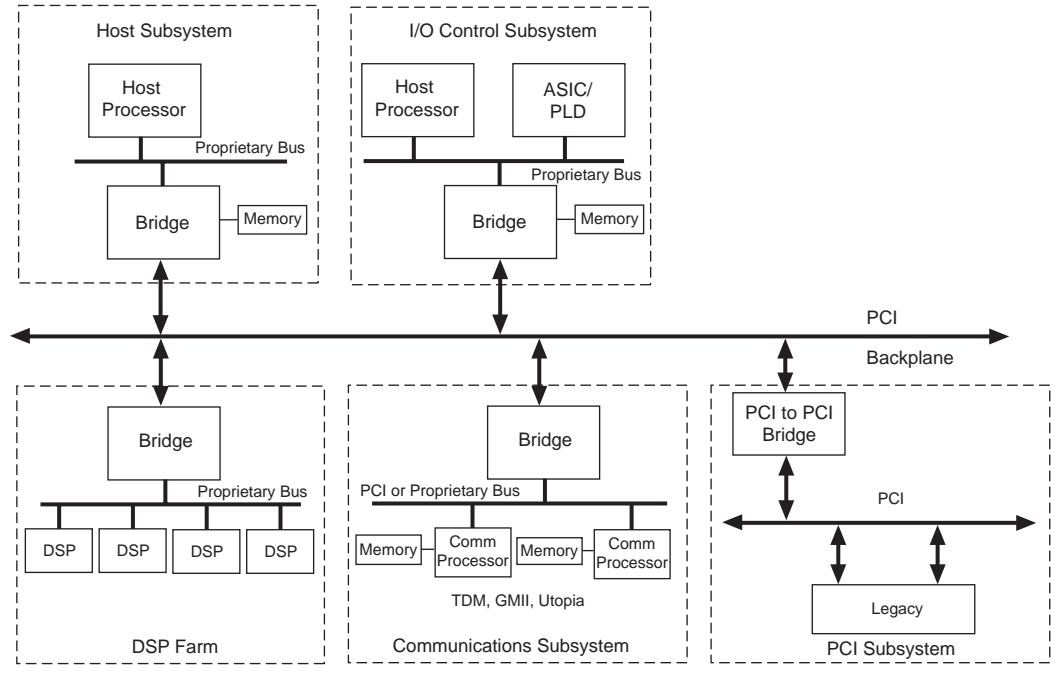
Both the RapidIO and the POS-PHY Level IV standards are source-synchronous mode interfaces with edge-aligned data to the clock.

RapidIO Architecture Support

Mercury device source-synchronous mode supports the RapidIO interconnect architecture at 250 to 500 Mbps, using the LVDS I/O standard.

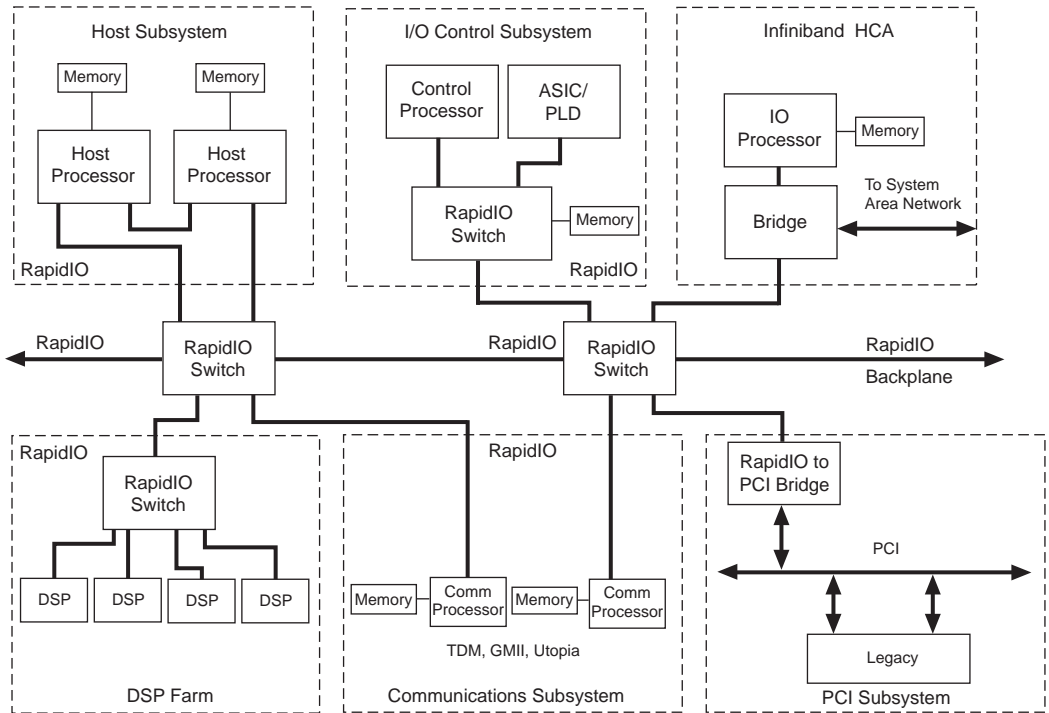
Traditional interconnect architectures have been implemented with PCI bus and circuitry to bridge between the PCI bus and the proprietary buses used on individual subsystems, as shown in [Figure 15](#).

Figure 15. Traditional Interconnect Architecture



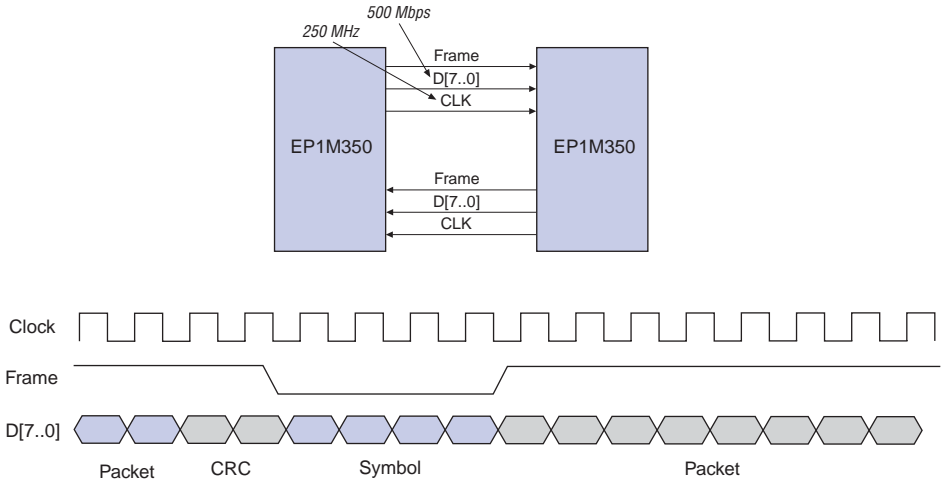
RapidIO switches can be used to route data from one subsystem to another at higher data rates. Figure 16 shows an application using the RapidIO standard.

Figure 16. RapidIO Interconnect Architecture



Mercury devices support 8-bit wide RapidIO interconnect at 500 Mbps with the HSDI channels (with $W = 2$ and $J = 8$). Figure 17 illustrates an 8-bit wide RapidIO interconnect.

Figure 17. 8-Bit Wide RapidIO Interconnect

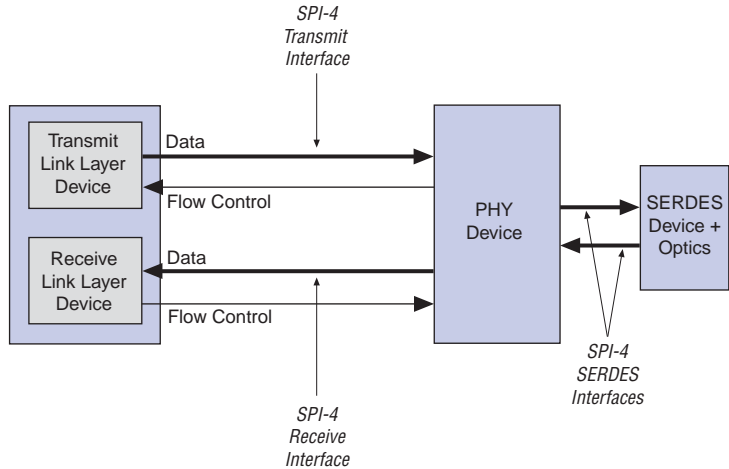


RapidIO interconnect at 250 Mbps can be implemented using the Flexible-LVDS channels using DDR, or with the HSDI channels (with $W = 2$ and $J = 4$ or 8).

POS-PHY Level IV

POS-PHY Level IV (also referred to as POS-4) is a general term that includes both the SPI-4 and SFI-4 interfaces where the 4 indicates OC192 data rate 10 gigabits per second (Gbps). Serdes-Framer Interface (SFI) is the standard interface between the PHY device and the SERDES. System-packet interface (SPI) is the interface between the link layer and the PHY layer. Mercury devices are ideal for implementing transmit and receive modules in the link layer.

SFI-4 requires a 622-MHz clock with the 622-Mbps data rate. SPI-4 requires a 311-MHz clock, which Mercury devices can also support. [Figure 18](#) illustrates a PHY-to-link-layer interface.

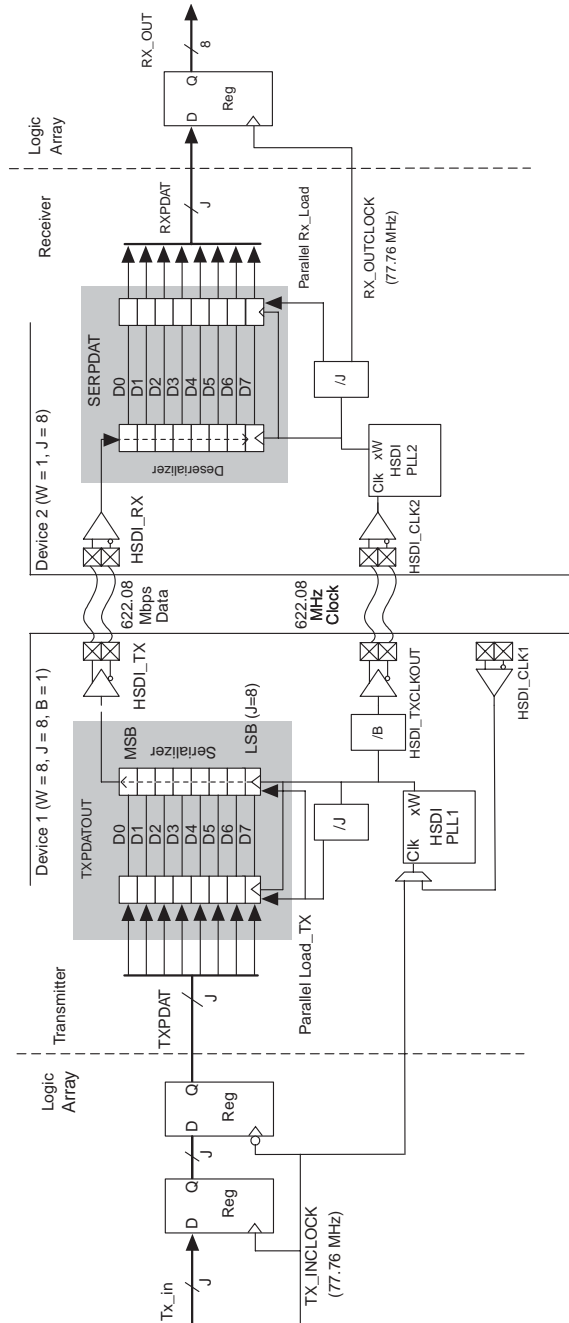
Figure 18. PHY to Link Layer Interface

Source-Synchronous LVDS with $\times 1$ Clocking

Mercury devices can transmit and receive differential data at up to 650 Mbps with one bit transmitted per clock cycle ($\times 1$ clock scheme). This scheme is commonly used for interfacing with optical devices such as with the SFI-4 interface covered in “POS-PHY Level IV” on page 30.

Figure 19 shows the required W , J , and B settings to implement the $\times 1$ clocking scheme for both the transmitter and receiver in Mercury devices at 622 Mbps. While only shown for a Mercury-to-Mercury device setup, this scheme can be used to interface with optical devices.

Figure 19. 622 Mbps LVDS Interface with 622 MHz Clock



Conclusion

Mercury devices can support a wealth of applications using the source-synchronous I/O with the Flexible-I/O feature and HSDI. The source-synchronous mode can support a number of protocols such as the RapidIO, POS-PHY Level IV, and SFI-4 standards. Mercury devices support communication with up to 18 channels operating at data rates of up to 840 Mbps in source-synchronous mode using LVDS, LVPECL, and PCML. This flexibility plus high internal core performance makes the Mercury architecture ideal for telecommunications applications.



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