



HardCopy Series

ASIC Gain Without the Pain



January 2005

HardCopy Structured ASICs



HARDCOPY™

Altera's HardCopy® series is the industry's most compelling structured ASIC solution. With its unique FPGA front-end design flow, you can use Altera's high-density, high-performance FPGAs to develop, verify, and finalize your system design before committing to silicon. The product development flexibility and time-to-market benefits of the HardCopy series are unparalleled by any other offering in the market. Ideal for high-volume designs, HardCopy structured ASICs give you a competitive edge in storage, networking, wireless communication, consumer electronics, telecom, military, and industrial applications.

The HardCopy series includes three families: HardCopy II, HardCopy Stratix®, and HardCopy APEX™ structured ASICs. The 90-nm HardCopy II devices use Stratix II FPGAs for prototyping and testing and offer up to 350-MHz system performance, 2.2 million ASIC gates, and 8.8 million bits of memory. HardCopy Stratix devices, on 0.13-µm process technology, use Stratix FPGAs for prototyping and offer up to 1 million ASIC gates and 5.6 million bits of memory. The first-generation HardCopy family, HardCopy APEX devices on 0.18-µm process technology, offers up to 600K ASIC gates and 442K bits of memory.

In today's market, with increasing competitive pressures and shorter product life cycles, you have less time to develop and differentiate higher performance, more complex designs—designs often requiring long verification and simulation cycles. Despite your team's best efforts, ASICs still frequently need to be re-spun, further increasing development time and schedule pressure. In fact, Collett International Research, Inc. estimates that while 40 percent of all standard-cell ASIC designs require only one spin, over 60 percent have to be re-spun due to logic verification problems, new features added during development, or system integration challenges (Figure 1). In today's competitive market, the demand to meet development schedules is enormous, but the unique HardCopy series can help you better manage these pressures.

Standard-cell ASICs were once considered the best approach to achieve low unit cost for high-performance, complex logic designs. However, development costs are escalating with each new process technology (Figure 2).

Companies developing ASIC designs using 0.13-µm process technology can expect total development costs to be in excess of US\$20 million, making those devices viable for only the highest volume products. HardCopy structured ASICs address these fast-rising development costs.

Figure 1. ASIC Design Spins

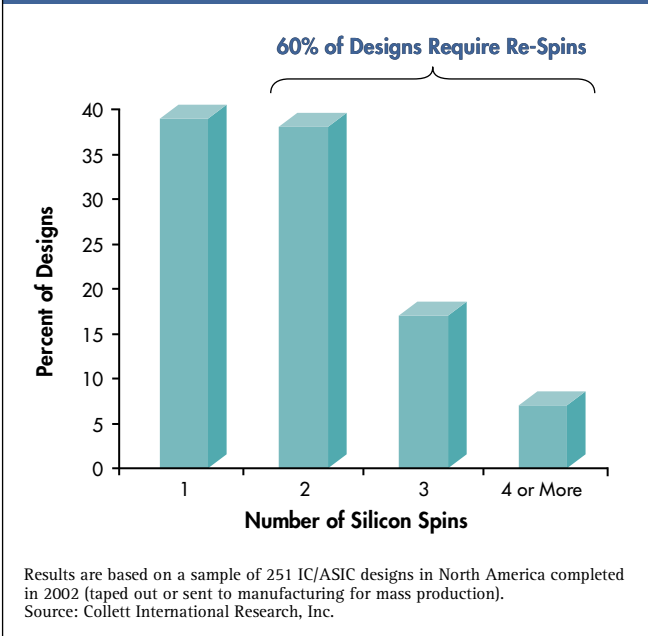
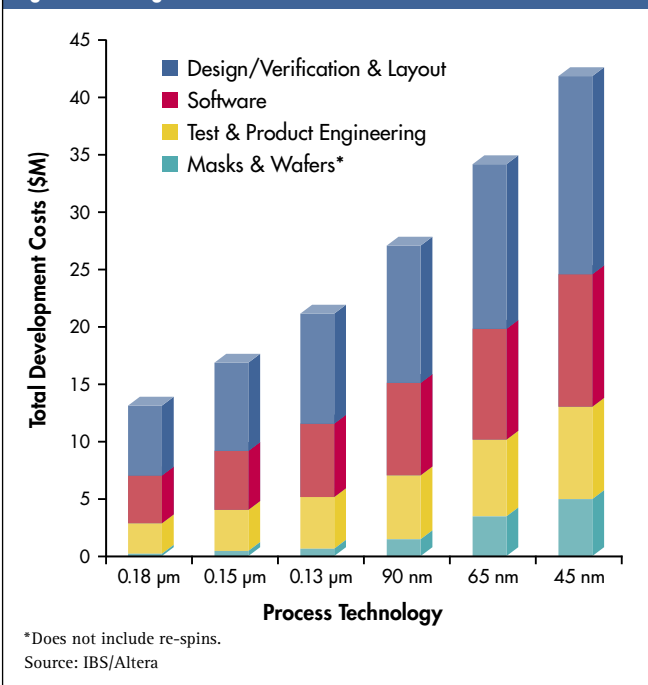


Figure 2. Rising ASIC Costs



Structured ASIC Technology

Structured ASICs were conceived to bridge the gap between standard-cell ASIC technology and FPGAs, offering low unit cost combined with faster development time. Structured ASICs start with standard, pre-tested base layers of logic and hard intellectual property (IP), and the proprietary design is then implemented on the top few metal layers, as shown in Figure 3. However, some structured ASICs still require long design verification time and exhaustive simulation to reduce the risk of design problems, and even then the design can not be fully validated until the prototypes are manufactured. With these devices, you still run the risk of re-spinning the design, increasing your development time, schedule pressure, and costs.

A Unique Design Method

Altera's HardCopy structured ASICs offer a unique prototype-to-production design process. Using your existing design environment, you can leverage Altera's FPGAs as your design's front end. Once you finalize your design, Altera's HardCopy Design Center seamlessly migrates it to HardCopy structured ASICs for high-volume production, with first silicon in seven to eleven weeks. This process dramatically shortens the time it takes to bring your product to market so you are more likely to hit your market's window. In addition, Altera's unique process minimizes your development risk—your system is fully tested and verified before you need to commit to ASIC silicon. You can also test-market features and develop multiple designs to choose which is most likely to succeed. Design flexibility is in your hands.

Figure 4 illustrates the advantages that HardCopy devices offer over other structured ASICs.

Manage Your Product Life Cycles

Altera's FPGAs and HardCopy structured ASICs offer you increased production flexibility that puts you in control of costs throughout your product's life cycle. You can prototype and enter into early production with an Altera FPGA, and when you're ready, migrate to the HardCopy version of the design for volume production (Figure 5).

Once mainstream production is completed and you transition to the system's end of life, you can use the FPGA version to finish out the remainder of the product life and avoid excess inventory. In addition, during the mainstream production phase, you can always decide to shift back to the

Figure 3. Structured ASIC Layers

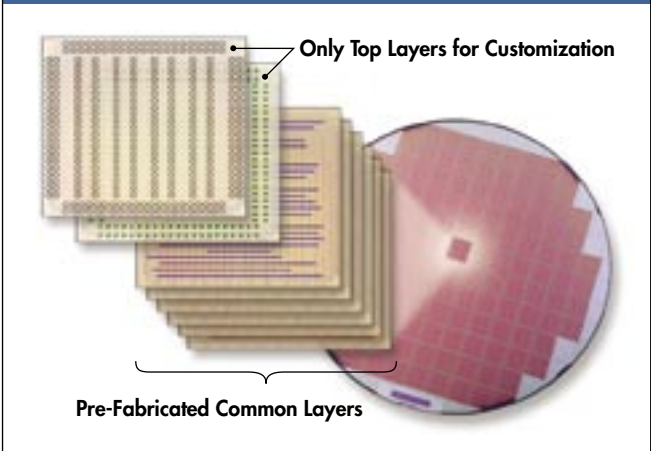
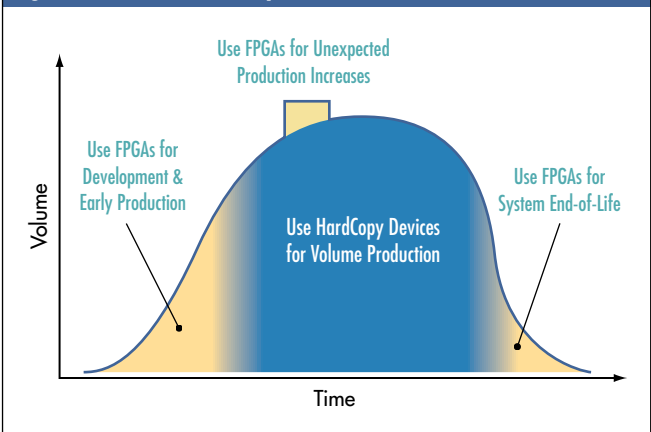


Figure 4. Lowest Risk & Fastest Path to Silicon Success

HardCopy Structured ASICs		Other Structured ASICs
✓	Low NRE & Price	✓
✓	ASIC-Level Performance & Power Consumption	✓
✓	Shorter Development Cycle	✓
✓	FPGA Prototype	
✓	Seamless Migration	
✓	Guaranteed Silicon Success	
✓	Use Existing Design Flow	

Figure 5. Production Life Cycle

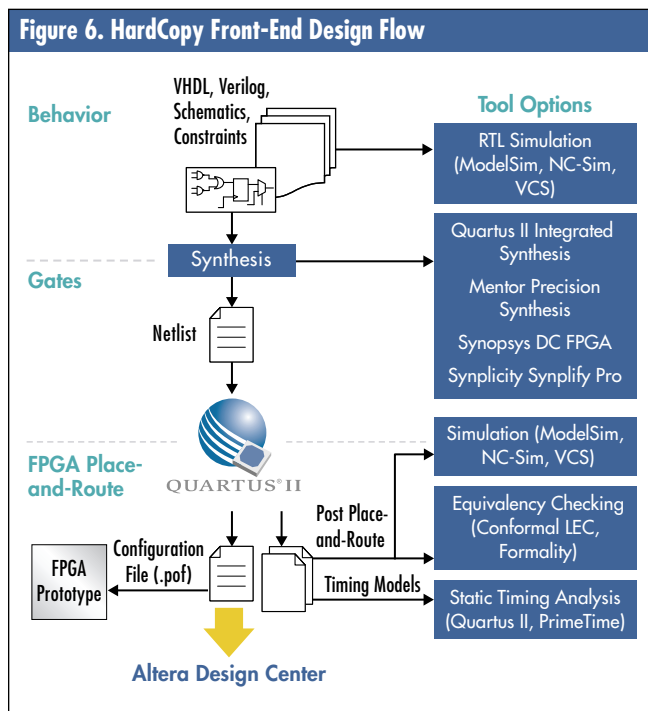


FPGA if you choose to update the design to meet new standards, test market a new feature, or customize the design for specific customer projects. Because HardCopy structured ASICs are pin-compatible and functionally equivalent to the FPGA prototype, you can even use an off-the-shelf FPGA in a HardCopy device socket for unexpected increases in demand.

Use Your Existing Design Environment

You can design HardCopy structured ASICs using standard synthesis, verification, timing analysis, and equivalency checking tools from Cadence, Mentor Graphics, Synopsys, and Synplicity in conjunction with Altera's Quartus® II design environment (Figure 6). When designing for HardCopy structured ASICs, you can take advantage of all Quartus II software design flow features as well as the EDA tools typically used in FPGA or ASIC design flows, minimizing additional training time and expenses. Quartus II software is the most advanced software for structured ASIC design as it is the only design software that supports parallel FPGA and structured ASIC design and development.

Using the latest Quartus II software, you can target an FPGA at the beginning of your design cycle with the idea of migrating to a HardCopy device at a future date. Alternatively, you can target a HardCopy structured ASIC up front, using the identical design flow, architecture, and tools as the Altera FPGA prototype. Once your design is completed, Quartus II software automatically generates the files to submit to the HardCopy Design Center to start the migration process.



Quartus II software supports the same basic design, register transfer level (RTL) synthesis, place-and-route, and verification flows used by ASIC designers. Table 1 highlights some of the features in the Quartus II software that support HardCopy device design. For a complete description of Quartus II features, visit www.altera.com/software.

Table 1. HardCopy Design Features in Quartus II Software

Feature	Benefits
HardCopy Optimization Wizard	Optimizes HardCopy designs, generates floorplan views of the final placement, and calculates system performance.
Device Resource Guide	Indicates which HardCopy II devices are suitable for a specific FPGA design migration.
PowerPlay Early Power Estimator	Calculates power consumption for the design when implemented in the HardCopy device.
Design Assistant	Performs design rule checking to guarantee a seamless migration from the FPGA prototype to the final HardCopy device.
HardCopy Files Wizard	Generates all the file deliverables that the Altera HardCopy Design Center needs to produce the final HardCopy device.

Take Advantage of Intellectual Property

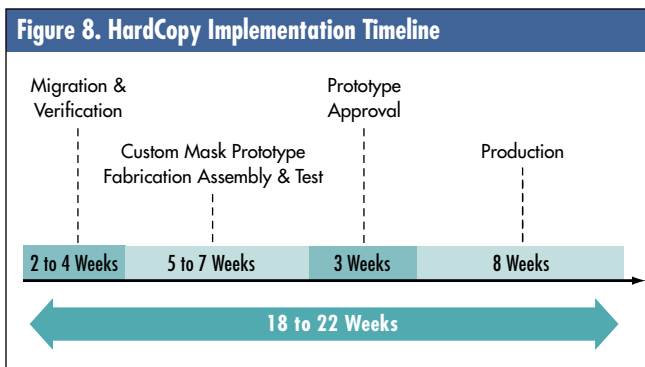
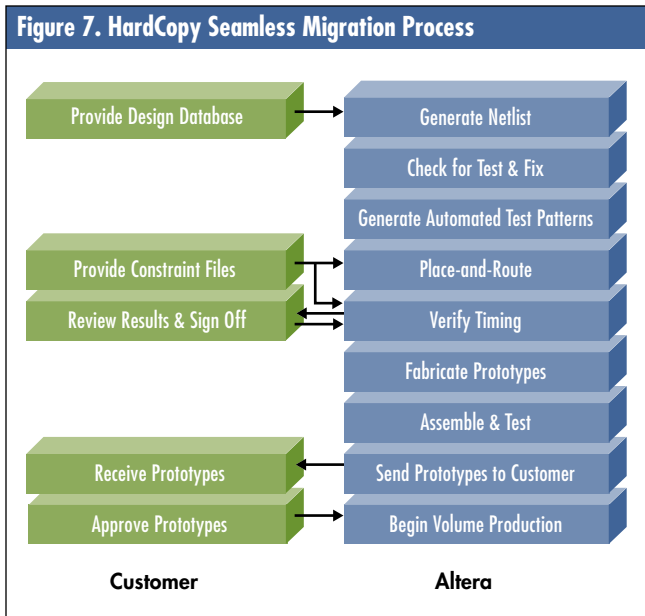
Altera and Altera Megafunction Partners Program (AMPPSM) partners offer an extensive library of standard IP cores. IP cores provide total solutions by targeting specific application areas, improving performance and system reusability, and significantly reducing a product's time-to-market. All Altera IP can be included in your HardCopy design without any additional licensing fees. You can visit the IP MegaStore™ web site at www.altera.com/ipmegastore.

Leverage the Industry's Most Versatile Processor

For embedded systems, Altera offers the Nios® II family of flexible processors. The Nios II processor, one of the most popular embedded processor architectures in the world, is available in several development kits, and includes a library of standard peripherals. For more details on the Nios II embedded processor, please refer to www.altera.com/nios.

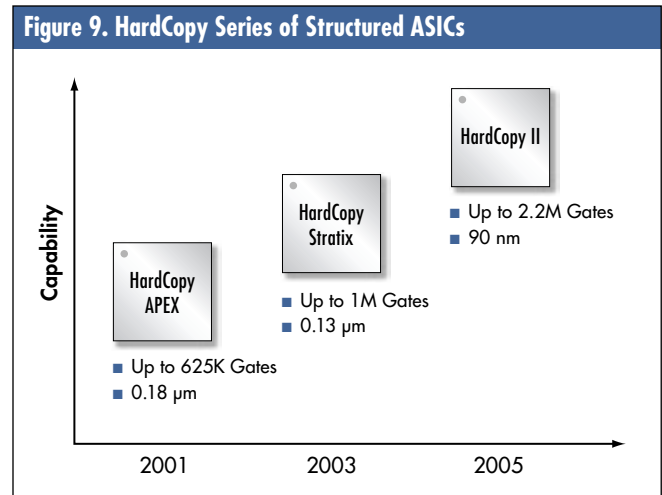
Enjoy Guaranteed Production Success

Once you are satisfied with your design, Quartus II software automatically generates design files for Altera's HardCopy Design Center. The Design Center's seamless migration process (Figure 7) minimizes risk and guarantees success to low-cost production devices with minimal effort from you. You get guaranteed, fully operational prototypes and production units in record time (Figure 8).



HardCopy Structured ASIC Series

The HardCopy series of structured ASICs offers a range of solutions for your logic density and performance requirements. Figure 9 shows an overview of the HardCopy series of structured ASICs, including HardCopy APEX, HardCopy Stratix, and HardCopy II devices.



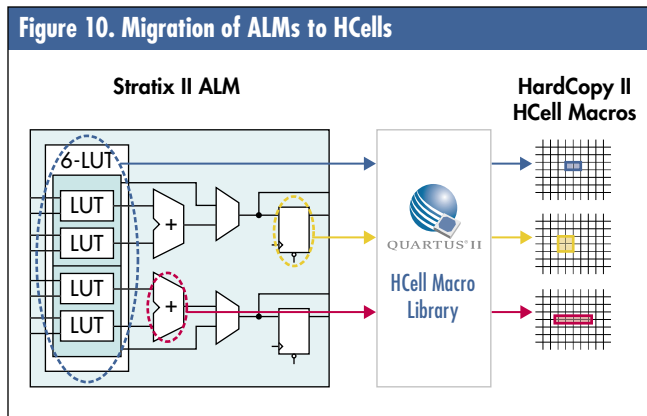
HardCopy II

The new 1.2-V, 90-nm HardCopy II family builds on the success of Altera's first two generations of structured ASICs. Using Stratix II FPGAs for prototyping and testing, then migrating to HardCopy II devices, you are guaranteed success with your high-volume production devices. HardCopy II devices offer 2.2 million ASIC gates for logic prototyping, 8.8 million bits of memory, and over 350-MHz system performance. Compared to the FPGA prototype, HardCopy II devices offer over 50 percent core power reduction at as little as one-tenth the cost.

HardCopy II devices are built on a fine-grained architecture designed for low cost that is made up of an array of HCells. An HCell is the smallest HardCopy II building block that enables the construction of any combinatorial gate and sequential element. This HCell architecture supports seamless FPGA migration while providing the density, cost, performance, and power benefits of ASIC technology.

The seamless migration of logic and DSP functions from Stratix II adaptive logic modules (ALMs) to HardCopy II HCells is implemented through a library of pre-defined and pre-verified HCell macros in Quartus II software. Each macro, made up of multiple HCells, corresponds to a DSP

block or a unique ALM configuration (Figure 10). Quartus II software uses the macro library to map each ALM into the HardCopy II HCell-based architecture. No risky re-synthesis is required.



Each HardCopy II base array has embedded hard IP, such as RAM, I/O cells, and PLLs, that is functionally equivalent to the corresponding structures in Stratix II FPGAs. Quartus II software maps the I/O cells in Stratix II FPGAs to the same pin locations in HardCopy II devices to deliver a pin-compatible device. In addition, the HardCopy II packages are equivalent to the Stratix II packages, and the HardCopy II die is produced on the same 90-nm process at the same production facility that produces the Stratix II devices.

The result of this FPGA front-end design process and seamless migration is a structured ASIC that is functionally equivalent and pin-compatible to the Stratix II FPGA prototype. What's more, HardCopy II devices require less than

50% of the core power compared to the Stratix II FPGA design because the HardCopy II die is significantly smaller, and because only the logic used in the HardCopy II device is powered on.

External memory interface circuitry support includes 233-MHz DDR2 SDRAM and 250-MHz RDRAM II. HardCopy II devices also support 1-Gbps differential I/O and high-speed interfaces, including 10-Gigabit Ethernet (XSBI), SFI-4, SPI 4.2, HyperTransport™, RapidIO™, and UTOPIA Level 4 interfaces at up to 1 Gbps. Table 2 provides an overview of the HardCopy II device family.

HardCopy Stratix

Introduced in 2003, Altera's HardCopy Stratix family is manufactured on 1.5-V, 0.13-µm process technology. These devices use Stratix FPGAs for prototyping and have the same logic element (LE) architecture as Stratix devices. With 300 thousand to 1 million ASIC gates and up to 5.6 million bits of memory, HardCopy Stratix devices offer a 50 percent performance increase and 40 percent lower power consumption than the Stratix prototype.

HardCopy Stratix devices support a wide range of high-speed interfaces—including the SPI-4 Phase 2, 10-Gigabit Ethernet (XSBI), and RapidIO interfaces. HardCopy Stratix devices also support the LVDS/LVPECL and HyperTransport high-speed I/O standards. These advanced capabilities allow designers to connect high-speed memory devices like quad-data rate (QDR) and zero-bus turnaround (ZBT) SRAMs. Table 3 provides an overview of the HardCopy Stratix device family.

Feature	HC210W ¹	HC210	HC220	HC230	HC240
ASIC Gates ²	1M	1M	1.6M	2.2M	2.2M
Additional Gates for Digital Signal Processing (DSP) Blocks ³	0	0	0.3M	0.7M	1.4M
Total RAM Bits	875,520	875,520	3,059,712	6,345,216	8,847,360
Phase-Locked Loops (PLLs)	4	4	4	8	12
Maximum User I/O Pins ⁴	300	334	494	698	951
Packages	484-pin Wire Bond FBGA ⁵	484-pin FBGA	672-pin FBGA, 780-pin FBGA	1,020-pin FBGA	1,020-pin FBGA, 1,508-pin FBGA
FPGA Prototype Options	EP2S30 EP2S60 EP2S90	EP2S30 EP2S60 EP2S90	EP2S60 EP2S90 EP2S130	EP2S90 EP2S130 EP2S180	EP2S180

Notes

1. HC210W is in a wire bond package. Devices in wire bond packages offer different speed and power characteristics than devices in flip chip packages.
2. Available for both logic and DSP functions as implemented in the Stratix II FPGA prototype.
3. Additional ASIC gates available for Stratix II DSP block functions.
4. Preliminary information. I/O pin count composed of user I/O and clock pins.
5. FBGA: FineLine BGA® package.

Table 3. HardCopy Stratix Family Overview					
Feature	HC1S25	HC1S30	HC1S40	HC1S60	HC1S80
ASIC Gates	325K	400K	500K	700K	1,000K
LEs	25,660	32,470	41,250	57,120	79,040
M512 RAM Blocks (512 Kbits + Parity)	224	295	384	574	767
M4K RAM Blocks (4 Kbits + Parity)	138	171	183	292	364
M-RAM Blocks (512 Kbits + Parity)	2	2 ¹	2 ¹	6	6 ¹
Total RAM Bits	1,944,576	2,137,536	2,244,096	5,215,104	5,658,048
DSP Blocks	10	12	14	18	22
Embedded Multipliers ²	80	96	112	144	176
PLLs	6	10	12	12	12
Maximum User I/O Pins	473	597	615	773	773
Packages	672-pin BGA ³	780-pin BGA	780-pin BGA	1,020-pin BGA	1,020-pin BGA
FPGA Prototype	EP1S25	EP1S30	EP1S40	EP1S60	EP1S80

Notes

1. The number of M-RAM blocks in this device differs from the number of M-RAM blocks in the corresponding Stratix FPGA.
2. Total number of 9x9 multipliers. To obtain the total number of 18x18 multipliers per device, divide the total number of 9x9 multipliers by a factor of 2. To obtain the total number of 36x36 multipliers per device, divide the total number of 9x9 multipliers by a factor of 8.
3. BGA: ball-grid array.

HardCopy APEX

HardCopy APEX devices, manufactured on 1.8-V, 0.18- μ m process technology, were Altera's first generation of HardCopy devices. HardCopy APEX devices maintain the equivalent APEX 20KC and APEX 20KE FPGA architecture and features. Table 4 shows the features and packages available with HardCopy APEX devices.

Table 4. HardCopy APEX Family Overview				
Feature	HC20K400	HC20K600	HC20K1000	HC20K1500
ASIC Gates	200K	300K	450K	600K
LEs	16,640	24,320	38,400	51,840
Maximum RAM Bits	212,992	311,296	327,680	442,368
PLLs	4	4	4	4
Maximum User I/O Pins	502	624	708	808
Packages	652-pin BGA, 672-pin FBGA	652-pin BGA, 672-pin FBGA	652-pin BGA, 672-pin FBGA, 1,020-pin BGA ¹	652-pin BGA, 1,020-pin BGA
FPGA Prototype Options	EP20K400C EP20K400E	EP20K600C EP20K600E	EP20K1000C EP20K1000E	EP20K1500E

Note

1. "F33" ordering code.

Contact Altera Today

With the HardCopy series and the Altera Design Center, Altera provides the best high-volume solution for your high-density designs. Visit www.altera.com/hardcopy today to learn more about the HardCopy series.



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