Building Reliability Into Full-Array BGAs

Yuan Li, Ph.D., Anil Pannikkat, Ph.D.,
Larry Anderson, Tarun Verma, Bruce Euzent
Altera Corporation
101 Innovation Drive, San Jose, CA 95134

Biography

Yuan Li received his BS in the Department of Precision Instrument at Tsinghua University in 1989, MS and Ph.D. in Mechanical Engineering at University of Colorado at Boulder in 1993 and 1996 respectively. His main research areas were advanced electronic packaging such as flip chip and BGA, electronic package reliability simulation using finite element, SMT technology, process modeling and optimization, artificial neural network. From March 1996 to Oct. of 1997, he was a SMT Engineer in Exabyte Corporation in Boulder, Colorado. From Oct. 1997 to July 1998, he was a Research Associate at University of Colorado. Since July 1998, he is a senior Packaging Engineer at Altera Corp., responsible for reliability, thermal and electronic characterization of electronic packages. He has published numerous papers in ASME Journal of Electronic Packaging, IEEE CPMT and IEE Journal of Electronic Manufacturing. He has received 1996 Best Paper Award from Journal of Electronic Packaging.

Anil Pannikkat received his Bachelor of Technology Degree from IIT Bombay, India and his MS and Ph.D. degrees in Materials Science & Engineering from Cornell University, Ithaca, NY. He is presently in the Quality & Reliability Group @ Altera. His interests are primarily in the development of advanced packaging technologies and component and board level reliability.

Larry Anderson received his BSEE from San Jose State University in 1965 and joined General Microelectronics as a device characterization engineer. Over his 35 year career he has held various management positions in operations (final test, assembly, wafer fab, wafer sort and mask making), product design, foundry business, and package development. He has also worked for Electronic Arrays, NEC, IMP and Altera Corp. He joined Altera in 1992 and is currently Director of Package and Assembly Technology.

Tarun Verma received the B. Tech. in Metallurgical Engineering from Indian Institute of India, Kanpur, India in 1985 and M.S. in Material Science from University of California at Berkeley in 1987. He was a Packaging Engineer with National Semiconductor from 1987 to 1989. Since 1990, he has held various engineering positions at Altera Corporation. Currently, he is a Senior Manager in charge of package development.

Bruce Euzent received the B.S. in electrical engineering from Cornell University in 1972 and the Masters of Engineering from Carnegie-Mellon Univeristy in 1974. He joined Intel Corporation in 1974 as a Reliability Engineer. In 1978 he became Intel's Customer Quality Assurance Manager for Europe. In 1983 he became the manager of Intel's Non-Volatile Memory Quality and Reliability department. In 1991 he joined Weitek Corporation as Director of Quality and Reliability. Since 1995 he has been Director of Quality and Reliability at Altera Corporation. He is a member of IEEE and a past General Chair of the IRPS. He has published papers on Non-Volatile Memory Reliability, Hot Electron Effects, Package Reliability, Electromigration, Failure Analysis, and ESD.

© SEMI 2000

Abstract:
To provide the benefits of higher I/O density, smaller feature size, and better electrical performance, a full-array 1.0-mm pitch BGA package family were developed. Three package options, termed as A, B and C, were investigated. Each of these options has its own advantages and disadvantages. Moiré Interferometry technique was used to measure the effective coefficient of thermal expansion (CTE) of these three options. To more efficiently access package reliability, a three-dimensional and non-linear finite element method was established. This method has shown good accuracy in predicting solder joint reliability. Using this method, various factors were studied including die size, package size, package pad opening size, board pad size, solder ball size, die attach thickness, pad design, substrate thickness and board thickness. These studies have given us a good understanding of the effect of each factor and the direction to improving solder joint reliability. The possible optimum settings of paremeters were selected for the packages. Finite element modeling was used to determine solder joint reliability of the three package options versus die size and package size. Thus, a roadmap of solder joint reliability vs substrate technology, die size and package size was established. From this roadmap, a preset reliability goal can always be achieved by choosing the right combination of substrate, die and package size.

Data:

Introduction

To provide packages with high-speed and high I/O density, a 1.0-mm-pitch full–array BGA family was developed. This family includes a number of die sizes and package sizes with a good proportion of large dies. Since it's pitch is 1.0 mm instead of the more common 1.27 mm, smaller solder balls and pads were used. All these factors made the package's solder joint reliability a critical issue. Three package options, A, B and C, were investigated. A, B and C represented different substrate materials and package internal structures. Accurate finite element modeling was employed to fundamentally study the effects of various important factors. Based on the results of the study, the optimum settings of paremeters were selected for the packages. Finite element modeling was used to determine solder joint reliability of the three package options versus die size and package size. Thus, a roadmap of solder joint reliability vs substrate technology, die size and package size was established. From this roadmap, a preset reliability goal can always be achieved by choosing the right combination of substrate, die and package size.

Package options

Three package options, A, B and C, were investigated. Each of these options has its own advantages and disadvantages. Moiré Interferometry technique was used to measure the effective coefficient of thermal expansion (CTE) of these three options. The measured CTE across the surface of each package options was shown in Fig. 1. CTE of option C matches that of FR4 board very well. Option A has a great CTE mismatch with FR4 board. Option B falls in between. Finite element modeling was also used to evaluate the viability of each option, which will be discussed later.

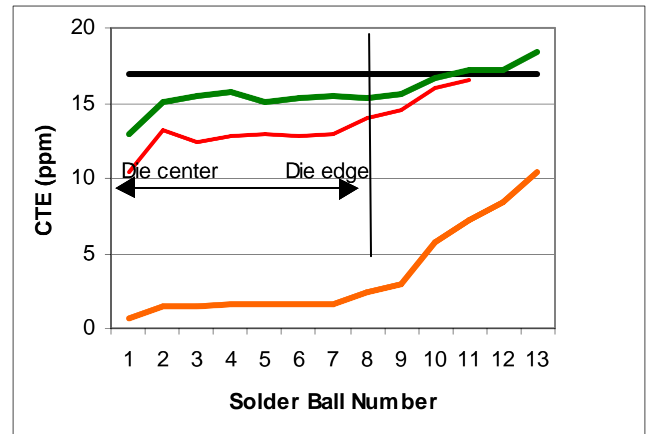


Fig. 1. CTEs of the three options measured by Moiré Interferometry

Finite element modeling method

The modeling methodology and the life prediction model in [1] were adopted to predict

© SEMI 2000

solder joint fatigue life. Because of the high homologous temperature (ratio of operating and melting temperatures in absolute scale) and slow strain rates in actual service conditions, time dependent creep is the primary deformation mode for eutectic solder joints. Grain boundary sliding and matrix creep are the major deformation mechanisms considered in this methodology. Readers are referred to [1] for details.

ANSYS® [2] was used for finite element analysis. The modeling approach can be described as follows: A one-quarter symmetric model of the package was developed using eight-node 3-D brick elements. This coarse model was first analyzed using linear elastic analysis to determine the location of the solder joint failing first. The joint at that location was removed from the model and the rest of the package was analyzed as a substructure using linear properties of solder. The substructure was analyzed for a unit temperature increase resulting in a super-element with a stiffness matrix and a load vector. Finally, a detailed model of the solder joint at the location of first failure was developed and a non-linear creep analysis was done to predict the accumulated creep strain per cycle. In order to avoid the inaccuracy caused by interfacial singularity, creep strains for a 0.025mm layer of solder at the package-solder or solder-board interface were used to predict mean fatigue life instead of the maximum creep strain. The life prediction model [1] was shown in Equation (1).

$$N_f (0.02xE^{Eq}_{GBS} + 0.063xE^{Eq}_{MC}) = 1.0 \qquad (1)$$

Where N_f is mean fatigue life, E^{Eq}_{GBS} *and* E^{Eq}_{MC} are the accumulated equivalent, multi-axial creep strains for grain boundary sliding and matrix creep per cycle respectively.

Finite element modeling versus experiment

Various daisy chain packages have been tested through thermal cycling. These parts comprised of combinations of different die sizes, package sizes and substrates. The daisy chain board used was FR4 and 1.57 mm (62 mils) thick. The thermal cycling profile is 0 – 100°C with a frequency of 2 cycles per hour. The sample size is usually 32. First failures normally occurred in the solder joints under the corner of die due to the constraint of die's very low CTE (coefficient of thermal expansion). See Fig. 2. The actual fatigue life is obtained by fitting failure data using a log-normal or Weibull distribution to predict cycles to 0.1% fail. In general, the modeling process is as follows: First, a simulation is run using the designed nominal dimensions for each package; then after board mounting, a part is cross-sectioned and the actual dimensions are input to the model for a second run. This way we can know the difference between the design specified dimensions and the actual ones and the consequent effect on reliability. The comparison between the modeling predictions and the actual failure free life was shown in Fig. 3. The modeling predictions matched the actual results quite well. It also shows that option C has the best board-level reliability.

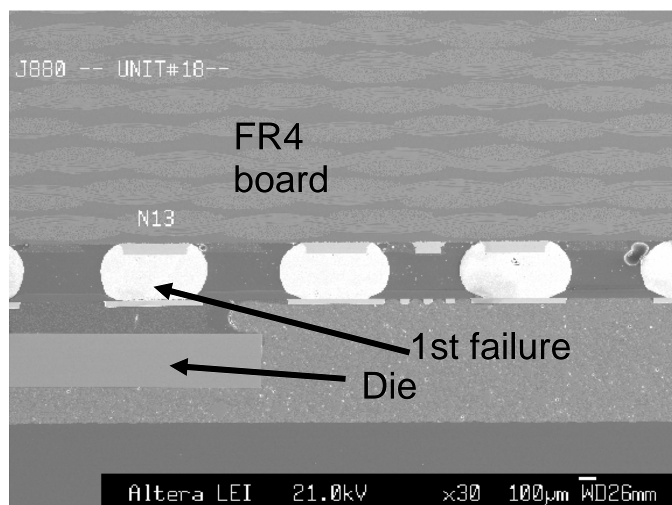


Fig. 2. First failure location

© SEMI 2000

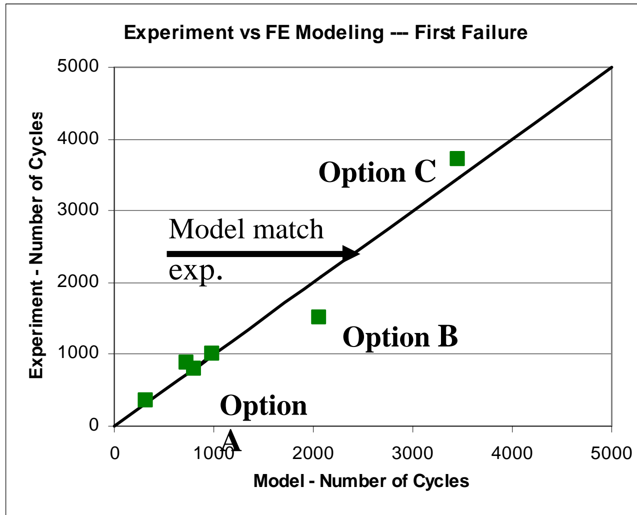


Fig. 3. Modeling predictions VS actual results

Parametric study

Various parameters were studied to find their effect on reliability using finite element modeling. The results were reported below.

Die size and package size

Fig.4 showed failure free life versus die size for two package sizes. Two observations could be made from this figure. The obvious one is that solder joint fatigue life decreases with die size. The other observation is that the larger package gives better fatigue life than the smaller one. This can be attributed to two reasons: one is that the larger package has more solder balls to share stress; the second one is that the larger package has a smaller die-to-package ratio, thus more compliant. To verify the accuracy of this observation, two daisy chain packages with every thing the same except the package size and number of solder balls were built. The Weibull plot was shown in Fig. 5. It is clear that the 27mm package had longer fatigue life than the 23-mm package.

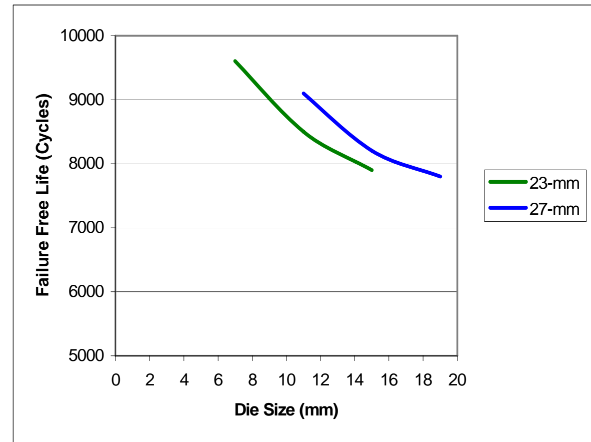


Fig. 4. Failure free life VS die size

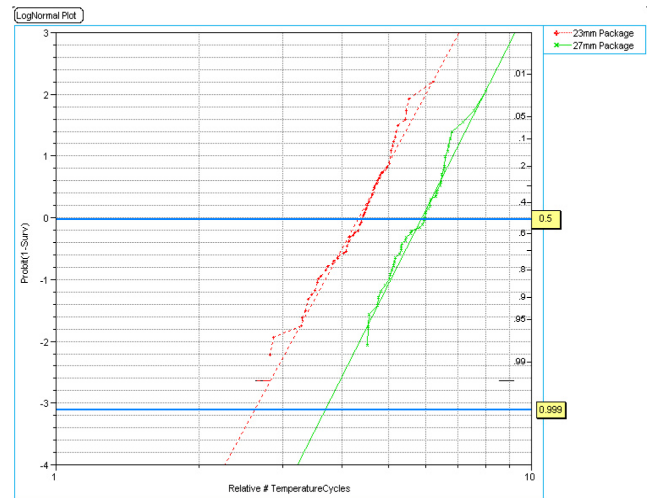


Fig. 5. Weibull plot of two packages

Package pad opening size

Pads are solder mask defined (SMD) on package substrates and non-solder mask defined (NSMD) on boards, thus solder joint failures normally occur at SMD side due to the fact that SMD causes higher stress concentration [3-4]. Since package pad opening (defined by solder mask) is the length that crack needs to propagate before the solder joint totally fails, larger package pad openings generally improve solder joint reliability. For the case studied, fatigue life of the solder joint tripled by increasing package pad

© SEMI 2000

opening from 0.45 mm to 0.60mm, as shown in Fig. 6. In this case, board pad size was constant at 0.46 mm.

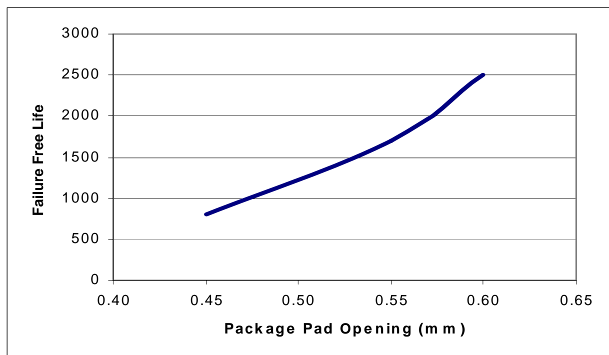


Fig.6. Failure free life VS package pad opening

Board pad size

Three board pad sizes were modeled: 0.30 mm, 0.38 mm and 0.46 mm, while package pads were 0.38 mm. It was found that 0.30-mm pads resulted in the longest solder joint fatigue life. The results were shown in Fig. 7. It can be explained as follows. Since package pads are solder mask defined and board pads are non-solder mask defined, stress tends to concentrate more at the interface between solder joints and package pads. Smaller board pads will shift more stress towards the other interface between solder joints and board pads, thus stress becomes more balanced at both the interfaces, resulting in an overall less stress.

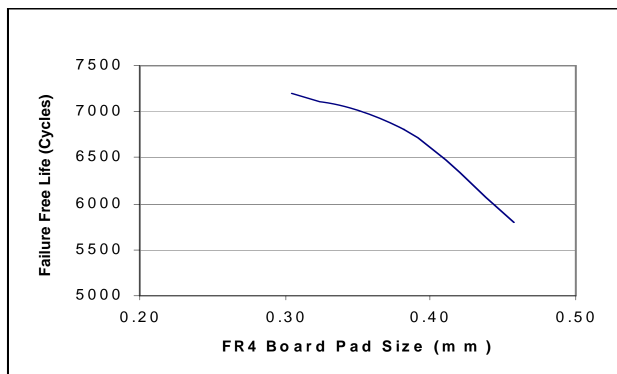


Fig. 7. Failure free life VS board pad size

Solder ball size

Finite element modeling indicated that 0.635 mm solder balls would improve fatigue life by over 50% compared with 0.45 mm balls, see Fig. 8. The actual test results matched the predictions very well.

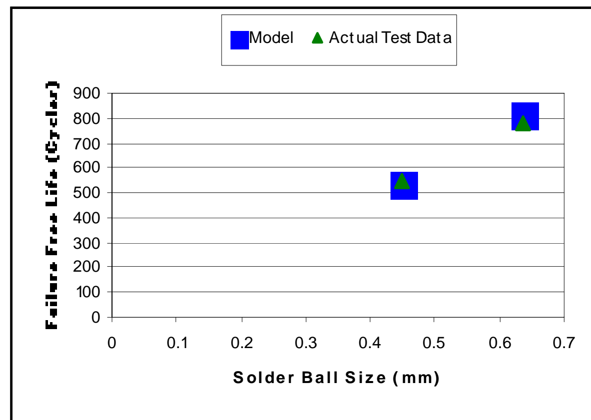


Fig. 8. Failure free life VS solder ball size

Die attach thickness

Die attach thickness control is very important. Its variation has profound effect on solder joint reliability as shown in Fig. 9

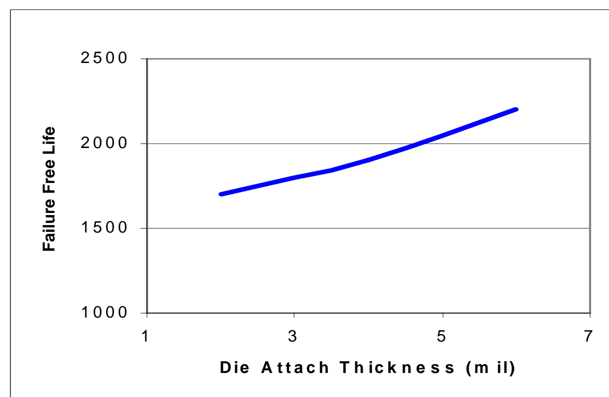


Fig. 9. Failure free life VS die attach thickness

SMD and NSMD

SMD and NSMD package pads were compared. NSMD pad was predicted to improve solder joint reliability by more than 100%. Identical daisy

© SEMI 2000

chain parts with SMD and NSMD pads were tested. Packages with SMD pads failed first at 3600 cycles. The prediction is about 3400 cycles. Packages with NSMD pads had no failures at 5000 cycles when the test was stopped. The prediction is about 7000 cycles. The results are shown in Fig. 10. Previous studies [3-4] have shown the same trend.

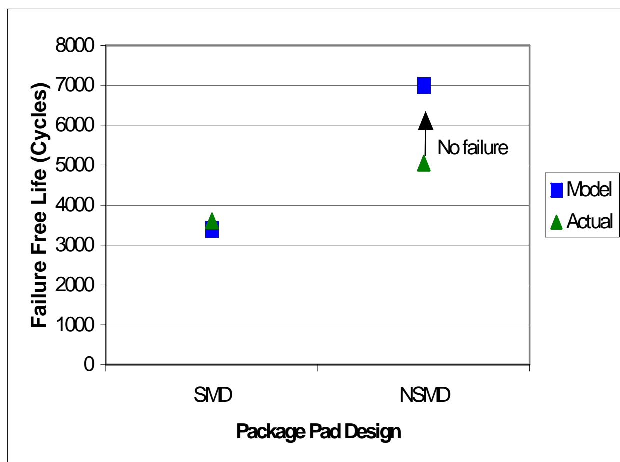


Fig. 10. SMD vs NSMD

Substrate thickness

For BGAs using BT substrate, substrate thickness contributes greatly to solder joint reliability. 0.35-mm- and 0.55-mm- thick substrates were compared. It was found that 0.55-mm-thick substrate resulted in close to 90% increase in solder joint fatigue life as shown in Fig. 11. Two daisy chain packages were tested. The one with 0.35mm thick BT substrate had first failure at 2600 cycles. The prediction is 2400 cycles. The one with 0.55mm thick BT substrate had no failure at 3700 cycles when the test was stopped. The prediction is about 4700 cycles.

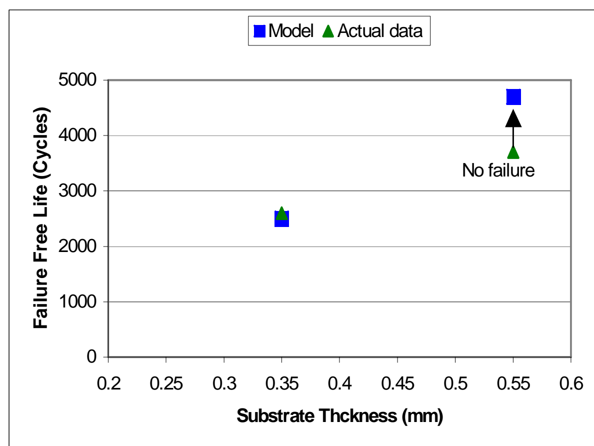


Fig. 11. Failure free life VS substrate thickness

Board thickness

Nowadays, many industries use printed circuit boards thicker than 1.57mm (62 mils), i.e., 2.36 mm (93 mils), hence the effect of board thickness was also studied. It was found that 93-mil boards could result in over 40% reduction in solder joint fatigue life compared to 62-mil boards, see Fig. 12.

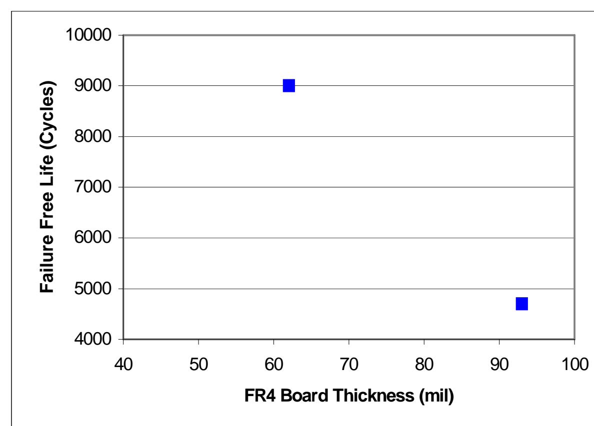


Fig. 12. Failure free life VS board thickness

Roadmap

The parametric study has given us a good understanding of the effect of each factor. An optimum setting of each factor was selected for

© SEMI 2000

the development of the full-array BGA family. Package options, A, B and C, were continually studied. For each option, a plot was generated to correlate solder joint reliability with die size and package size using finite element modeling. Due to propritary reasons, the plots will not be shown here. These plots become a road map of substrate technologies, die size and package size where the preset reliability goal can always be achieved by selecting the right combinations.

Conclusion:

An accurate three-dimensional and non-linear finite element modeling has been established. It has been used to systematically study the effect of various factors on solder joint reliability of BGAs. These factors include die size and package size, package pad opening size, board pad size, solder ball size, die attach thickness, SMD or NSMD, package substrate thickness and board thickness. The results of these studies have provided guidance for the development of a family of 1.0-mm pitch full-array BGAs. Three package options were investigated. Using finite element modeling, a road map of substrate technologies, die size and package size was developed. From this road map, a right combination of die, package and substrate can be easily chosen to ensure packages to achieve or pass the preset reliability goal.

References:

1. Syed, A.R., 1997. "ACES of Finite Element and Life Prediction Models for Solder Joint Reliability" pp. 347-355 from DESIGN & RELIABILITY OF SOLDERS AND SOLDER INTERCONNECTIONS, Editors R.K. Mahidhara et al., TMS.

2. ANSYS® 5.5, 1999. ANSYS, Inc..

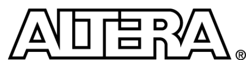
3. Darveaux, R., Heckman, J. and Mawer, A, 1998. Effect of test board design on the 2nd level reliability of a fine pitch BGA package, Surface Mount International Conference and Exposition. Proceedings, p. 807, pp. 105-11.

4. Mawer, A.; Cho, D.; Darveaux, R., 1996. The effect of PBGA solder pad geometry on solder joint reliability SMI. Surface Mount International. Advanced Electronics Manufacturing Technologies. Proceedings of The Technical Program, p. 2 vol. 826, pp. 127-35.

Acknowledgments:

Authors are very thankful to Ahmer Syed of Amkor for providing valuable advice for finite element modeling.

© SEMI 2000



101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
http://www.altera.com

Copyright © 2006 Altera Corporation. All rights reserved. Altera, The Programmable Solutions Company, the stylized Altera logo, specific device designations, and all other words and logos that are identified as trademarks and/or service marks are, unless noted otherwise, the trademarks and service marks of Altera Corporation in the U.S. and other countries. All other product or service names are the property of their respective holders. Altera products are protected under numerous U.S. and foreign patents and pending applications, maskwork rights, and copyrights. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera Corporation. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.