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A Jitter Estimation Method for Cascaded, Programmable Phase- Locked Loops

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Abstract

In a phase-locked loop (PLL), it is critical to understand how reference clock noise affects the output quality, particularly in applications where PLLs are cascaded. That is, where the output of one PLL serves as the reference clock for another PLL. Traditionally, this problem is solved by qualitative analyses, rules of thumb, and simulation, all of which require confirmation with measurements. We present a characterization technique that quantifies and predicts the transfer of reference clock noise to the PLL output, without requiring a circuit model. We will present theory, data, and measurement correlations, as well as application examples.

Author Biographies

Dr. Daniel Chow is a senior member of technical staff in the characterization group at Altera Corporation. His responsibilities include testing and validation of high-speed components. Specifically, he is responsible for developing Altera's knowledge base on jitter measurement issues. Dr. Chow received his Ph.D. from the University of California, Davis.

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1. Background and Motivation

In typical phase-locked loop (PLL) applications, excessive noise in the PLL output is generally undesirable. Typically, the main concern surrounds timing noise, expressed as phase noise in the frequency domain or jitter in the time domain. Noise can come from internal components of the PLL or external sources such as the reference clock or power supply. From an application perspective, it is important to understand how reference clock noise affects the output quality of the PLL. This is particularly important in applications where PLLs are cascaded. That is, the output of one PLL serves as the reference clock for another PLL. In these applications, jitter accumulates from one PLL to another. If the jitter is excessive, a PLL at a later stage will lose its lock. Traditionally, there is no comprehensive method to characterize this type of noise transfer. Often, engineers rely on qualitative assessments, general rules of thumb, and simulations to tackle this challenge, all of which require confirmation with measurements.

The transceiver characterization team at Altera has developed a novel technique to quantitatively predict the transfer of noise from a reference clock to the PLL output without requiring a circuit model. The reference clock may be a laboratory clock generator, crystal oscillator, or another PLL. This methodology is immediately applicable to engineers concerned with noise issues in PLL applications.

2. PLL Noise Theory

Much research has been dedicated to the modeling of noise in PLLs [1, 2]. Figure 1 shows a PLL block diagram consisting of a reference clock, phase detector, charge pump, loop filter, voltage controlled oscillator (VCO), and loop divider. Under normal operation, the PLL output frequency (f_{Out}) is the product of the reference clock frequency (f_{Ref}) and the loop divider value. Typical models assume that every component in the PLL has an associated intrinsic noise power and gain. In closed loop operation, all of the intrinsic noise powers and gains interact to create the total noise at the PLL output.

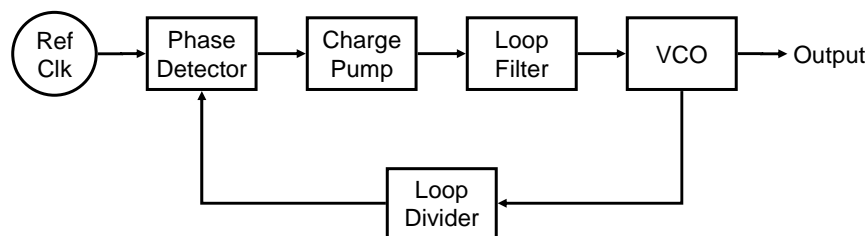


Figure 1: Block diagram for PLL components.

The intrinsic noise power and gain of the individual components are often difficult (if not impossible) to characterize. Some components can be simulated, but this still requires correlation with measurements. Therefore, it is extremely challenging to build an accurate PLL noise model from its components.

Since the primary concern in most applications is the jitter output of the PLL, we propose a method to predict PLL output jitter based on laboratory measurement and characterization of the PLL's intrinsic properties. The advantage of this method is that the PLL is treated as a system, rather than as a collection of individual components.

For a PLL in locked operation with small phase errors, the noise behavior of the components shown in Figure 1 can be lumped together to form a linear PLL noise transfer model, shown in Figure 2. The noise power of the reference clock is denoted as P_{Ref} . The noise power of the PLL output is P_{Out} . All components inside the PLL collectively behave as an intrinsic system noise power (P_{Int}) and a closed-loop gain (G). Note that P_{Ref} , P_{Int} , P_{Out} , and G are all frequency-dependent parameters.

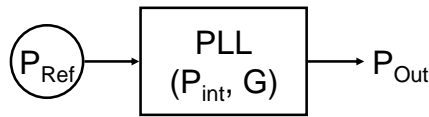


Figure 2: Block diagram for PLL system noise model.

From this model, for any frequency, the PLL output noise power is simply the reference clock noise power amplified by the closed-loop gain plus the PLL intrinsic noise power, expressed as

$$P_{Out}(f) = P_{Ref}(f) \times G(f) + P_{Int}(f). \quad \text{Eq. 1}$$

The noise powers P_{Ref} and P_{Out} correspond to the stimulus and response of the system. Both parameters are measurable as phase noise spectra. The intrinsic parameters P_{Int} and G can be inferred by manipulating the stimulus and observing response of the PLL. This model quantifies the PLL intrinsic noise and noise transfer without any knowledge of the circuits.

3. Proposed Methodology and Data

For the lumped-component linear noise model, knowledge of P_{Int} and G allows the prediction of P_{Out} for any P_{Ref} . The two quantities P_{Int} and G can be found by careful manipulation of P_{Ref} and observation of P_{Out} using a bench-top characterization setup shown in Figure 3.

The PLL under test is a transmitter (Tx) PLL for a transceiver device. The reference clock generator is an Agilent 81134A externally clocked by an rf generator (Agilent 8257D) to minimize intrinsic noise. Controlled levels of phase noise are added to the reference clock by applying white voltage noise (NoiseCom UFX 9836) to the time delay input of the clock generator. The time delay converts input voltages into timing offsets in the clock signal with a ratio of 250 ps/V and a bandwidth of 200 MHz. Table 1 shows the relevant settings of the Tx PLL.

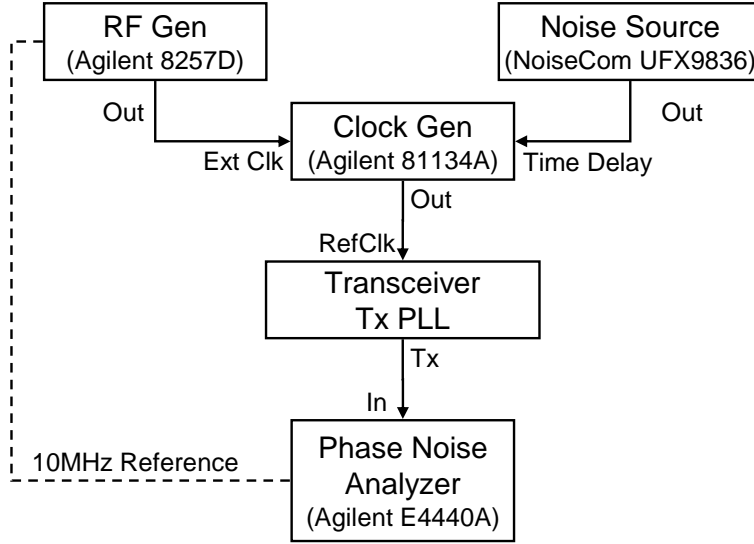


Figure 3: Setup for characterization of PLL intrinsic noise power and closed-loop gain.

Parameter	Value
f_{Ref}	159.375 MHz
Loop Divider	20
f_{Out}	3.1875 GHz
Tx Data Rate	6.375 Gb/s

Table 1: Tx PLL operational settings.

The reference clock generator with added phase noise is applied to the reference clock input of the Tx PLL. The Tx PLL output drives a high-speed Tx buffer configured to generate a clock-like “1010” pattern such that the transition edges reflect the timing of the Tx PLL output due to the half-rate architecture. The Tx buffer output is measured with a phase noise spectrum analyzer (Agilent E4440A). We maximized measurement accuracy and eliminated wander by configuring the spectrum analyzer to share a 10-MHz time base reference with the rf generator.

From Eq. 1, the P_{Ref} has a linear relationship with the P_{Out} , which was observed by varying the levels of noise added to the reference clock and measuring the phase noise of the PLL output at the Tx. Figure 4 shows the measured phase noise spectra for P_{Ref} and P_{Out} with varying levels of added noise. For simplicity, only selected noise levels are shown. Both sets of data show the same trend of phase noise increasing with added noise.

Phase noise was measured for frequency offset $f_{off} = 100 \text{ kHz} - 100 \text{ MHz}$. For $f_{off} < 100 \text{ kHz}$, the intrinsic noise of the Agilent 8257D is dominant in the setup, effectively masking the relationship expected in Eq. 1. The upper cut-off value of $f_{off} = 100 \text{ MHz}$ is sufficient to capture the PLL’s in-band noise.

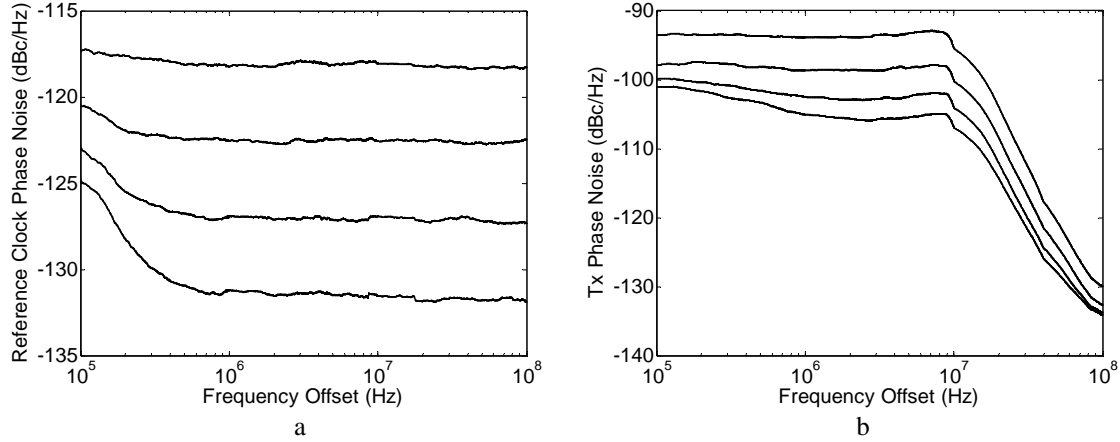


Figure 4: Phase noise measurements for a) reference clock and b) Tx PLL output for selected varying levels of added noise.

Phase noise is typically expressed in a logarithmic scale given by

$$L(f_{off}) = 10 \log \left(\frac{P(f_{off})/\text{Hz}}{P_C} \right), \quad \text{Eq. 2}$$

where f_{off} is the frequency offset relative to the carrier frequency, L is phase noise in units of dBc/Hz, P is the single side-band power, and P_C is the power of the carrier signal. For analysis using Eq. 1, all phase noise values are converted to a linear scale as a ratio of power density of the single side-band to the power of the carrier. That is,

$$\frac{P(f_{off})/\text{Hz}}{P_C} \quad \text{Eq. 3}$$

with units of 1/Hz.

For every f_{off} , P_{Out} is plotted against P_{Ref} . From Eq. 1, a linear fit of P_{Out} vs. P_{Ref} gives a slope and intercept corresponding to G and P_{Int} , respectively. Figure 5 shows the least squares linear fit of P_{Out} vs. P_{Ref} for $f_{off} = 8.6$ MHz with an intercept of $P_{Int} = 1.41 \times 10^{-11} \text{ Hz}^{-1}$ (or -108.5 dBc/Hz).

For small phase errors, the behavior of the PLL is purely linear, with G as the simple slope of the fit. However, for large phase errors, the PLL deviates from linearity. As a result, G at high power requires a small correction factor. The value of G for $P_{Ref} < 0.251 \times 10^{-12} \text{ Hz}^{-1}$ (or -126 dBc/Hz) is 225.18 (or 23.5 dB) and G for $P_{Ref} > 0.251 \times 10^{-12} \text{ Hz}^{-1}$ (or -126 dBc/Hz) is 318.37 (or 25 dB). For this f_{off} , the gain at high P_{Ref} differs from the gain at low P_{Ref} by $\sim 20\%$. The division between low P_{Ref} and high P_{Ref} is determined by least squares fitting.

Figure 5 also shows the 95% ($\pm 2\sigma$) prediction intervals [3, 4] associated with the fit. For $P_{Ref} < 0.251 \times 10^{-12} \text{ Hz}^{-1}$ (or -126 dBc/Hz), the prediction interval is $\pm 4.02 \times 10^{-12} \text{ Hz}^{-1}$. For $P_{Ref} > 0.251 \times 10^{-12} \text{ Hz}^{-1}$ (or -126 dBc/Hz), the prediction interval is $\pm 51.8 \times 10^{-12} \text{ Hz}^{-1}$.

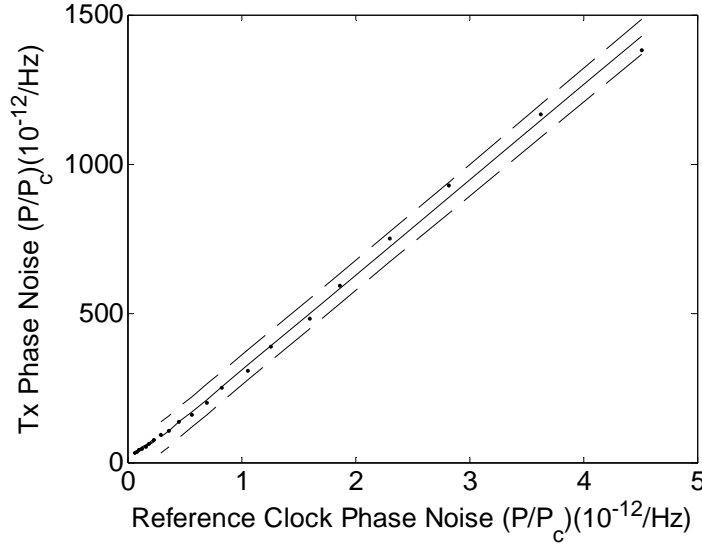


Figure 5: Tx phase noise vs. refclk phase noise at $f_{off} = 8.6 \text{ MHz}$. Dots represent data, the solid line is a linear fit, and the dashed lines are 95% ($\pm 2\sigma$) prediction intervals.

The plotting and fitting of P_{Out} vs. P_{Ref} is repeated for every f_{off} in the phase noise spectra, resulting in P_{Int} and G as functions of f_{off} . For the Tx PLL data shown in Figure 4, the P_{Int} and G from 100 kHz to 100 MHz are shown in Figure 6 in logarithmic scales.

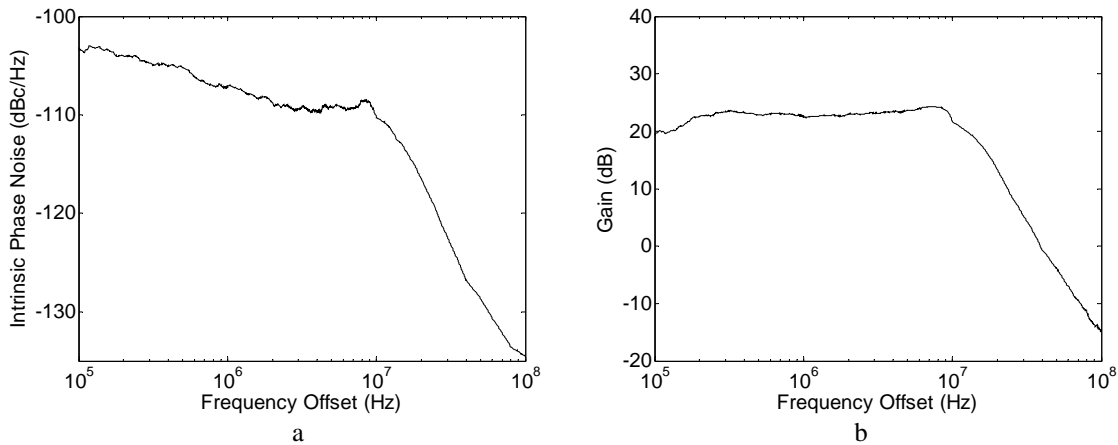


Figure 6: Tx PLL a) intrinsic phase noise and b) gain from 100kHz to 100MHz.

P_{Int} and G have a -3 dB corner and roll-off similar to the jitter transfer function of the Tx PLL due to the loop filter. The low gain at high frequency indicates that reference clock noise can only impact the Tx PLL output within the loop bandwidth. With P_{Int} and G known, the PLL output phase noise power can be determined for any reference clock phase noise power.

4. Jitter Estimation Results

In Section 3, we found the intrinsic noise power P_{Int} and gain G for a Tx PLL. With this information, we can predict the output noise of this PLL for any reference clock and correlate to laboratory measurement. Figure 7 shows the measured phase noise spectra for two reference clock generators: Agilent 81134A and Agilent 8131A. Across all frequencies, the Agilent 8131A has higher phase noise than the Agilent 81134A.

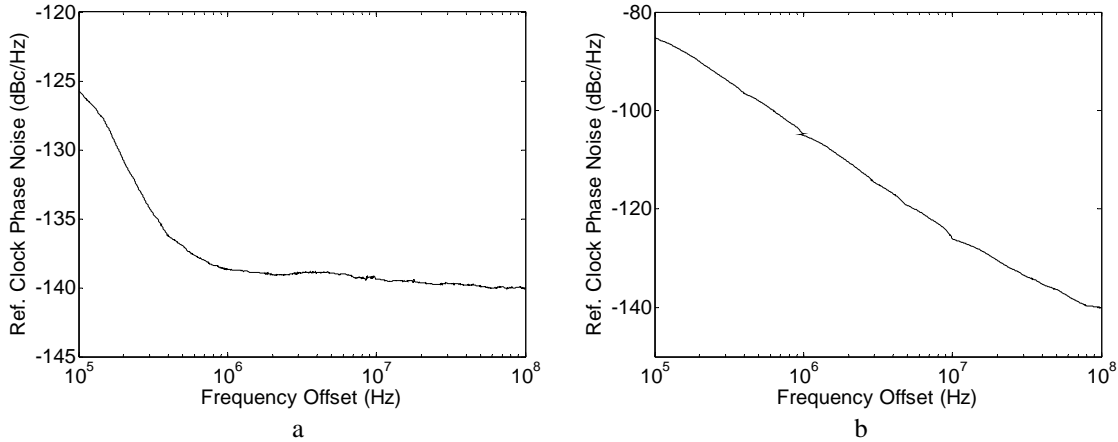


Figure 7: Phase noise spectra for a) Agilent 81134A and b) Agilent 8131A clock generators.

Using Eq. 1 in conjunction with the P_{Int} and G determined in Section 3, we predict P_{Out} for the case of Agilent 81134A as the reference clock, shown in Figure 8a. The uncertainty of the prediction is given by the 95% prediction interval obtained from the fit of P_{Ref} vs. P_{Out} at each f_{Off} . Specifically, the prediction interval is shown in Figure 5 for $f_{Off} = 8.6$ MHz. Figure 8b shows the measured phase noise at the Tx output. The measured P_{Out} falls within the 95% prediction interval, demonstrating good correlation between prediction and measurement.

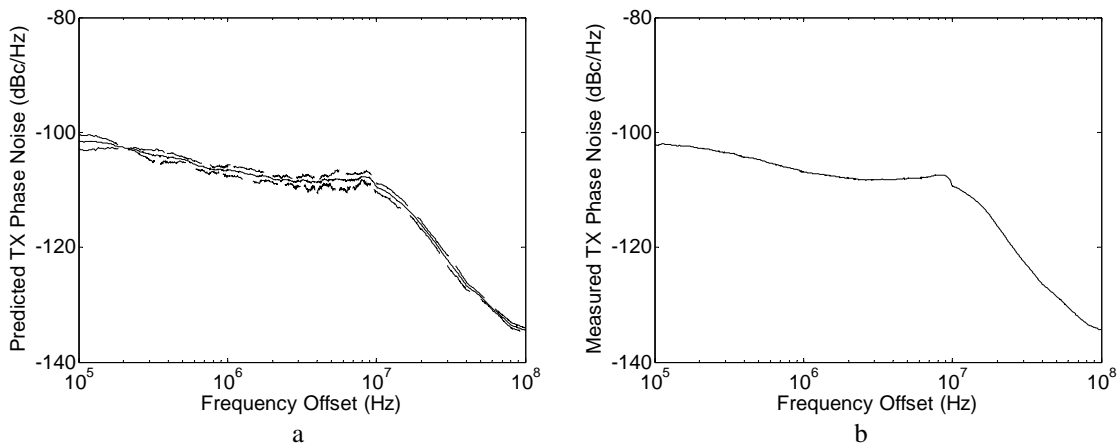


Figure 8: Tx PLL a) phase noise prediction (solid line), 95% prediction intervals (dashed lines), and b) measurement for Agilent 81134A as reference clock.

For Agilent 8131A as the reference clock, Figure 9a shows the predicted P_{Out} with associated 95% prediction intervals. Figure 9b shows the measured P_{Out} . Again, the measured P_{Out} falls within the 95% prediction interval except near $f_{Off} = 100$ kHz, demonstrating good overall correlation between prediction and measurement.

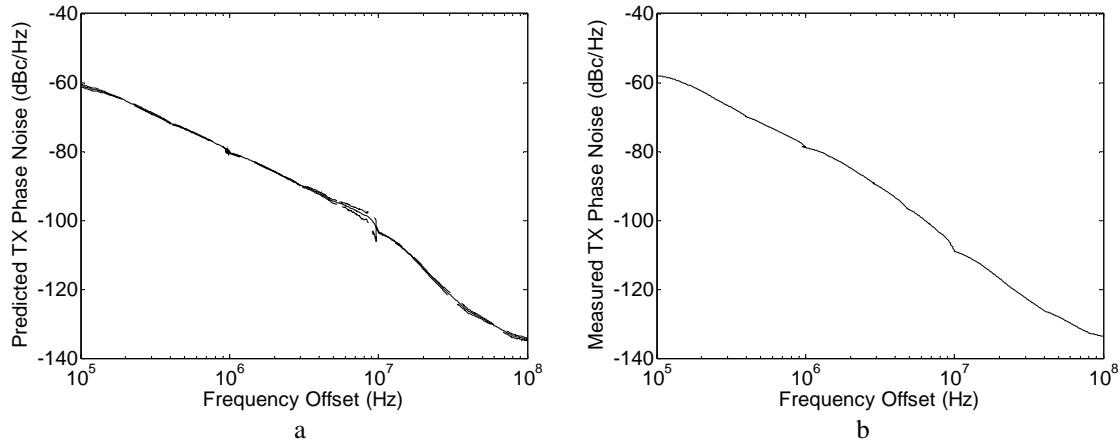


Figure 9: Tx PLL a) phase noise prediction (solid line), 95% prediction intervals (dashed lines), and b) measurement for Agilent 8131A as reference clock.

The predicted phase noise spectra can be integrated to give rms jitter values. Furthermore, the jitter values can easily be expressed with different reference frames such as phase jitter, period jitter, and/or cycle-to-cycle jitter by applying the appropriate transfer function [5]. Table 2 shows the jitter values integrated from the predicted and measured phase noise spectra over the frequency range of 100 kHz to 100 MHz for Agilent 81134A as the reference clock. Table 3 shows the jitter values for Agilent 8131A as the reference clock. The values of period and cycle-to-cycle jitter are extremely small (on the order of femtoseconds) because the respective transfer functions are high pass filters that strongly suppress phase noise from 100 kHz to 100 MHz [5].

Jitter (rms, 100 kHz–100 MHz)	Predicted	Measured
Phase	1.12 ± 0.12 ps	1.15 ps
Period	30.4 ± 2.4 fs	30.6 fs
Cycle-to-cycle	2.9 ± 0.15 fs	2.92 fs

Table 2: Predicted and measured Tx jitter values for Agilent 81134A as reference clock.

Jitter (rms, 100 kHz–100 MHz)	Predicted	Measured
Phase	23.1 ± 0.6 ps	31.2 ps
Period	55.9 ± 3.5 fs	47.9 fs
Cycle-to-cycle	3.02 ± 0.14 fs	3.14 fs

Table 3: Predicted and measured Tx jitter values for Agilent 8131A as reference clock.

We successfully demonstrated a novel methodology for predicting PLL output phase noise and jitter for any given reference clock phase noise. One immediate application of this technique is to determine the impact of reference clock noise on the Tx output phase noise and jitter. This capability can address issues regarding the necessity and cost for clean reference clocks in transceiver applications.

5. Cascaded PLLs

Another significant application of this technique is in the analysis of noise transfer in cascaded PLLs. That is, the output of one PLL serves as the reference clock for another PLL as shown in Figure 10. The parameters P_{Int1} , G_1 , P_{Int2} , and G_2 are the intrinsic noise powers and gains for first-stage PLL (PLL1) and second-stage PLL (PLL2), respectively.

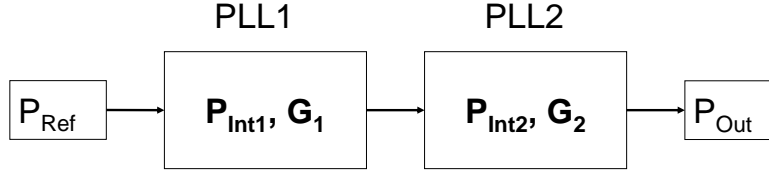


Figure 10: Block diagram for cascaded PLLs.

In these cases, the reference clock noise power (P_{Ref}) is transferred through PLL1 and PLL2, amplifying by G_1 and G_2 and accruing P_{Int1} and P_{Int2} along the way. Applying Eq. 1 to Figure 10, the output noise power of cascaded PLLs is given by

$$P_{Out}(f) = [P_{Ref}(f) \times G_1(f) + P_{Int1}(f)] \times G_2(f) + P_{Int2}(f) . \quad \text{Eq. 4}$$

We demonstrate this application by characterizing cascaded PLLs consisting of a general-purpose PLL (GPLL) driving the Tx PLL described in Sections 3 and 4. The relevant parameters for both PLLs are shown in Table 4.

	Parameter	Value
GPLL	f_{Ref1}	15.9375 MHz
	Loop Divider	10
	f_{Out1}	159.375 MHz
Tx PLL	f_{Ref2}	159.375 MHz
	Loop Divider	20
	f_{Out}	3.1875 GHz
	Tx Data Rate	6.375 Gb/s

Table 4: GPLL and TX PLL operational settings.

The GPLL's P_{Int} and G is first characterized independently using the method described in Section 3. The results are shown in Figure 11. Comparison with Figure 6 shows that the GPLL has comparable P_{Int} and G with the Tx PLL, but with a lower loop bandwidth.

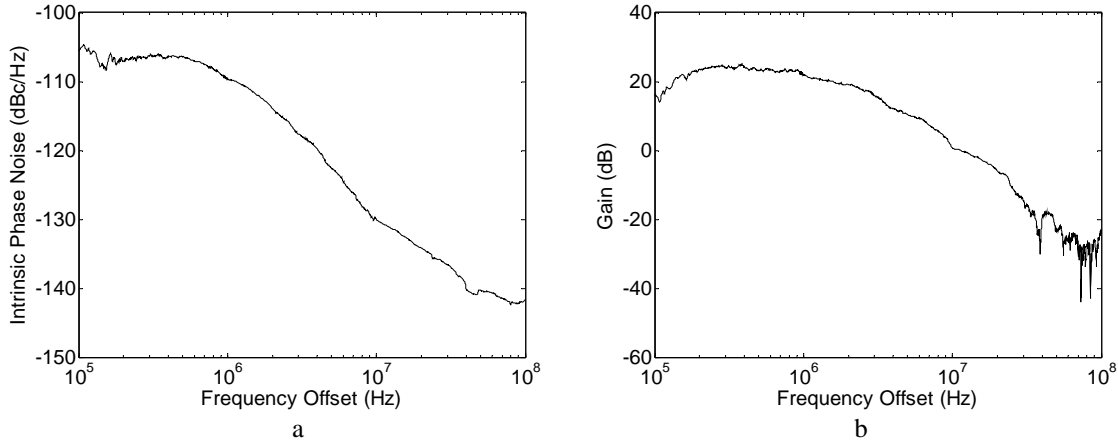


Figure 11: GPLL a) intrinsic phase noise and b) gain for GPLL from 100kHz to 100MHz.

In the cascaded PLL setup, an Agilent 81134A served as the reference clock for the GPLL. The output of the GPLL was configured to serve as the reference clock for the Tx PLL as shown in Figure 10. We predict the output phase noise of the cascaded PLLs using Eq. 4 (Figure 12a) and compare with measurement (Figure 12b). The prediction and measurement show good correlation across frequency.

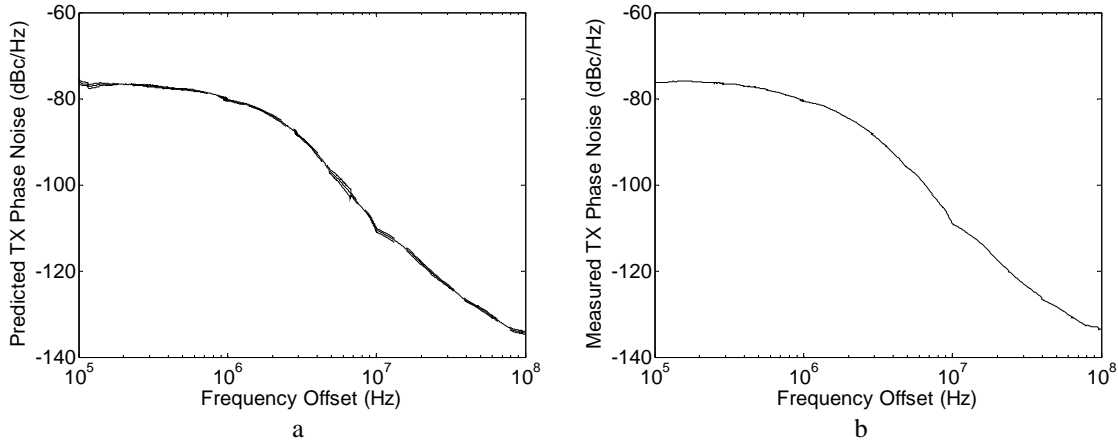


Figure 12: Cascaded PLLs a) phase noise prediction (solid line), 95% prediction intervals (dashed lines), and b) measurement.

The phase noise spectra are integrated to give jitter values (Table 5). The jitter values also show good correlation.

Jitter (rms, 100 kHz–100 MHz)	Predicted	Measured
Phase	11.2 ± 0.2 ps	11.3 ps
Period	43.6 ± 0.5 fs	45.8 fs
Cycle-to-cycle	2.85 ± 0.1 fs	3.11 fs

Table 5: Predicted and measured Tx jitter values for cascaded PLLs.

We demonstrated our PLL phase noise and jitter estimation methodology for cascaded PLLs with good correlation of results between prediction and laboratory measurements.

6. Conclusions

The transceiver characterization group at Altera has developed a novel methodology for determining PLL output phase noise for any given reference clock without the need for knowledge of the specific circuits. The reference clock can be a laboratory clock generator, crystal oscillator, or another PLL. The theory is derived from existing linear PLL noise theories. The parameters of this model are determined by characterization of the PLL.

We demonstrated this technique on a general-purpose PLL and a transceiver PLL. The simulation results predicted a PLL output phase noise that shows excellent correlation with laboratory measurements. Furthermore, the phase noise spectra can be integrated to give jitter values, expressed as phase jitter, period jitter, and cycle-to-cycle jitter.

This methodology is immediately applicable to any PLL application where output noise is of concern. One example is the cost-benefit selection of reference clock oscillators. Another example is the noise transfer in cascaded PLLs.

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