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Study of Fundamental Limit and Packaging Technology Solutions for 40-Gbps Transceiver Package Design

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Abstract

This paper discusses the fundamental constraints of current packaging technology and how they affect the performance of multichannel 10-Gbps FPGAs. FPGA packages act as interconnects between dies and system boards. While IC chips take advantage of Moore’s law for dimension and cost reduction, system boards traditionally have not. From design optimization practice, we conclude that the inherent dimension mismatch among layout features that link the die to boards hampers the upper limit of bandwidth. To overcome these constraints, we propose advanced technologies such as coreless, fine-pitch packages and demonstrate extended 40-GHz bandwidth, making performance comparable to state-of-the-art microwave devices.

Author Biographies

Dr. Hong Shi is Packaging Design Engineering Manager at Altera Corporation. Dr. Shi’s responsibilities include developing the strategy for high-density and high-performance FPGA packaging, simulating system-level electrical performance, and establishing chip-package-board interconnect co-design capability. He has published over 40 technical papers in areas of optoelectronics, microwave circuits, and digital circuit packages.

Xiaohong Jiang is Member of Technical Staff at Altera Corporation, focusing on high-performance package electrical design and technology development. Prior to Altera, she was with Lucent Technologies Inc. and BigBear Networks to work on 40-Gbps transponders. Her interests involve electromagnetic field analysis and modeling of RF/microwave circuits and components, signal integrity, and system-level simulations.

Dr. John Yuanlin Xie has more than 13 years of semiconductor industry experience. He has been with Altera Corporation for eight years, and currently serves as senior manager in Altera's package technology department. Dr. Xie's interests include IC packaging technology, substrate material and process, package design engineering, and silicon-package-PCB co-design, manufacturing, and solution integration.

I. Introduction

As devices and systems rapidly increase in complexity, new packaging technologies are essential to meet the demand for more integrated sizes, as well as more robust functionality and reliability. The required bandwidth demands careful interconnect designs for successful signal propagation. The FPGA package can act as an interconnect between the die and the system board in a wide variety of applications, such as computer networking, data networking, instrumentation, video processing, digital signal processing, or any other applications that use programmable or reprogrammable logic .

While IC chips take advantage of Moore's law in dimension and cost reduction, system boards traditionally have not. Figure 1 shows feature density shrinkage for silicon, package, and PCB respectively compared with Moore's law (top chart). Also shown is the dimension history of IC line width, BGA ball pitch, package substrate line width, and PCB line width. The clear message from these two charts is the mismatch of feature dimension reduction.

The package as interconnect between silicon die and system board is manufactured with intrinsic geometry mismatch. For example, C4 bump typically has ~100-um diameter and ~200-um pitch, which are to facilitate IC dimensions. On the second-level interface where the package meets the PCB, mostly used ball diameter and pitch are 550 um and 1 mm respectively, which is as much as 5X larger than bumps. While bump pitch is following IC feature shrinkage, PCB technology has limited itself in slower feature reduction pace. As a result, the package becomes not only the electrical interconnect, but also a geometry transformer that progressively increase the dimension from bump on its top layer to ball on bottom layer.

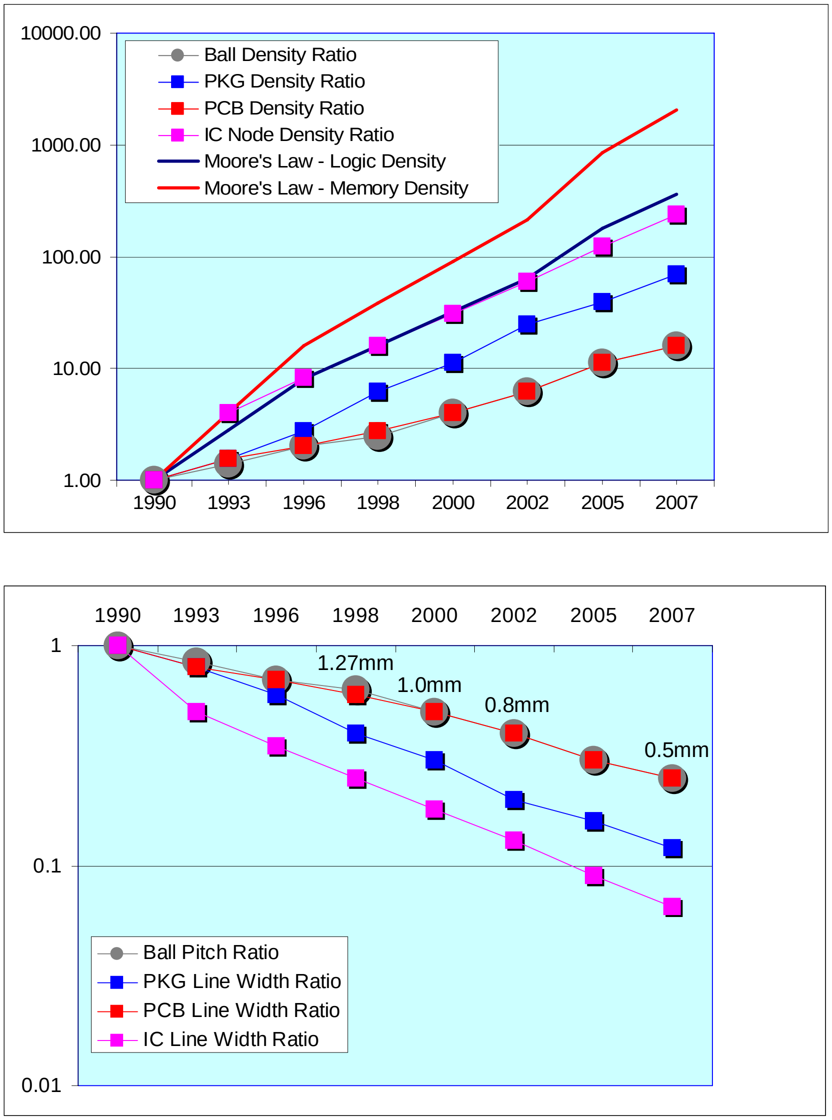

Figure 1. Feature density shrinkage for silicon, package, and PCB compared to Moore's Law (Top). Dimension history of IC line width, BGA ball pitch, package substrate line width, and PCB line width. (Bottom)

Multi-layer BGA packages show the increased flexibility of high-I/O-count routing and power/ground planes management. Successful signal integrity management requires good impedance matching, control of crosstalk noise, and careful engineering of return loss and insertion loss of the transmission paths. The previous focus was on optimizing the horizontal transmission lines in the multi-layer packages. 50Ω single-ended and 100Ω differential drive impedance control of horizontal microstrip or stripline were carefully managed to meet the signal propagation requirements. However, optimization of vertical transitions between micro vias and plated through holes (PTH) and BGA balls, as well as PTH/BGA cross-coupling to the ground planes, were often ignored although it becomes critical in complex multi-layer packages operating in 10-Gbps or faster systems. Therefore, there are significant discontinuities and loss along these vertical components, even if horizontal transmission lines are well designed.

In this paper, we will first focus efforts on vertical transition improvement and strategies, followed by fundamental limit analysis to impedance control arising from package's feature geometry constraints. In the final section, advanced packaging techniques are investigated for organic package designs to achieve 40 Gbps and beyond.

II. Design Optimization of High-Speed Multi-Layer BGA Packages

In this section, our study is on optimization to vertical structure designs. The focus is to improve impedance discontinuity by engineering geometry of layout feature in via and ball transitions. Further enhancement is extended into the broad frequency range, making the return loss 10+ dB less than original design over 25-GHz bandwidth.

Package Physical Structure

A typical multi-layer BGA package contains a variety of elements from bump (or wire) to ball: flip chip bumps or wire bonds, transmission lines, micro vias, plating through holes, and BGA balls, as illustrated in Figure 2. Horizontal structures are transmission lines designed as either microstrip or stripline. Vertical transition portion includes bump to via, via to via, via to ball, and ball to PCB vias.

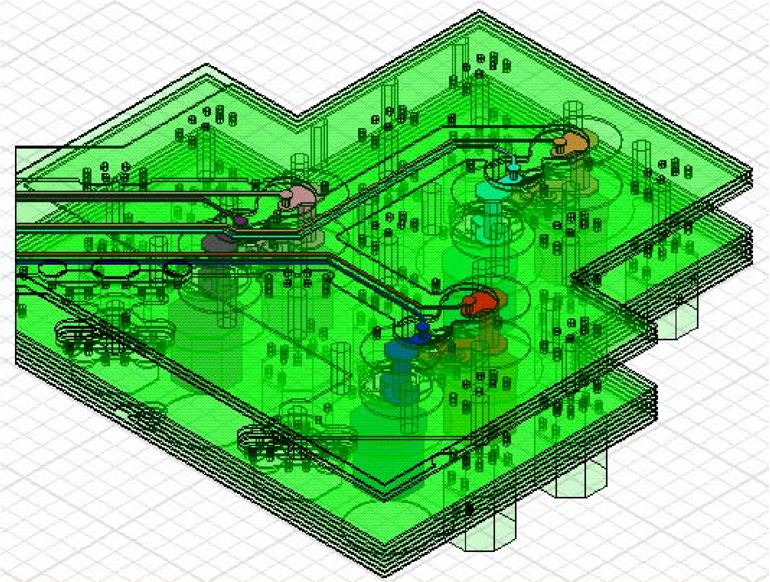

Figure 2. Illustrative BGA package structure (Flip chip bump or wire bond is not drawn)

Optimized Package Design

While impedance matching of horizontal transmission lines is relatively easy to understand and control, more attention is needed for vertical transitions, cross coupling, and impedance control from layer to layer. Although package substrate layer thickness is very small compared to the length of horizontal transmission lines, when the number of layers significantly increases, the impedance matching of micro vias and PTH becomes non-trivial, especially under the stringent process constraints. Figure 3 shows the impedance profile of a transmission path in a flip chip package from bump to BGA ball before and after optimization.

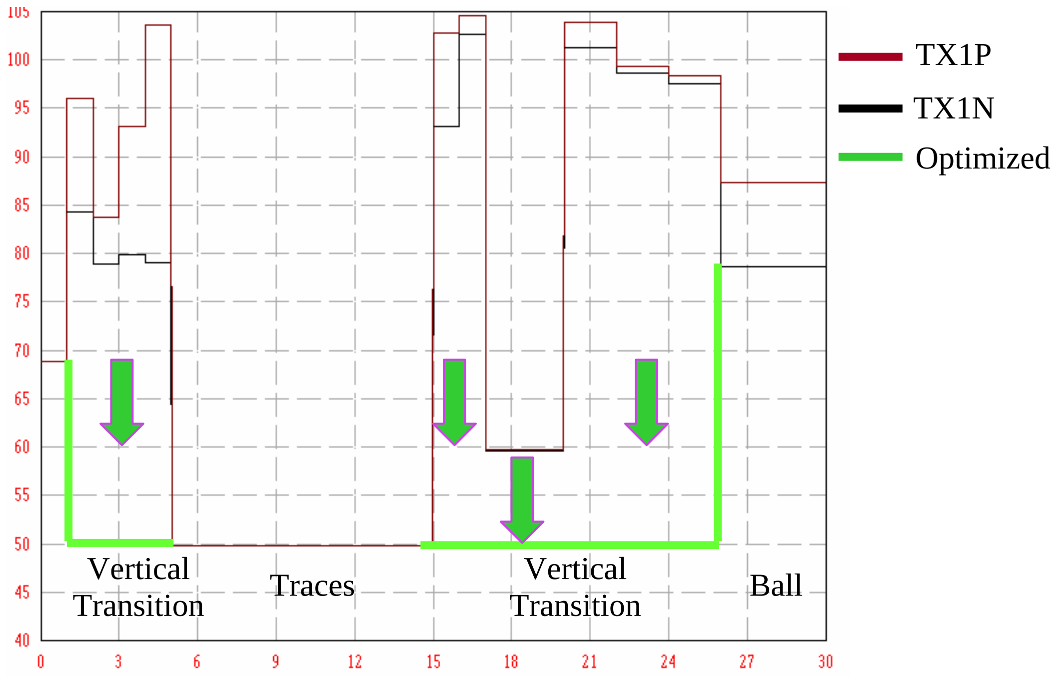

Figure 3. Impedance profile of a single-ended pair in multi-layer BGA package vertical transition (The green curve indicates the optimized transition with close to 50Ω characteristic impedance.). X-axis stands for layer transition in absolute unit. Y-axis is impedance in terms of Ohms.

The trace portion has nearly perfect 50Ω characteristic impedance, whereas the vertical dimension can have as much as 105Ω and is single-ended. The optimization goal is to engineer the vertical portion to yield characteristic impedance as close to 50Ω as possible. It is important to note that the impedance of the BGA ball remains largely unchanged. Patterns of I/O to surrounding ground ball may lower impedance, but the patterning effect is limited by the smallest ball diameter and pitch allowed, in this case 0.5 mm and 1 mm. This clearly demonstrates why current packaging technology has limitations on achieving higher bandwidth with improved return loss.

Figure 4 compares the performance of two designs with original and optimized vertical transition. Within layout design constraints, optimized design with well-matched vertical transition can improve the comprehensive transmission performance by up to 10 dB. Notice that the reflection is minimized drastically in the bottom insertion loss (S21) chart.

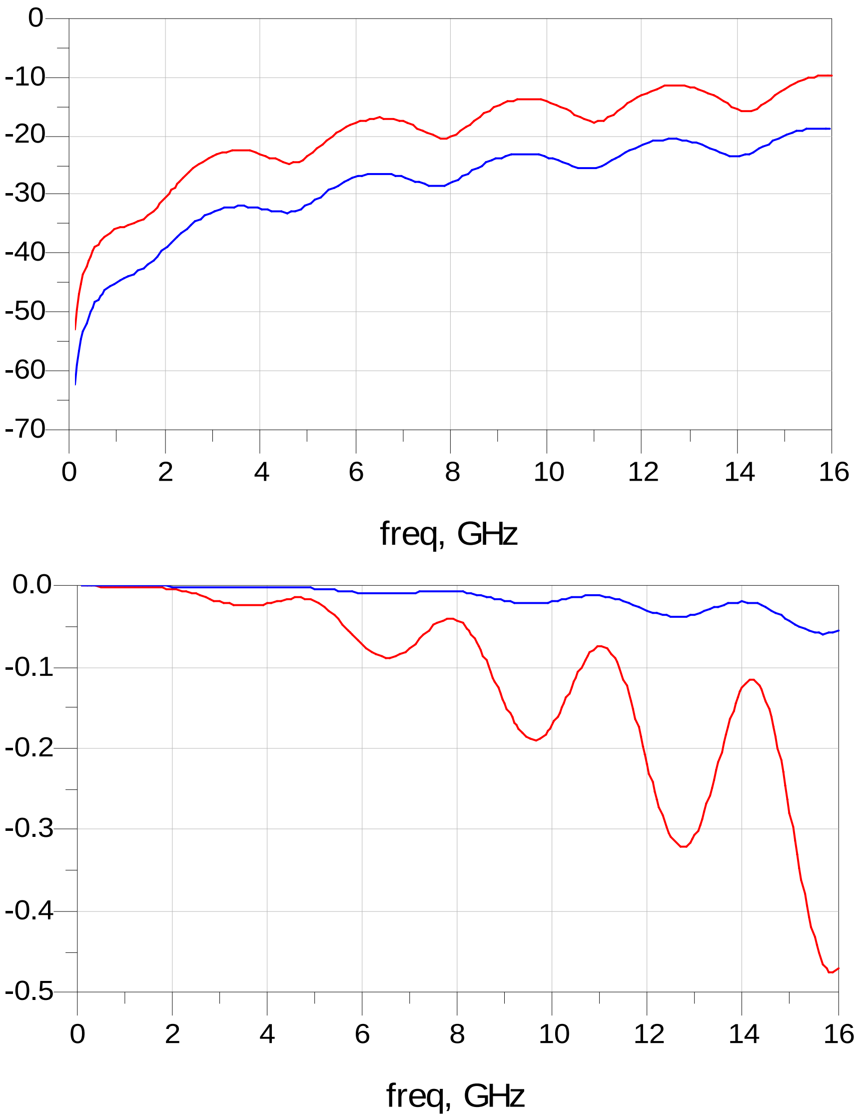

Figure 4. Comparison of multi-layer BGA packages before and after vertical impedance matching (Top is return loss (S11) and bottom is insertion loss (S21)

An important concept is to achieve broadband impedance match. Mathematically, one can always achieve 50Ω characteristic impedance by matching local inductive effect, *L*, to local capacitive effect, *C*. However, the bandwidth over which 50Ω is maintained depends on not only *L* and *C* values, but also on reducing parasitics that cause the impedance to deviate from the desired value in the high-frequency range. This technique is a combination of impedance control and parasitics control, often depending on frequency range for the most enhancements. Figure 5 shows two enhancement cases that demonstrate the desired S11 performance for different purposes.

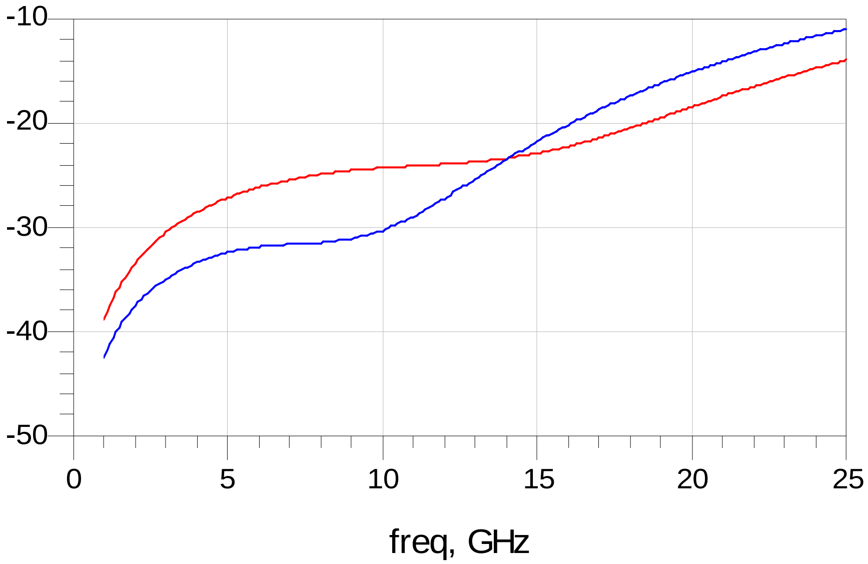

Figure 5. Two cases show return loss improvement for broad frequency (red) and specific frequency area (blue).

Figure 5 shows that the physical structure can be engineered to either achieve good return loss over a broad range (red curve), superior return loss in a narrow frequency range (blue curve), or anything between. For 10-Gbps applications, return loss (S11) over broad range is preferred while narrow band enhancement is beneficial for 3.25 Gbps.

III. New Packaging Technology to Meet 40-Gbps Challenge

Even when the horizontal and vertical transmissions are well optimized, the bandwidth for conventional multi-layer BGA packages is inherently restricted due to the dimension mismatch and associated parasitic reduction constrains. In most 10-Gbps applications, designers can use optimized multi-layer packaging techniques. Die pin capacitance should also be considered for overall channel performance.

Figure 6 demonstrates high-speed channel compliance with the 10-Gbps XFI interface standard for differential return loss, which includes the effect of package designs as well as die capacitance. The results demonstrate performance degradation as die capacitance increases with package design as baseline. Continuous high-speed channel enhancement for packages is under consideration for next generation 40-Gbps operation.

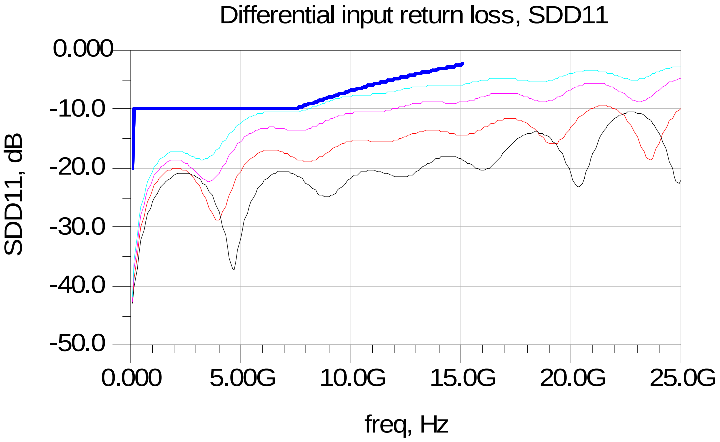

Figure 6. Performance compliance for 10-Gbps XFI for different package and die designs
(The blue boundary illustrates XFI interface specifications for the entire system. The lowest curve is the package only, and the remaining curves measure the pin capacitance for different die.)

Further technical considerations include the paradigm change for material, process, and design. To lower costs, organic materials will remain mainstream in FPGA and most ASIC package designs. Designs have been optimized over years, including the vertical transition enhancement discussed earlier in this paper. The next phase is process modification. In this paper, we consider coreless technology and M-type packages with 0.5-mm pitch. The goal is to reduce dominant geometry mismatch inside the package, plated through hole and solder balls.

Figure 7 compares the transition from micro-via, PTH to ball for a conventional package and a coreless package. An average of 10-dB return loss improvement is achieved over the 25-GHz bandwidth in the coreless structure. This advanced package is appropriate for high-performance broadband applications. The final comparison is in time domain. Our simulations compare 40-Gbps eye diagrams from three generations of packaged devices, as shown in Figure 8. The eye diagram demonstrates inadequate bandwidth and related jitter degradation. The new packaging technique gives increased eye opening and less jitter. It does not include die capacitance.

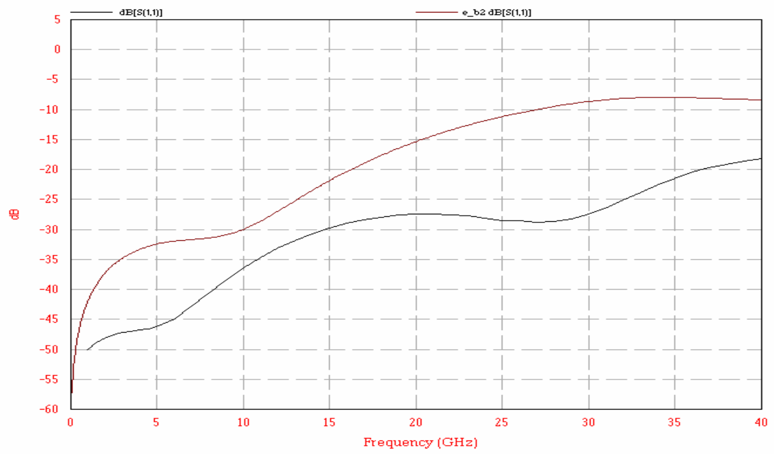

Figure 7. Comparison of micro-via, PTH to ball transition of conventional (upper curve) vs. next-generation packages (lower curve)

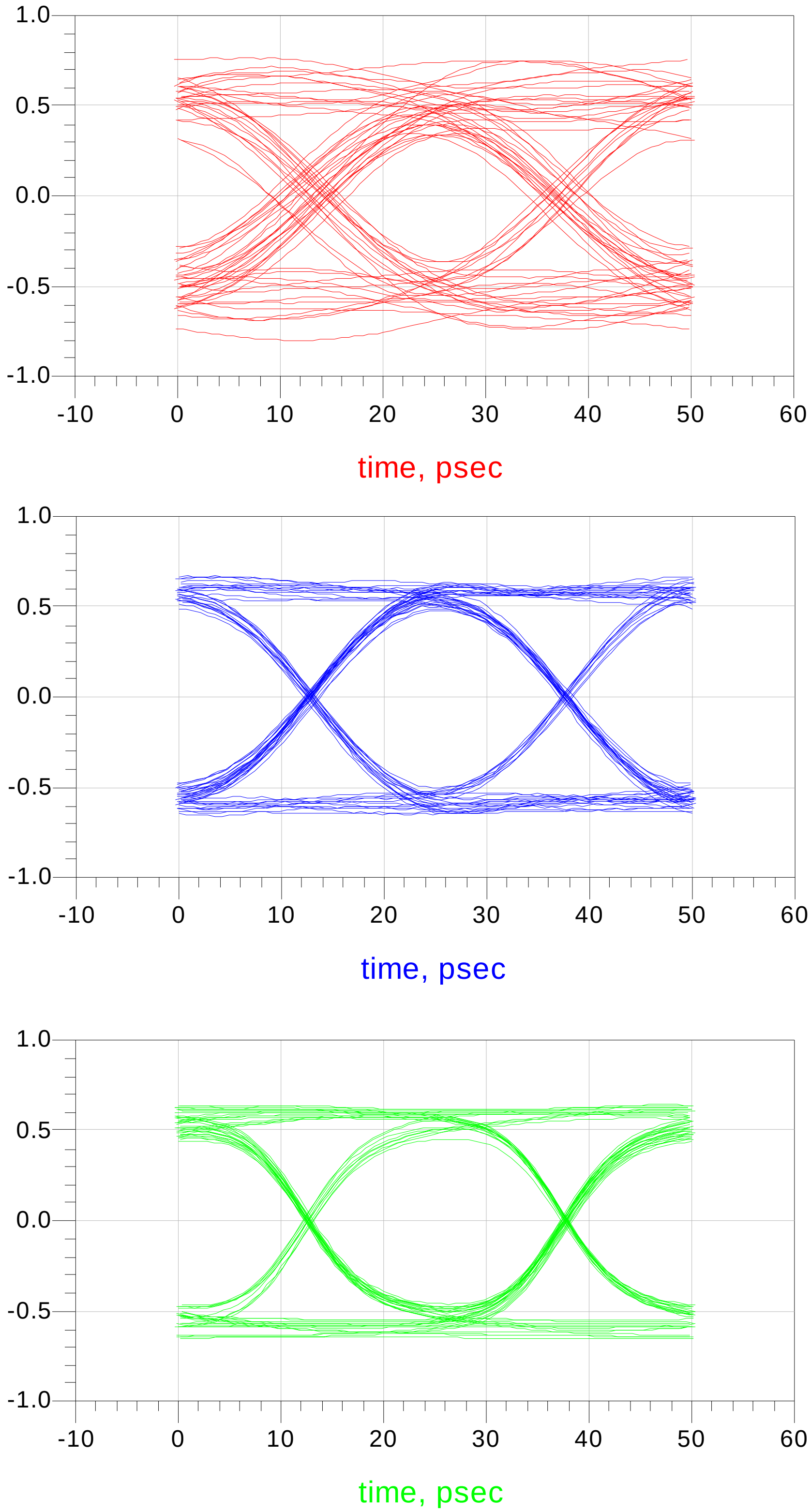

Figure 8. 40-Gbps eye diagrams for original unoptimized packages (Top), optimized with vertical transitions (Middle), and new packaging technology (Bottom).

IV. Summary

In summary, a conventional multi-layer BGA package containing flip-chip bumps or wire bonds, transmission lines, micro vias, plated through holes, and BGA balls are simulated before and after vertical transition optimization. A proposed coreless package with fine pitch uses micro vias to replace the plated through holes option, and uses a 300-µm diameter ball with 500-µm pitch. A comparison of the proposed coreless package to the conventional package before and after the vertical optimization reveals the fundamental limitation for high-speed design residing in intrinsic geometry diversity. This limitation results from an unparallel feature shrinkage path for die, package, and PCB. An improvement of approximately 15 dB can be achieved after the vertical transition is optimized in the conventional BGA package, while a much broader bandwidth can be obtained with 40-GHz applications in a coreless fine-pitch package.

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