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Process and Temperature Variations on Electrical Parameters of Wire-Bond BGA Packages: an Impact Analysis Using Simulation-Based DOE Methodology

Hui Liu, Altera Corporation
hliu@altera.com

Hong Shi, Altera Corporation
hshi@altera.com

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Abstract

This paper describes the impact of process and temperature variations on the electrical parameters of a FPGA wire-bond ball-grid array (BGA) package, using analysis from a simulation-based, two-level, fractional factorial design of experiment (DOE) methodology. Nine design factors are chosen to cover material properties, package geometries, and simulation setup. Eight design responses include self-inductance, self-capacitance, mutual inductance, mutual capacitance, DC resistance, AC resistance, impedance, and propagation delay. Linear regression models are built for each DOE response for electrical performance variation prediction. A simulation using a 3D quasi-static electromagnetic solver generates DOE data.

Author(s) Biography

Hui Liu holds a MS in electrical engineering from the University of Washington, Seattle. Liu is a member of the technical staff in the packaging technology department at Altera Corporation. Liu specializes in signal integrity, power integrity, and timing integrity analysis in high-speed and high-bandwidth FPGA package design and applications.

Dr. Hong Shi is technical lead for the packaging technology department at Altera Corporation. As manager of the packaging group's electrical design team, Dr. Shi's responsibilities include developing the strategy for high-density and high-performance FPGA packaging, simulating system-level electrical performance, and establishing chip-package-board interconnect co-design capability. Before joining Altera, Dr. Shi worked at HP and Agilent Technologies, where he was project leader for Agilent's first 40-Gbps digital communications analyzer module. He has published over 30 technical papers in the areas of optoelectronics, microwave circuits, and digital circuit packages. Dr. Shi obtained his BSEE from Xi'an Jiaotong University, MS in physics from DePaul University, and PhD in electrical engineering from CREOL College of Optics at the University of Central Florida.

Introduction

Electrical behaviors of FPGA wire-bond BGA packages are complicated. Signal integrity analysis in FPGA applications is usually based on simulations using package electrical models generated at nominal conditions in design. Process and temperature variations in production and applications are not considered.

This paper describes a simulation-based, two-level, fractional factorial design of experiment (DOE) approach of analyzing the impact of process and temperature variations on electrical parameters of package models. Linear regression models are built for each DOE response for electrical performance variation prediction. These predictions can be used in package design trade-off consideration and design optimization as well as in electrical performance budget analysis for FPGA and structural ASIC applications.

The FPGA wire-bond BGA package under study is a typical four-layer design with the top layer for signal routing, the second layer for ground reference, the third layer for power, and the bottom layer for solder ball pads.

To make it more comprehensive, the study uses signal nets with different trace lengths and bonding wire lengths. Also used are core power, I/O power, and ground nets.

DOE Methodology and Parameter Setup

The DOE method is useful in product variation analysis for a complicated system. Simulation-based DOE is a good approach for the electrical parameter analysis of such a system involving so many variables.

Design Factor Selection

Nine design factors covering package material properties, package geometries, and simulation setup are used in this study. Each design factor has two levels, a minimum and a maximum value. In selecting the minimum and maximum values of each factor, the authors factored in the worst package process and temperature variation. Simulation frequency is selected based on typical FPGA applications. Figure 1 shows the minimum and maximum values of all nine design factors.

Figure 1: Minimum and Maximum Values of Design Factors

Design Factors	Material Properties	Package Geometries	Simulation Setup	Minimum Value	Maximum Value
A	Solder mask ε_r			3.5	4.3
A	Substrate ε_r			3.9	4.7
B	Metal σ			41861 mho/mm	51163 mho/mm
B	Wire σ			35294 mho/mm	43138 mho/mm
C		Conductor thickness		(1)	(1)
D		Conductor width		35 µm	55 µm
E		Wire length		(2)	(2)
F		Dielectric thickness		(1)	(1)
G		PTH plating thickness		15 µm	25 µm
H			Mesh size	250	350
J			Frequency	400 MHz	600 MHz

(1) See Figure 2 for package stackup information
(2) The uncertainty for wire length is +/-100 µm. See Figure 4 for the nominal wire length for different nets under study.

Figure 2: Values of Design Factors C and F in the Four-Layer Package Stackup

Layer	Nominal (µm)	Variation (µm)	Variation #1 (µm)	Variation #2 (µm)	Variation #3 (µm)	Variation #4 (µm)
D1 (SM)	1200	1200	1200	1200	1200	1200
M1 (Signal)	15	+/-5	10	10	20	20
D2	50	+/-10	40	60	40	60
M2 (GND)	72	+/-10	62	62	82	82
D3	200	+/-20	180	220	180	220
M3 (PWR)	72	+/-10	62	62	82	82
D4	50	+/-10	40	60	40	60
M4 (Pads)	15	+/-5	10	10	20	20
D5 (SM)	20	20	20	20	20	20

Design Response Selection

Eight design responses include self inductance, self capacitance, mutual inductance, mutual capacitance, DC resistance, AC resistance, impedance, and propagation delay. These design responses cover all major electrical parameters in package design analysis and package signal integrity analysis.

Fractional Factorial Design

A 32-run 2_{IV}^{9-4} fractional factorial design is used for the experiment, since a nine-factor factorial design, with a total of 512 runs, requires too many experiment resources. Figure 3 lists all factor values in the 32 simulation runs for the design.

Figure 3: Two-Level Fractional Factorial Design

	Factors and Factor Levels								
Simulation Run #	**A**	**B**	**C**	**D**	**E**	**F**	**G**	**H**	**J**
1	-	-	-	-	-	+	+	+	+
2	+	-	-	-	-	+	-	-	-
3	-	+	-	-	-	-	+	-	-
4	+	+	-	-	-	-	-	+	+
5	-	-	+	-	-	-	-	+	-
6	+	-	+	-	-	-	+	-	+
7	-	+	+	-	-	+	-	-	+
8	+	+	+	-	-	+	+	+	-
9	-	-	-	+	-	-	-	-	+
10	+	-	-	+	-	-	+	+	-
11	-	+	-	+	-	+	-	+	-
12	+	+	-	+	-	+	+	-	+
13	-	-	+	+	-	+	+	-	-
14	+	-	+	+	-	+	-	+	+
15	-	+	+	+	-	-	+	+	+
16	+	+	+	+	-	-	-	-	-
17	-	-	-	-	+	-	-	-	-
18	+	-	-	-	+	-	+	+	+
19	-	+	-	-	+	+	-	+	+
20	+	+	-	-	+	+	+	-	-
21	-	-	+	-	+	+	+	-	+
22	+	-	+	-	+	+	-	+	-
23	-	+	+	-	+	-	+	+	-
24	+	+	+	-	+	-	-	-	+
25	-	-	-	+	+	+	+	+	-
26	+	-	-	+	+	+	-	-	+
27	-	+	-	+	+	-	+	-	+
28	+	+	-	+	+	-	-	+	-
29	-	-	+	+	+	-	-	+	+
30	+	-	+	+	+	-	+	-	-
31	-	+	+	+	+	+	-	-	-
32	+	+	+	+	+	+	+	+	+

Note: “+” means maximum value and “-” means minimum value

Net Selection

To make the study more comprehensive, the authors selected nets of different properties. As the later analysis shows, nets of different properties have different responses to factor variations.

The study uses three signal nets of different total net length and of different bonding wire length. The study also uses one I/O power net, the core power net, and the reference ground net. Figure 4 lists the six nets selected for this study.

Figure 4: Nets Selected for the Study

Net Name (Net Type)	**Net Length (μm)**	**WB Type**
S_B2_X_LVDSCLK_01N (Signal)	14324.51	Long
X_B2_X_VREF01B2 (Signal)	3547.28	Short
V_B2_X_LVDSL_37N (Signal)	13637.17	Long
VCCN2 (I/O Power)	12753.44	Short
VSS (Ground)	295070.65	Short
VCC (Core Power)	141942.1	Short

Simulation and Analysis

The DOE data are from simulation. It is impossible to collect the needed data for such a large-scale experiment through measurements. The simulation uses a 3D quasi-static electromagnetic solver. The simulation setup uses nominal values for all parameters except for those nine design factors.

Relative Factor Effect

Based on simulation data, the authors identified primary and secondary effects for each of the eight responses for each of the six selected nets. Figure 5 shows how each factor affects the DC resistance (DCR) of each net relatively. For nets (VCC, VSS, and VCCN2) with short bonding wires, DCR is most sensitive to conductivity variation. For nets with long bonding wires, DCR is more sensitive to conductor width and thickness variations.

Figure 5: Relative Factor Effect (in %) on DCR for Different Nets

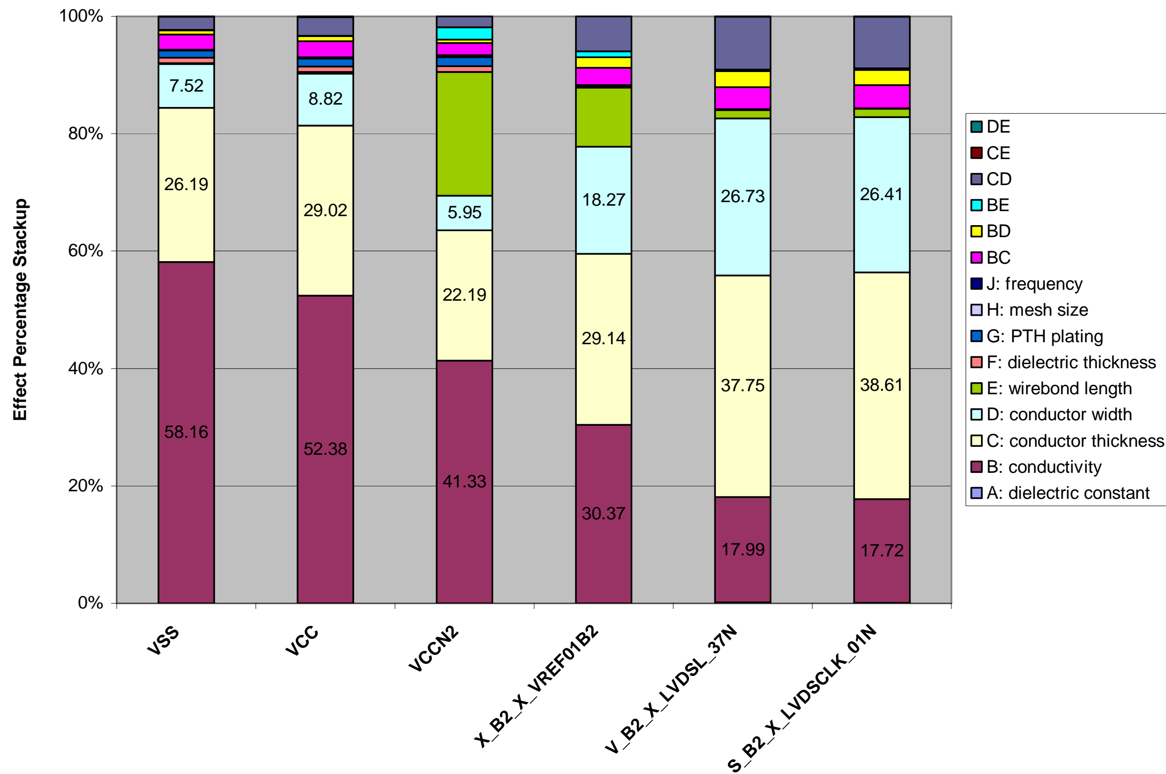
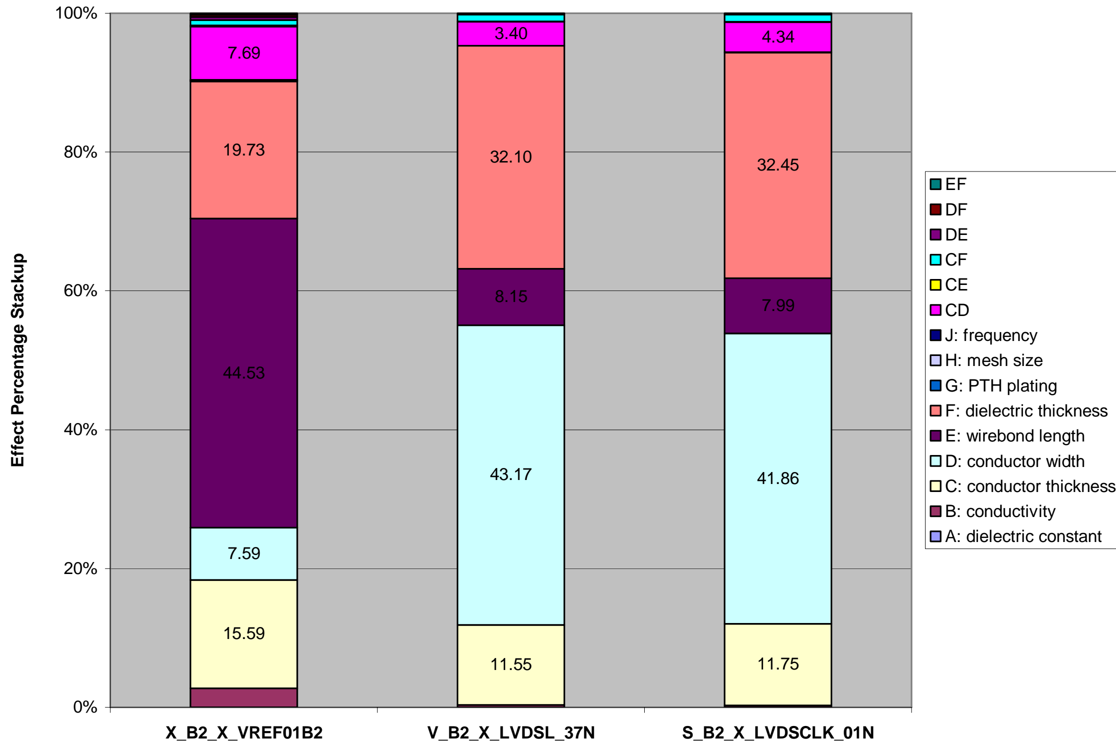


Figure 6 shows how each factor affects the self-inductance of each signal net relatively. For net X_B2_X_VREF01B2 with short bonding wires, self-inductance is very sensitive to bonding wire length variation. For nets S_B2_X_LVDSCLK_01N and V_B2_X_LVDSL_37N with long bonding wires, self-inductance is more sensitive to conductor width and dielectric thickness variations. From the DOE simulation data, it is easy to generate similar relative charts for relative factor effect on other electrical parameters. The authors also conducted similar sensitivity analysis for other electrical parameters.

Figure 6: Relative Factor Effect (in %) on Self-Inductance for Signal Nets



Linear Regression Model

Assuming all effects are linear, the authors derived a linear regression model based on the equation

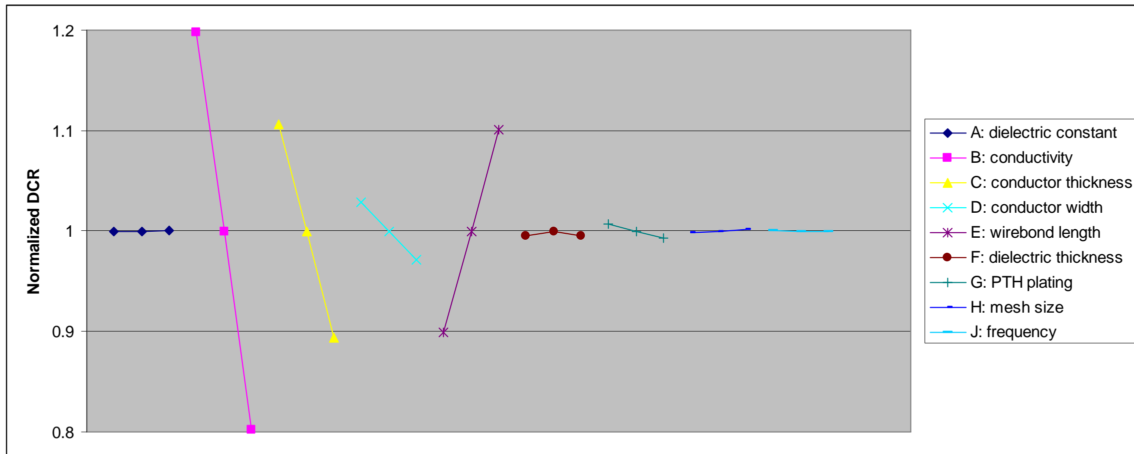
$$Response = \beta o + \beta m * Xm + \beta mn * Xm * Xn + \ldots\ldots + \varepsilon$$

where,

Xm is a factor of value [-1, +1]
βm is a fitting parameter corresponding to primary effect
βmn is a fitting parameter corresponding to secondary effect
ε is a residual error

for prediction of package electrical parameter variation. This model can be used to calculate the effectiveness of factors on each response of each net. Figure 6 shows the primary effectiveness of factors on DCR of net VCCN2. From the figure, for net VCCN2, DCR is more sensitive to conductivity, conductor thickness, and wirebond length than other factors.

Figure 6: Primary Effectiveness of Factors on DCR of Net VCCN2



Product Variation Case Study

As explained in the factor selection section, in this DOE, the authors considered the worst package process and temperature variation when selecting minimum and maximum values of each factor. The probability that each factor has the minimum or maximum value is every small. Most likely, the value for each factor will have a typical bell curve of normal distribution. Without the 3σ information, the variation of a factor is set at 25 percent of the minimum or maximum value to investigate the response difference between the nominal design and the product with variations. Figures 7 through 14 show different cases of product variation under different factor variation combinations.

As Figures 8 and 9 show, power/ground nets have less than 11 percent DCR variation while signal nets have about 25 percent DCR variation. In general, nets with planes/shapes and with more wires, such as power and ground nets, have much less DCR variation. Signal nets have much higher DCR variation, which, generally, is not a large concern.

Figure 7: Normalized Factor Values for DCR Variation Study

Design Factor	**Normalized Factor Value: Case 1**	**Normalized Factor Value: Case 2**
A: Dielectric constant	0.25	-0.25
B: Conductivity	0.25	-0.25
C: Conductor thickness	-0.25	0.25
D: Conductor width	-0.25	0.25
E: Wirebond length	-0.25	0.25
F: Dielectric thickness	0.25	-0.25
G: PTH plating	0.25	-0.25
H: Mesh size	0.25	-0.25
J: Frequency	0.25	-0.25

Figure 8: Product DCR Variation Study, Case 1

Net Name (Type)	Design DCR (mOhms)	Product DCR (mOhms)	Change (%)
VSS (Ground)	0.64	0.70	7.91
VCC (Core Power)	1.29	1.40	8.65
VCCN2 (I/O Power)	12.02	13.34	10.97
X_B2_X_VREF01B2 (Signal)	142.69	163.93	14.89
V_B2_X_LVDSL_37N (Signal)	556.08	692.42	24.52
S_B2_X_LVDSCLK_01N (Signal)	577.94	721.62	24.86

Figure 9: Product DCR Variation Study, Case 2

Net Name (Type)	Design DCR (mOhms)	Product DCR (mOhms)	Change (%)
VSS (Ground)	0.64	0.59	-7.67
VCC (Core power)	1.29	1.18	-8.32
VCCN2 (I/O power)	12.02	10.75	-10.57
X_B2_X_VREF01B2 (Signal)	142.69	122.82	-13.93
V_B2_X_LVDSL_37N (Signal)	556.08	431.91	-22.33
S_B2_X_LVDSCLK_01N (Signal)	577.94	446.96	-22.66

As Figures 11 and 12 show, signal nets have less than 10 percent impedance variation and less than 5 percent delay variation under the same set of factor variations shown in Table 10. Based on the regression model, it is easy to generate similar case study results for other electrical parameters.

Figure 10: Normalized Factor Values for Signal Impedance and Delay Variation Study

Design Factor	Normalized Factor Value: Case 1	Normalized Factor Value: Case 2
A: Dielectric constant	0.25	-0.25
B: Conductivity	0.25	-0.25
C: Conductor thickness	-0.25	0.25
D: Conductor width	0.25	-0.25
E: Wirebond length	0.25	-0.25
F: Dielectric thickness	-0.25	0.25
G: PTH plating	0.25	-0.25
H: Mesh size	0.25	-0.25
J: Frequency	0.25	-0.25

Figure 11: Product Signal Impedance Variation Study, Case 1

Net Name (Type)	Design Zo (Ohms)	Product Zo (Ohms)	Change (%)
X_B2_X_VREF01B2 (Signal)	54.98	53.40	-2.88
V_B2_X_LVDSL_37N (Signal)	71.15	66.69	-6.26
S_B2_X_LVDSCLK_01N (Signal)	69.82	64.74	-7.28

Figure 12: Product Signal Impedance Variation Study, Case 2

Net Name (Type)	Design Zo (Ohms)	Product Zo (Ohms)	Change (%)
X_B2_X_VREF01B2 (Signal)	54.98	56.70	3.12
V_B2_X_LVDSL_37N (Signal)	71.15	75.57	6.22
S_B2_X_LVDSCLK_01N (Signal)	69.82	74.98	7.38

Figure 13: Product Signal Delay Variation Study, Case 1

Net Name (Type)	Design Delay (Ohms)	Product Delay (Ohms)	Change (%)
X_B2_X_VREF01B2 (Signal)	38.51	40.13	4.23
V_B2_X_LVDSL_37N (Signal)	104.18	107.63	3.31
S_B2_X_LVDSCLK_01N (Signal)	110.56	115.27	4.26

Figure 14: Product Signal Delay Variation Study, Case 2

Net Name (Type)	Design Delay (Ohms)	Product Delay (Ohms)	Change (%)
X_B2_X_VREF01B2 (Signal)	38.51	36.82	-4.38
V_B2_X_LVDSL_37N (Signal)	104.18	100.54	-3.50
S_B2_X_LVDSCLK_01N (Signal)	110.56	105.47	-4.60

Conclusion

Simulation-based DOE methodology is a useful approach of analyzing package electrical parameter variation caused by process and temperature variations. Linear regression models built in the DOE study provide informative predictions for package electrical parameter variations. From the model, in a typical worst-case scenario of process and temperature variation, a signal net can have up to eight percent variation for key electrical parameters such as impedance and delay. Similarly, a power net can have up to 11 percent DCR variation. These predictions can be used in package design trade-off consideration and design optimization as well as in electrical performance budget analysis for FPGA and structured ASIC applications.

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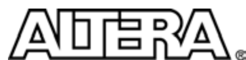

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San Jose, CA 95134
www.altera.com

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