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Using Programmable Logic for Receiver Offset and Yield Enhancement

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Abstract

As the chip manufacturing process scales down to smaller nodes, random offsets due to the statistical variations of fabrication are undermining performance, especially for analog/mixed signal circuitry. This paper presents a methodology for offset cancellation for the receive path of a programmable logic device (PLD) integrated wide-range transceiver. The transceiver was designed and fabricated in a 90-nm TSMC CMOS logic process. Voltage offsets in the receive path degrade the overall yield as performance specifications are violated. The main idea here is to take advantage of the digital PLD fabric to control analog front-end circuitry to enhance performance and, hence, manufacturability.

Author Biographies

Simar Maangat is a member of the technical staff at Altera Corporation, where he has worked for eight years, mainly in analog design development. His projects include work on 3.125-Gbps and 6.375-Gbps SERDES technology in Altera's Stratix® GX and Stratix II GX product lines. Prior to joining Altera, Mr. Maangat interned at Digital Equipment Corporation (DEC) in Palo Alto. He holds a BS degree in electrical engineering from the University of California, Berkeley. His areas of interest include high-speed analog technology.

Toan Thanh Nguyen is a member of the technical staff at Altera Corporation. He has over nine years of experience working in digital and analog design, and has worked on various blocks of high-speed transceiver and logic circuits. Mr. Nguyen holds a BS degree in electrical engineering and computer science from the University of California, Berkeley. His areas of interests are in high-speed analog design and signal integrity.

Wilson Wong is a principle design engineer at Altera Corporation. He has more than 18 years of experience in analog circuit design. His current interests include high-speed equalization, adaptive equalization, and clock data recovery circuits. Prior to joining Altera, Mr. Wong worked at Nexgen Microsystems and Tredennick, Inc. He holds a BSEE from the University of California, Berkeley.

Tina Tran is a senior design manager at Altera Corporation. She currently works in the design group responsible for the development of high-speed transceivers at Altera. Ms. Tran has worked in the semiconductor industry for more than 15 years, including 10 years with Altera. She holds a BSEE from the University of California, Berkeley.

Sergey Shumarayev is a director of engineering at Altera Corporation, responsible for analog design. He has worked at Altera for over 10 years in the capacities of design engineer, SERDES team engineering senior design manager, and analog group director. He holds a master's degree in electrical engineering from Cornell University and a BS in electrical engineering computer science and material science from the University of California, Berkeley. Mr. Shumarayev has over 30 issued patents and has co-authored several papers.

Tim Hoang is a design manager at Altera Corporation. He has over 13 years of experience in digital and analog design and development. Mr. Hoang has worked on SERDES and dynamic phase alignment (DPA) design in the Altera[®] Stratix[®] GX and Stratix II GX product lines. He holds a BS degree in electrical engineering from the University of California, Berkeley. His areas of interest are in high-speed analog technology.

Introduction

A wide-range transceiver was designed and fabricated in a 90-nm TSMC CMOS logic process. Each transceiver channel contains a transmitter and receiver with clock data recovery (CDR) circuit. The range of operation for this transceiver is from 622 Mbps to 6.5 Gbps. Voltage offsets in the receive path degrade the performance of the transceiver by putting a lower bound on the precision with which a data bit can be measured. In addition to raising the minimum input voltage that can be correctly detected by the CDR, offsets in the receive path cause duty cycle distortion. This distortion, coupled with inter symbol interference (ISI), reduces the overall margin of data recovery, directly worsening the bit error rate (BER). This paper presents a methodology to cancel voltage offsets in the receive path with a soft intellectual property (IP) core programmed in the programmable logic device (PLD).

The transceiver was designed for a wide range of wireline applications. It supports a variety of protocols including Gigabit Ethernet, XAUI, and CEI, which have a lowest input voltage specification. For instance, PCIe-Gen2 places the lower bound for V_{ID} (peak-to-peak input voltage) at 100 mV. The 3-sigma voltage offset, due to a mismatch in the receiver, was calculated to be a 36-mV differential. This offset eats into the V_{ID} requirement and puts pressure on the CDR, as shown in Figure 1 below. The IP developed to cancel the voltage offset in the receive path is implemented in the PLD. It makes use of the data captured by the phase detector (PD) in the CDR and controls the analog hooks in the receiver path to minimize the offset.

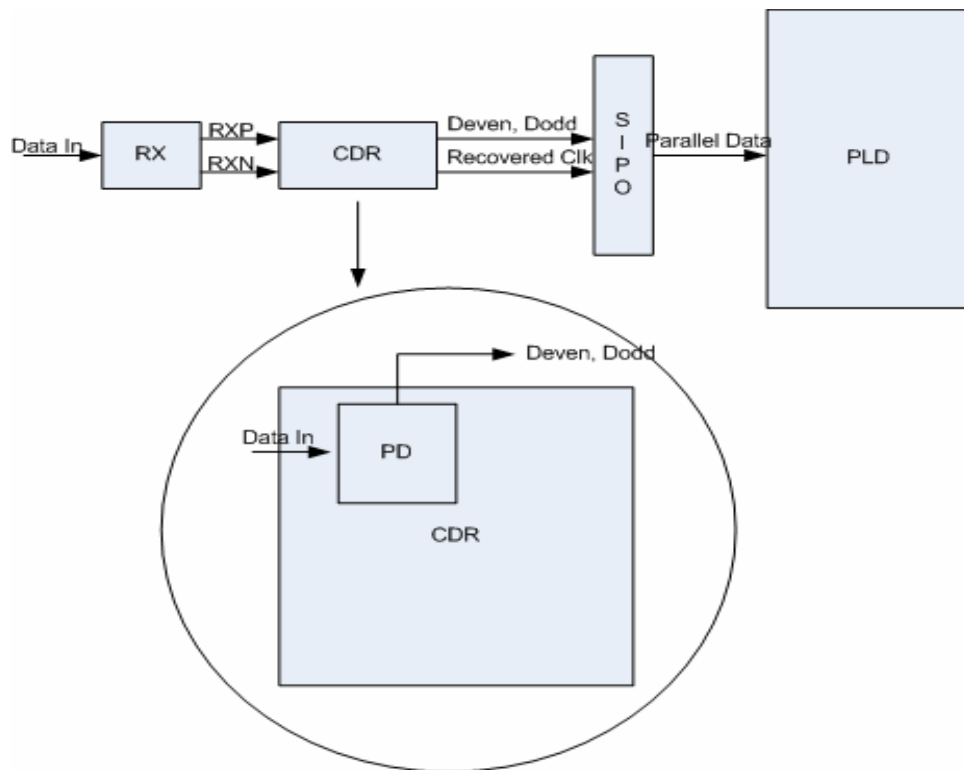


Figure 1. Receive Datapath

Receive Datapath Overview

The receive datapath is shown in Figure 1. A brief description of the receive datapath component follows.

Receiver (Rx)

The receiver (RX) receives the serial data and relays it to the CDR. It has a programmable equalization capability that is used to boost the gain at higher frequencies to negate the effect of high-frequency signal loss in the cable/backplane. The main function of this block is to reduce the demands on the phase detector (PD), which needs to convert the data into digital signal levels without error. Voltage offset of the receiver adds to the inter symbol interference (ISI), which is a primary manifestation of high-frequency signal attenuation, and further reduces the margin of detection by the PD. Since ISI is a frequency-dependent problem, a DC offset added to it just enhances that problem and translates into speed degradation. The DC gain of the receiver is 0 dB. The design provides up to four programmable zeros and four poles in the transfer function. A symbolic diagram of the receiver transfer function is shown below in Figure 2

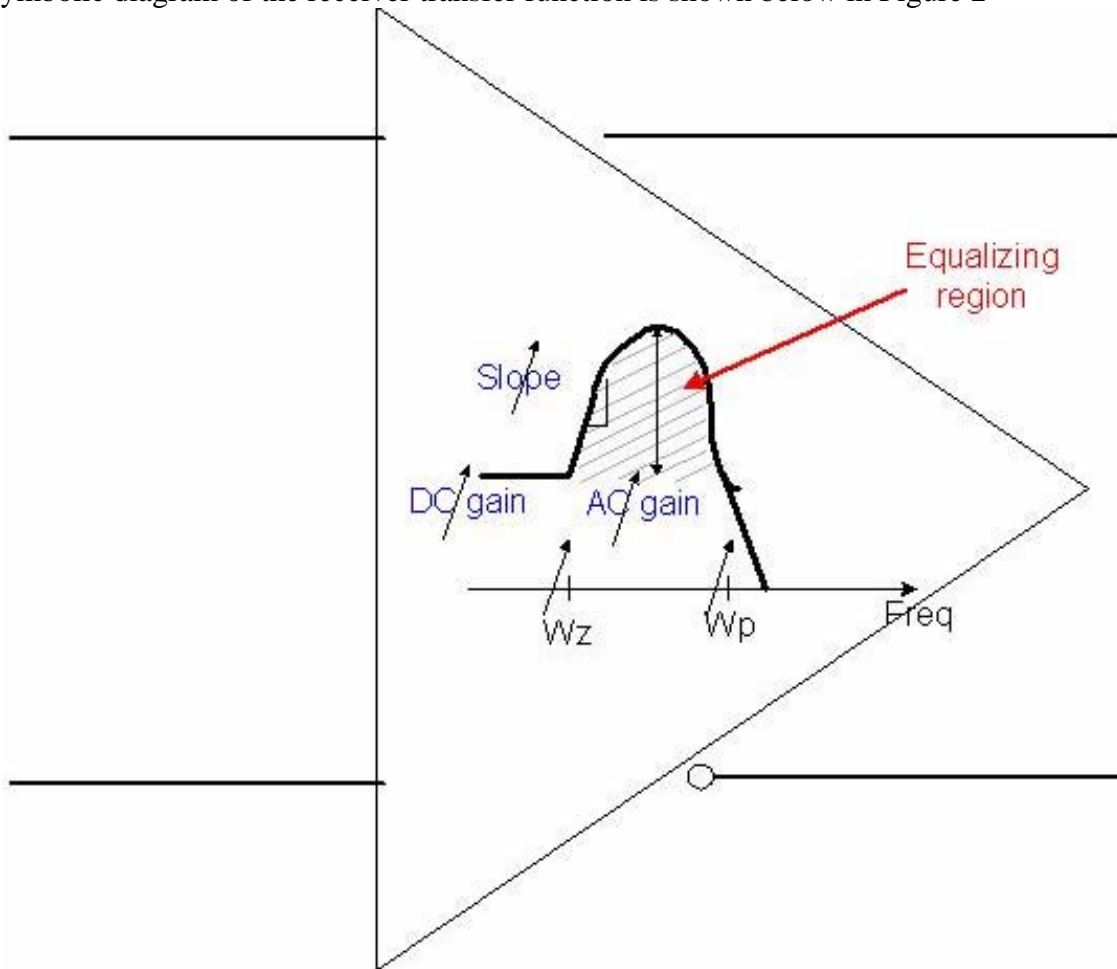


Figure 2. Receiver Transfer Function

Phase Detector

The phase detector (PD) in the CDR is a bang-bang phase detector (BBPD). The BBPD is a half-rate non-linear circuit. Half rate refers to the fact that the clock runs at half the rate of the data and that it is non-linear. This is because the output is not a scalar of the phase difference between clock and data. As shown in Figure 3, the first stage of flip-flops in BBPD is clocked by a 4-phase clock with phases 0, 90, 180, and 270 running at half the data rate. CLK0/CLK180 are used to sample EVEN and ODD bit data, respectively, and CLK90/CLK270 are used to detect transition edge. When the loop is locked, CLK0 and CLK180 should be aligned at the middle of the data. The recovered clock and data are then sent to the deserializer or serial-in-parallel-out (SIPO), from where the parallel low-speed data is then sent to the PLD core.

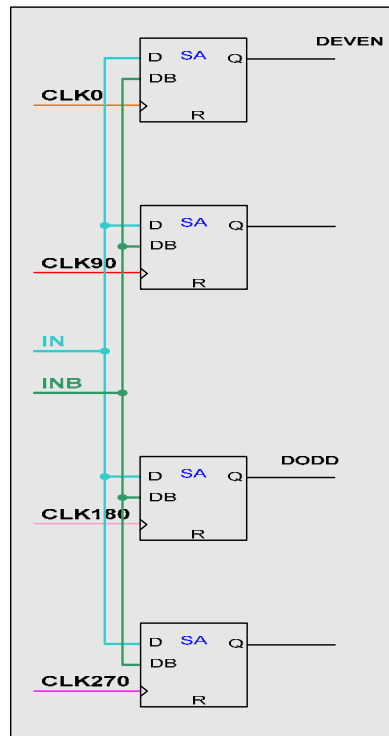


Figure 3. First Stage of Phase Detector

The BBPD timing diagram is shown in Figure 4. Phase matching decisions are made by looking at a combinational logic of samples at 0, 90, 180, and 180, 270, and 0, respectively. Note that even data corresponds to bit location sampled by phase 0 and odd data by phase 180.

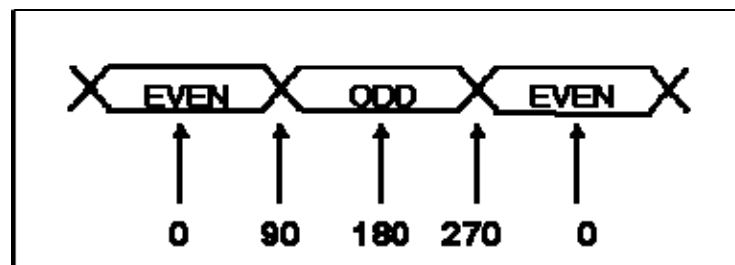


Figure 4. BBPD Timing Diagram

Deserializer (SIPO)

The deserializer receives the even and odd data (DEVEN/DODD) from the CDR along with the 4-phase clocks (CLK0, 90, 180, 270). It then converts the even/odd data into parallel data and sends it to the PLD core along with the recovered clock.

Receive Path Offsets

The offsets in the receive path occur in the RX and the PD. Since the data that is observed is clocked by phases 0 and 180, only those stages of the PD are shown in Figure 5.

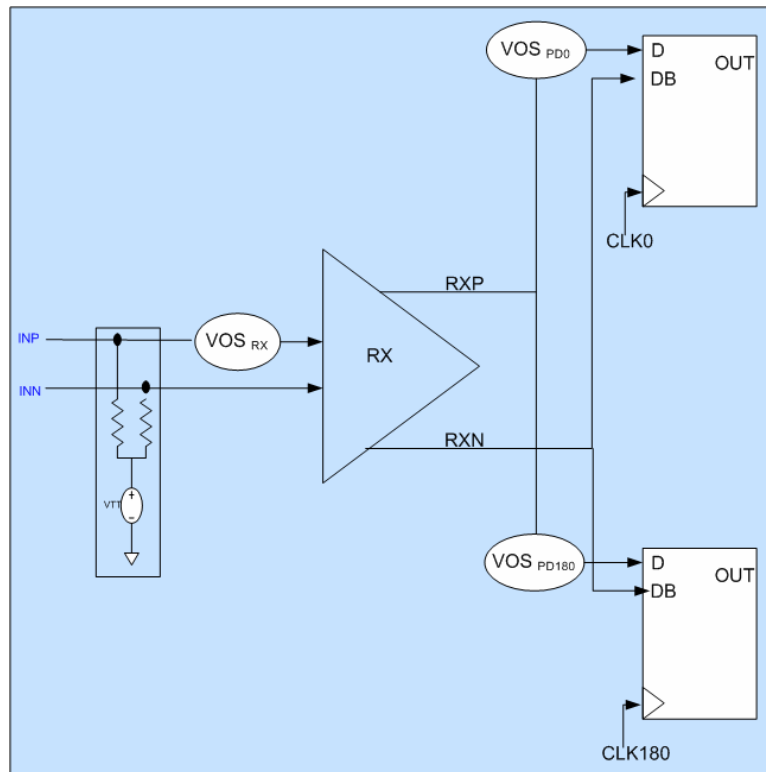


Figure 5. Voltage Offsets in Receive Path

From Figure 5, if the offsets of the PD (i.e., VOS_{PD0} and VOS_{PD180}) were zero, then the total offset would just be VOS_{RX} . However, the PD offsets in the worst-case scenario can be in the opposite direction, compounding the total offset.

The voltage offsets caused by a mismatch in the fabrication are getting worse as the technology shrinks. The 65-nm and 45-nm nodes have more of a mismatch problem than the 90-nm node, and increasing the number of legs of devices has a physical limitation. Hence, it is becoming more important to deal with offsets going forward to guarantee a decent yield.

Offset Reduction Methodology

In the methodology developed, the RX inputs are left floating at the common mode level. Thus, the outputs of the RX, namely RXP and RXN, will exhibit the total RX offset (since the RX gain is 0 dB). Combined with the individual offsets of the PD phases 0 and

180, *Deven* and *Dodd* are sampled and sent to the PLD core. Note that there is no timing issue here for the PD since the data is static and the clock is run at a low frequency of 400 MHz. A soft controller IP programmed in the PLD core analyzes the data and returns digital control to the RX buffer to induce a canceling offset. This is shown in Figure 6 below.

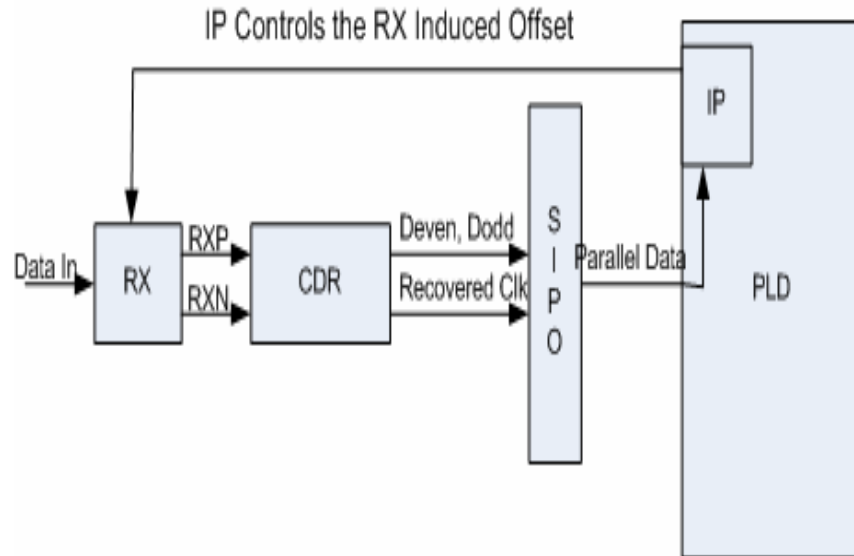
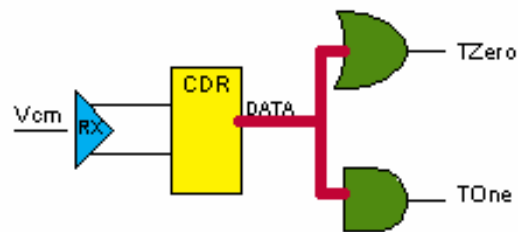


Figure 6. RX Offset Cancellation Scheme

The induced offset is stepped to both extremes until the data is a stable “1” or a stable “0”. The optimum offset cancellation setting is right in the middle of this “unknown” region. A symbolic diagram of the IP that controls the RX-induced offset is shown in Figure 7.



TZero	TOne	State
0	0	0
1	1	1
1	0	Unknown(X)

Figure 7. Soft Controller in the PLD

The unknown state happens when the differential voltage RXP-RXN is not large enough to trip the PD phases 0 and 180 both in the same direction. In other words, the ‘unknown’ region is the aperture of the PD. Therefore, *Deven* and *Dodd* will be of unstable state. The optimum voltage offset setting to result in the lowest V_{ID} is in the center of the ‘unknown’ region. This concept is illustrated graphically in Figure 8.

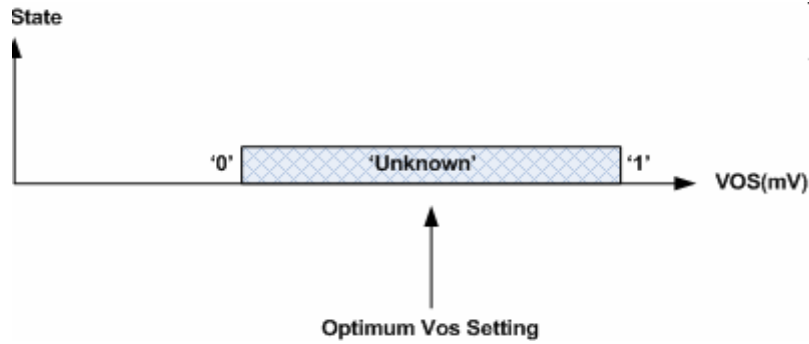


Figure 8. Optimal V_{OS} Selection

Thus, the offset cancellation scheme averages out the total offset seen at the PD stages 0 and 180, respectively.

Silicon Results

The 90-nm silicon measurements were taken with the offset cancellation scheme “on” and “off.” The PRBS10 pattern was used for the criteria of BER better than $10e-12$ on a sample size of 80 units. The results are promising as the minimum V_{ID} that achieved BER better than $10e-12$ has a much tighter distribution. A chart of the measurement data is shown below in Figure 9:

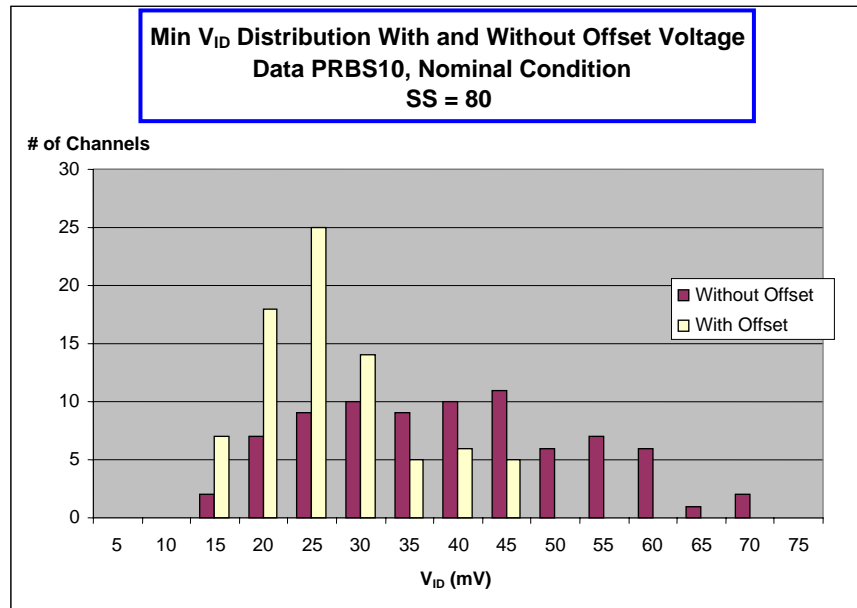


Figure 9. Minimum V_{ID} Distribution

Figure 10 below shows the minimum V_{ID} required as a function of all the offset settings available. It is apparent in two of the channels shown that the minimum V_{ID} is achieved by canceling out the offset. For the third channel, the random offset is 0; therefore, the minimum V_{ID} occurs at the 0 offset setting. This data is taken from within the 80 silicon samples.

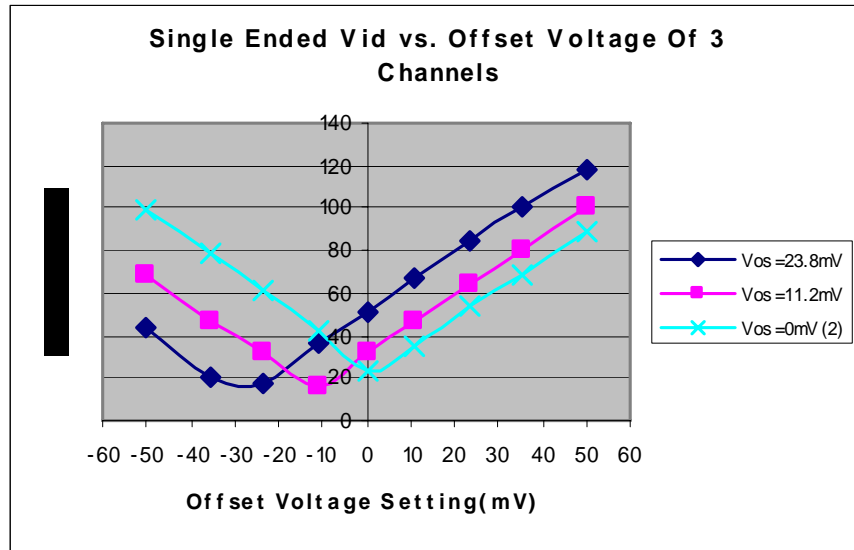


Figure 10. Minimum V_{ID} vs. Offset Voltage Setting

Figure 11 below shows the impact of offset cancellation directly on the BER. The measurement data is for a PRBS23 pattern through a 40" FR-4 backplane (which induces a large amount of ISI). The chart shows BER vs. offset voltage. Induced offset was stepped through all the settings available and BER was measured. We can see that the relative BER improves by an order of magnitude with offset cancellation "on" for a V_{OS} setting of 10 mV or 20 mV.

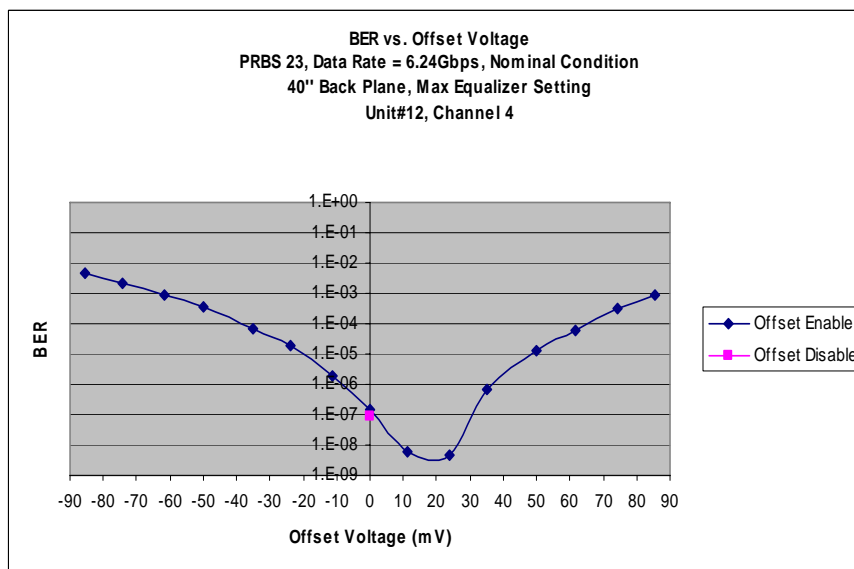


Figure 11. BER vs. Offset Voltage

Future Enhancements

For future process shrinks, i.e., going into 40-nm and 32-nm nodes, process mismatch will become a bigger problem for analog circuits and, in some cases, seriously affect performance. So, in future transceiver development, offset cancellation methodology is extended for PD stages also.

Conclusions

This paper has demonstrated a digitally assisted offset cancellation scheme that was proven on silicon. The offset reduction can improve the performance of a PLD integrated transceiver. The IP-based methodology was found to be an effective replacement for a switch capacitor or feedback amplifier schemes that have certain design impacts and requirements. The results show a tighter V_{ID} distribution directly affecting yield and an improved performance shown by the BER.

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References

B. Razavi, "Design of Analog CMOS Integrated Circuits"



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