

# **Multi-Clock Domain TDF ATPG Testing: An Innovative Approach**

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## **ABSTRACT**

With the rapid advancement of fab process technology into the nanometer node era, there is an increasing trend in the manifestation of deep sub-micron (DSM) marginal defects in integrated circuit (IC) fabrication. Despite transition delay fault (TDF) tests providing reasonable coverage against DSM marginal defects, this methodology is hampered in designs with multiple clock domains where the lowest operating clock frequency becomes the dominant TDF testing frequency. The methodology advocated in this paper aims to overcome this bottleneck by introducing an automated yet comprehensive approach to segregate and consolidate the various clock domains in any design for more effective TDF testing. It identifies all user registers in the design and recursively identifies the clock sources of those registers through intelligent net connectivity analysis. In an experimental 200M-transistor and 4-clock-domains test-chip netlist, this methodology is able to identify clock sources for all registers in five minutes time, and that processing time is negligible when compared to the TDF automatic test pattern generation (ATPG) time. Hence, it has been proven effective and highly successful in increasing the TDF test frequency to the highest operating clock domain frequency of the design.

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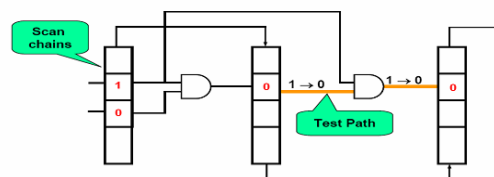
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## 1.0 Introduction

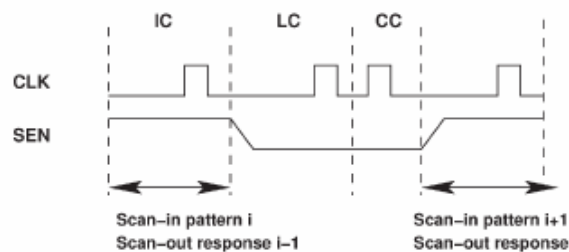
With the advance of process technology, gate counts and the number of interconnects increases. Deep sub-micron (DSM) effects such as higher clock rate, shrinking geometries, and longer wires are becoming more prominent, thereby increasing the probability of timing-related defects [1]. As a result, at-speed testing has become an important way to ensure the high quality of the device.

Transition delay fault (TDF) automatic test pattern generation (ATPG) testing provides relatively good coverage for marginal defects [2]. A TDF test requires a pattern pair (V1, V2) to be applied to the circuit under test. Pattern V1 is termed as the initialization pattern and V2 as the launch pattern. The response of the circuit under test to the pattern V2 is captured at the operational functional speed [3].

Figure 1 shows the 3-registers requirement to support the launch off capture (LOC) mode of TDF ATPG testing. Two registers are required to initiate a transition ( $0 \rightarrow 1$  or  $1 \rightarrow 0$ ) and the third register is used to capture the desired output. Figure 2 shows the waveform diagram for LOC mode. By applying two consecutive high-speed clock pulses, slow-to-rise (transition  $0 \rightarrow 1$ ) or slow-to-fall ( $1 \rightarrow 0$ ) can be detected accordingly.

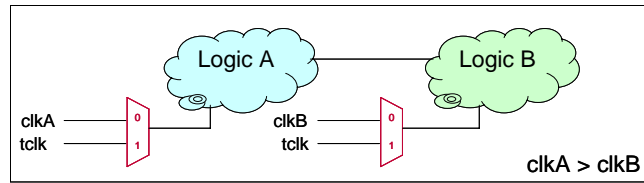


**Figure 1 3-Registers Requirement for TDF ATPG Testing**



**Figure 2 Launch Off Capture Mode**

It is common to have single test clock in the design under test (DUT) for testing purposes. It is efficient to enable stuck at ATPG testing with a low DFT overhead and minimal ATE resource (single high-speed clock source and single test enable). Figure 3 shows the single test clock for a typical user design. Multiplexers are added at the appropriate spot so that test clock and user clock are sharing the same clock path. The user clock can be generated from a primary pin, internal phase-locked loop (PLL), or core-generated clock.



**Figure 3 Single Test Clock Network**

During the static timing closure process, the register-to-register timing closure is performed at the user operating speed. In Figure 3, two clock domains (clkA and clkB) are shown where frequency of clkA is higher than clkB. Owing to different functional operating frequency, the static timing closure process guarantees that “Logic A” operates up to clkA frequency and “Logic B” operates up to clkB frequency. In order to apply TDF ATPG testing, two approaches are considered:

- Running TDF ATPG testing at a fixed frequency for a given DUT:* In this approach, TDF ATPG is applied to the entire DUT regardless of its clock domain. The fixed frequency must be the lowest user operating frequency or minimum operating frequency guaranteed by the design. As shown in Figure 3, TDF ATPG testing is performed at clkB frequency for both Logic A and Logic B.
- Running TDF ATPG testing according to user operating frequency:* In this approach, appropriate masking mechanism is required for user logic that is designed to run at a lower frequency than the testing frequency, using a multi-pass testing approach. Again referring to Figure 3, the first TDF ATPG testing is performed at clkA frequency by applying constraints to Logic B. Subsequent TDF ATPG testing is performed at clkB frequency to detect the rest of the undetected circuitry.

Approach (a) is the simplest method, but does not get good at-speed coverage. Approach (b) is the preferred method for better marginal defect coverage for any given DUT. The challenge with approach (b) is the ability to identify and segregate user logic according to the operational speed. The main objective of the proposed method is to allow approach (b) by an automatic software system for clock identification.

## 2.0 Clock Domain Segregation Process

In this section, the author will discuss further the user register extraction portion, the core engine to enable node back tracing mechanism, the software flow, and the automation in place for TDF ATPG testing.

### 2.1 User Register Extraction

During clock domain segregation process, user registers are identified and their user clock source is traced. Figure 4 assumes Logic A and Logic B are running at different frequencies. Register 2 is used to capture the Logic A response and Register 3 is used to capture the Logic B response, respectively. In TDF ATPG terminology, Register 2 is used as a capture register for Logic A and Register 3 is used as a capture register for Logic B. In other words, when we perform at-speed testing against Logic A, Register 3 must be masked during the capture cycle. Similarly, Register

2 is masked during the capture cycle when at speed testing is performed against Logic B. Tetramax from Synopsys supports register masking using the command “add\_capture\_mask.”

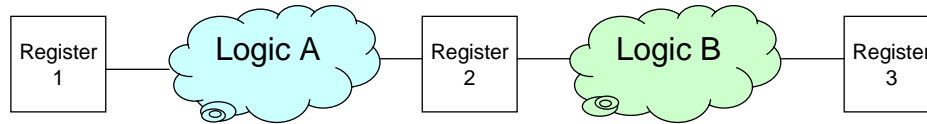


Figure 4 Register Extraction

## 2.2 Back Tracing Process

The number of clock domains and their clock characteristics (speed, phase, etc.) is design dependent. The clock can come from a primary pin, PLL, or core-generated clock. During design static timing analysis (STA), the clock source information can be dumped out using PrimeTime command “report\_clock.”

A clock buffer may be added to route the clock signal to the entire device. At the same time, combinatorial logic may be added as clock selection logic to have more than one clock feeding the same logic. In order to identify the clock frequency information of a given register, the clock node of register is mapped back to its clock source (identified in the STA report). This is known as the back-tracing process.

The back-tracing process (shown in Figure 5) starts with the clock node identification of registers. Connectivity analysis is carried out to find the signal route for the clock node until a clock source is identified.

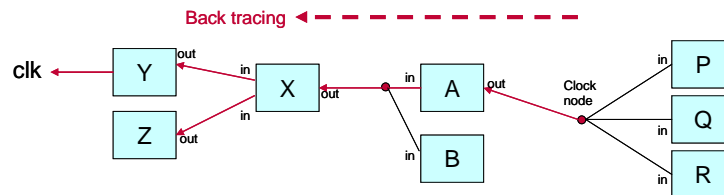


Figure 5 Back-Tracing Process

The back-tracing process uses a breadth-wide searching mechanism to intelligently look for all the fan-in nodes. A recursive technique is used to perform back-tracing operation. The pseudo-code of modular back-tracing method is explained in Figure 6.

```

FUNCTION BACKTRACE ( node )
  IF Clock OR PI FOUND
    Done
  ELSE
    Get all modules feeding node
    FOREACH module
      FOREACH input of module
        BACKTRACE ( input )
      END
    END
  END IF
END FUNCTION

```

Figure 6 Pseudo Code for Back Tracing

### 2.3 Software Flow

A Perl language-based software tool has been developed to automatically carry out the clock domain segregation process, with a set of Perl libraries developed to perform specific tasks. As shown in Figure 7, the software tool starts by parsing and loading all the Verilog libraries and design netlist, then builds the required data structure on the node connectivity. A report file is processed to store the clock source information (i.e., clock node to frequency information). Afterward, the clock port of every register is extracted, the back-tracing process matches the clock information, and the hierarchical names of the register nodes are printed out.

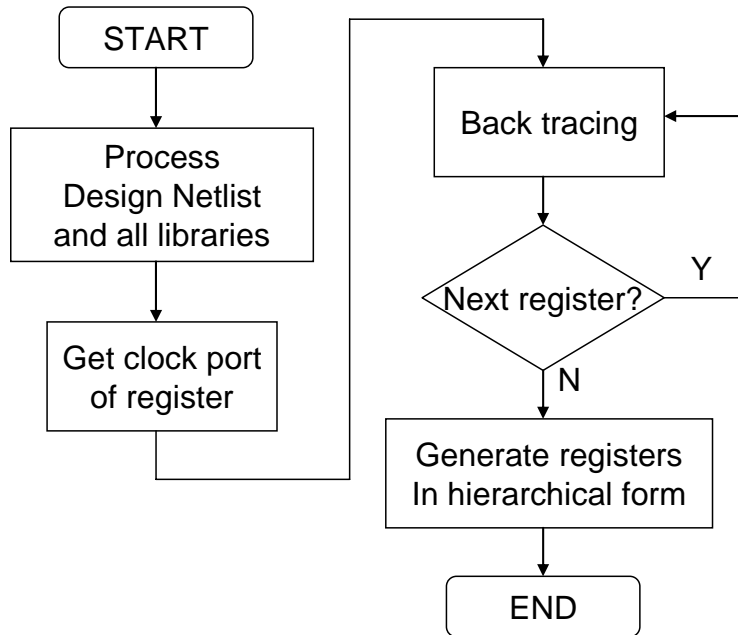


Figure 7 Software Flow Chart

### 2.4 TDF ATPG Process

The clock domain segregation process will be executed prior to TDF ATPG. Figure 8 shows the flow chart of TDF ATPG process, which is carried out on a per-clock-domain basis. During TDF ATPG, a capture mask will be applied to registers that have operational frequencies lower than the target TDF ATPG run frequency.

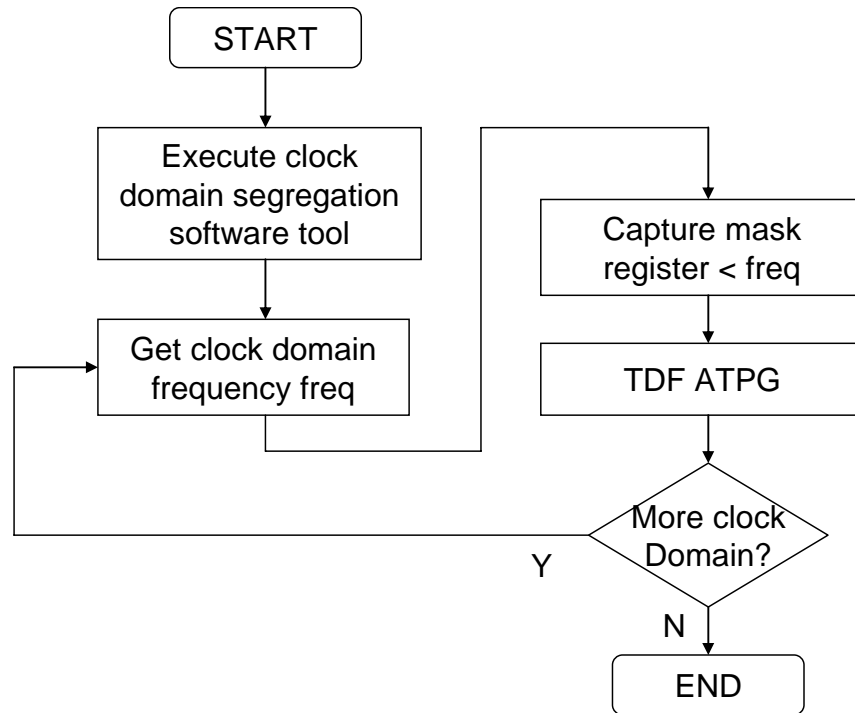


Figure 8 TDF ATPG Process

### 3.0 Conclusions and Recommendations

In this paper, the clock domain segregation process has been explained in detail. Back tracing is the key algorithm used throughout the clock domain segregation process. The process starts at the clock node of the register, and searches for all the fan-in nodes until a clock source is identified. This process will be part of TDF ATPG process, with a full automation environment enabled to support TDF ATPG.

### 4.0 Acknowledgements

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