

# DesignCon 2006

## Accurate Calibration and Measurement of Non-Insertable Fixtures in FPGA and ASIC Device Characterization

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## **Abstract**

S-parameter measurement on interfaces with non-insertable connections has been a challenge to FPGA- and ASIC-device characterization engineers. The standard two-port SOLT calibration is not well defined for a device-under-test (DUT) with connectors of a different family such as waveguide or coaxial. This paper describes a practical approach to performing accurate calibration on non-insertable test fixtures by employing the de-embedding technique. To demonstrate the technique, two characterization examples are illustrated. Full-wave models are generated to validate the experimental results.

## **Author Biographies**

**Hong Shi** is technical lead for electrical design in the Packaging Technology Group of Altera Corporation. His current responsibilities include developing strategy for high-density and high-performance FPGA packaging, simulating system level electrical performance and developing chip-package-board interconnect codesign capability. Before joining Altera, Hong was with HP and Agilent Technologies where he was principal engineer and project leader for Agilent's first 40-Gbps digital communications analyzer module. Hong has published over 30 technical papers in areas of optoelectronics, microwave circuits and digital circuit packages. Hong obtained his BSEE from Xi'an Jiaotong University, a MS in Physics from DePaul University and a PhD in electrical engineering from CREOL College of Optics at University of Central Florida.

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## I. Introduction

S-parameter measurement on interfaces with non-insertable connections, such as a fixture for the BGA package test, has been a challenge to FPGA and ASIC device characterization engineers. A common measurement strategy is to measure transmission behavior from BGA pads to board-edge SMA connectors. Advanced characterization also requires transmission measurement from V4 bumps in a package stacked on the test board to the edge SMA connectors. In both cases, the micro probe is the choice for probing pads or bumps, whereas coax cable connects the board SMA connector to an oscilloscope or VNA. The issue is that standard SOLT calibration cannot be entirely completed because the “thru” standard is not defined for different types of interfaces, such as probe and coax. The term “non-insertable” comes from the fact that probe used for probing BGA pads cannot directly mate to coax connector without using any adapter.

Figure 1 shows an example in high-speed FPGA transceiver characterizations.

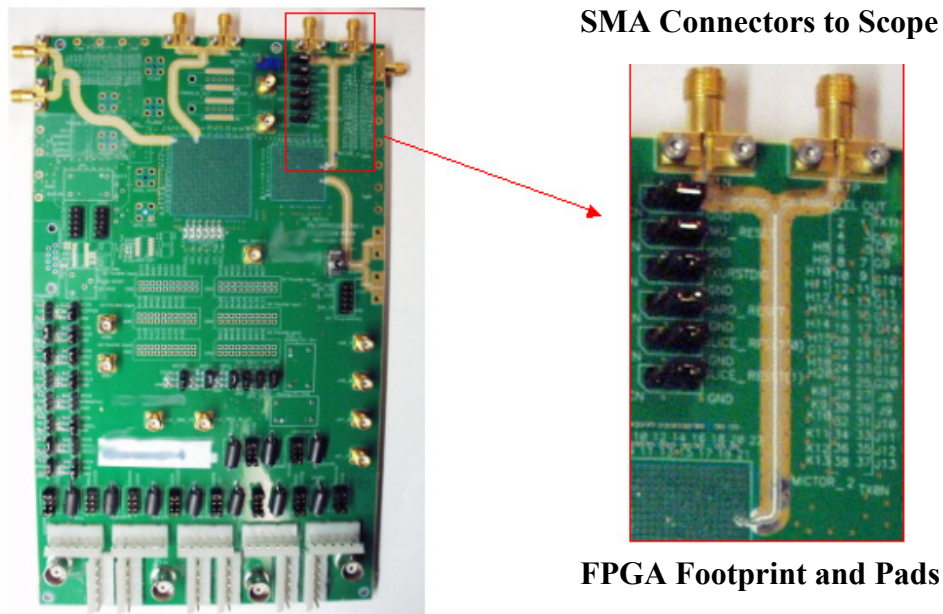


Figure 1. High-Speed Transceiver FPGA Device Characterization Board

In the picture, the outlined box in red indicates the transmission path connecting the FPGA pads to the edge SMA. The characteristics of this section of the fixture are critical to the accuracy of the measurement, especially for multi-gigahertz data transmission. The waveform at the oscilloscope (receiver) is a convolved impulse response of the FPGA transceiver, pads, transmission line and SMA connectors, in which only the FPGA transceiver behavior is of our interest. Thus, other contributions will have to be removed from the final waveform in order to reveal the actual performance of the FPGA device. The most common strategy for fixture removal is to separately characterize each portion

of the fixture and then use the “de-embedding” algorithm to mathematically substrate from receiver waveform.

However, there is a practical issue for removing a fixture that has a connection with a different family on each end, such as waveguide and coaxial in this case. It is not possible to directly measure such a fixture since the required full two-port calibration cannot be accomplished without a direct insertable thru standard between two distinct connections. As a work-around, a brute-force probe-to-SMA adapter can be built in a reversed interconnect sense and then connected back to back to the original fixture such that the end-to-end connection is with the same type, or, insertable for standard SOLT calibration. The caveat is that fixture errors are embedded in the final measurement.

An alternative work-around is with using the TRL calibration method, where (t)hru, (r)eflect and (l)ine are measured on a few short transmission lines. The challenge is that these transmission lines need to be fabricated in a strict sense to mimic the final fixture in terms of material, discontinuity and even the runs of PCB fabrication. For the V4 bump to board measurement, in which DUT has both vertical (bump and via) and horizontal (board trace) properties, it is very difficult at the best to establish TRL standards for accurate calibration and measurement in this environment.

In the approach pursued in this paper, we propose an accurate method to calibrate non-insertable fixtures and to measure BGA packages on test boards. It requires one additional measurement on a fixture and simple post processing for de-embedding using simulation tools such as ADS or mathematical tools such as MATLAB. To validate the approach, a 3D model that reflects the fixture after de-embedding is applied in end-to-end S-parameter simulations. The simulation correlation to de-embed the measurement demonstrates the accuracy of the proposed method.

## **II. Review of S-Parameter and Signal Flow Graph**

In this section, a brief review of the basics of the S-parameter and signal flow graph is given to establish the theoretical foundation for fixture de-embedding.

RF and microwave networks are often characterized using scattering or S-parameters. The S-parameters of a network provide a clear physical interpretation of the transmission and reflection performance of the device. The S-parameters for a two-port network are defined using the reflected or emanating waves,  $b_1$  and  $b_2$ , as the dependent variables, and the incident waves,  $a_1$  and  $a_2$ , as the independent variables. The general equations for these waves as a function of the S-parameters is shown below:

$$\begin{aligned} b_1 &= S_{11}a_1 + S_{12}a_2 \\ b_2 &= S_{21}a_1 + S_{22}a_2 \end{aligned}$$

Using these equations, the individual S-parameters can be determined by taking the ratio of the reflected or transmitted wave to the incident wave with a perfect termination

placed at the output. For example, to determine the reflection parameter from Port 1, defined as  $S_{11}$ , we take the ratio of the reflected wave,  $b_1$ , to the incident wave,  $a_1$ , using a perfect termination on Port 2. The perfect termination guarantees that  $a_2 = 0$ , since there is no reflection from an ideal load. The remaining S-parameters,  $S_{21}$ ,  $S_{22}$  and  $S_{12}$ , are defined in a similar manner. These four S-parameters completely define the two-port network characteristics, as shown in Figure 2.

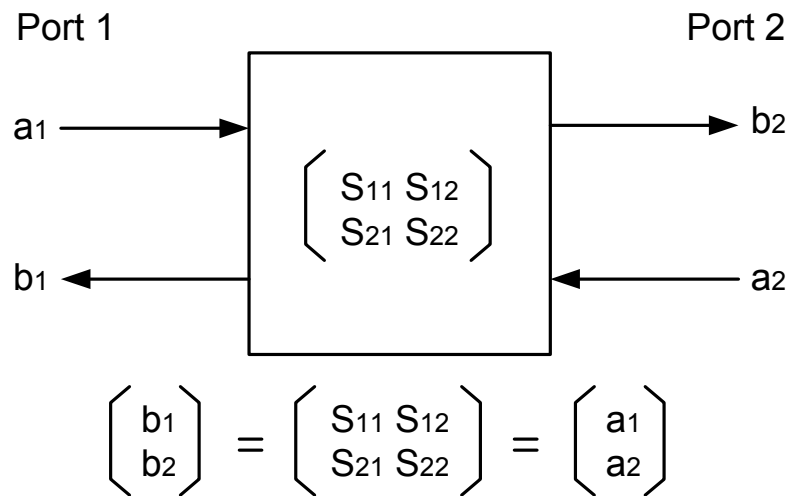


Figure 2. Two-Port Network Defined by S-Parameters

An alternative way to represent the S-parameters of any network is with a signal flow graph in Figure 3. A flow graph is used to represent and analyze the transmitted and reflected signals from a network point of view. Directed lines in the flow graph represent the signal flow through the two-port device. For example, the signal flowing from node  $a_1$  to  $b_1$  is defined as the reflection of Port 1 or  $S_{11}$ . When two-port networks are cascaded, it can be shown that connecting the flow graphs of adjacent networks is possible because the outgoing waves from one network are the same as the incoming waves of the next. This application of signal flow graphs will be used to develop the mathematics behind network de-embedding.

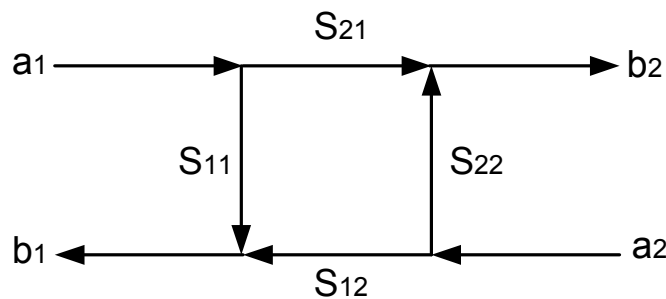


Figure 3. Two-Port Network Described by Signal Flow Graph

Before the mathematical process of de-embedding is developed, the test fixture and the DUT must be represented in a convenient form. Using signal flow graphs, the fixture and device can be represented as three separate two-port networks as shown in Figure 4. In this way, the test fixture is divided in half to represent the coaxial to non-coaxial interfaces on each side of the DUT. The two fixture halves will be designated as Fixture A and Fixture B for the left-hand and right-hand sides of the fixture respectively. The S-parameters  $FA_{xx}$  ( $xx = 11, 21, 12, 22$ ) will be used to represent the S-parameters for the left half of the test fixture and  $FB_{xx}$  will be used to represent the right half.

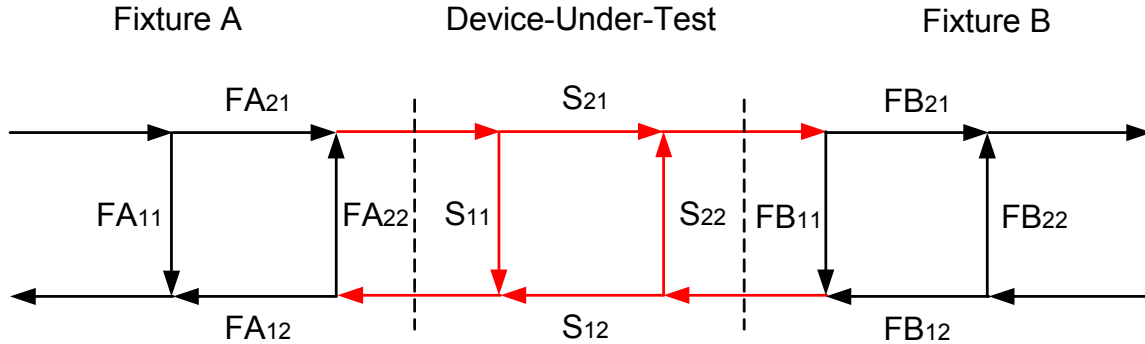


Figure 4. Signal Flow Graph Representing the Test Fixture Halves and DUT

If we wish to directly multiply the matrices of the three networks, we find it mathematically more convenient to convert the S-parameter matrices to scattering transfer matrices or T-parameters. The mathematical relationship between S-parameter and T-parameter matrices is given below. The two-port T-parameter matrix can be represented as  $[T]$ , where  $[T]$  is defined as having the four parameters of the network.

$$\begin{pmatrix} T \end{pmatrix} = \begin{pmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{pmatrix} = \begin{pmatrix} -(S_{11}S_{22}-S_{12}S_{21})/S_{21} & S_{11}/S_{21} \\ -S_{22}/S_{21} & 1/S_{21} \end{pmatrix}$$

Because we defined the test fixture and DUT as three cascaded networks, we can easily multiply their respective T-parameter networks,  $T_A$ ,  $T_{DUT}$  and  $T_B$ . It is only through the use of T-parameters that this simple matrix equation be written in this form.

$$\begin{pmatrix} T_{\text{measured}} \end{pmatrix} = \begin{pmatrix} T_A \end{pmatrix} \begin{pmatrix} T_{DUT} \end{pmatrix} \begin{pmatrix} T_B \end{pmatrix}$$

This matrix operation will represent the T-parameters of the test fixture and DUT when measured by the VNA at the measurement plane. General matrix theory states that if a matrix determinate is not equal to zero, then the matrix has an inverse and any matrix multiplied by its inverse will result in the identity matrix. For example, if we multiply the following T-parameter matrix by its inverse matrix, we obtain the identity matrix. It is

our goal to de-embed the two sides of the fixture, TA and TB, and gather the information from the DUT or TDUT. Extending this matrix inversion to the case of the cascaded fixture and DUT matrices, we can multiply each side of the measured result by the inverse T-parameter matrix of the fixture and yield the T-parameter for the DUT only. The T-parameter matrix can then be converted back to the desired S-parameter matrix using the equations given above.

$$\begin{pmatrix} T_A \end{pmatrix}^{-1} \begin{pmatrix} T_A \end{pmatrix} \begin{pmatrix} T_{DUT} \end{pmatrix} \begin{pmatrix} T_B \end{pmatrix} \begin{pmatrix} T_B \end{pmatrix}^{-1} = \begin{pmatrix} T_{DUT} \end{pmatrix}$$

Using the S or T-parameter model of the test fixture and VNA measurements of the total combination of the fixture and DUT, we can apply the above matrix equation to de-embed the fixture from the measurement. The process is implemented after the measurements are captured from the VNA. *Looking at the whole process of de-embedding, the most difficult part is creating an accurate model of the test fixture.* Because of the variety of printed circuit types and test fixture designs, there are no simple textbook formulations for creating an exact model. Nonetheless, many techniques can be used to aid the creation of fixture models, including simulation tools such as Agilent Advanced Design System (ADS) and other field solver tools, 2D and 3D alike.

In the following sections, we use two examples to demonstrate generation of model for test fixtures. The first example is a test fixture for extracting material properties of FPGA package epoxy material. Although fixture is insertable, de-embedding the fixture play a critical role in measurement accuracy and data convergence. The second example features a non-insertable fixture with one end FPGA ball pad (planar) and the other end coaxial SMA connector. Additional S-parameter measurement on fixture is required in order to obtain fixture model. Microwave CST field solver is employed to validate the after-de-embed measurement result.

All measurements are performed with using Agilent 4-port PNA, a powerful yet convenient tool for S-parameter measurement. Most de-embedding work is done in Agilent ADS.

### **III. FPGA Test Fixture De-Embedding**

The first example is about test substrate specially designed for material property extraction. In this measurement, the property of dielectric constant and loss tangent are extracted through S-parameter measurement on specially designed transmission lines or test coupons. Owing to the small feature size, use of probes is recommended. The transmission line portion provides the information needed for extraction, and the probe launch pad must be removed from measurement. Figure 5 shows the test coupon with the launch pad and micro-strip type transmission line.

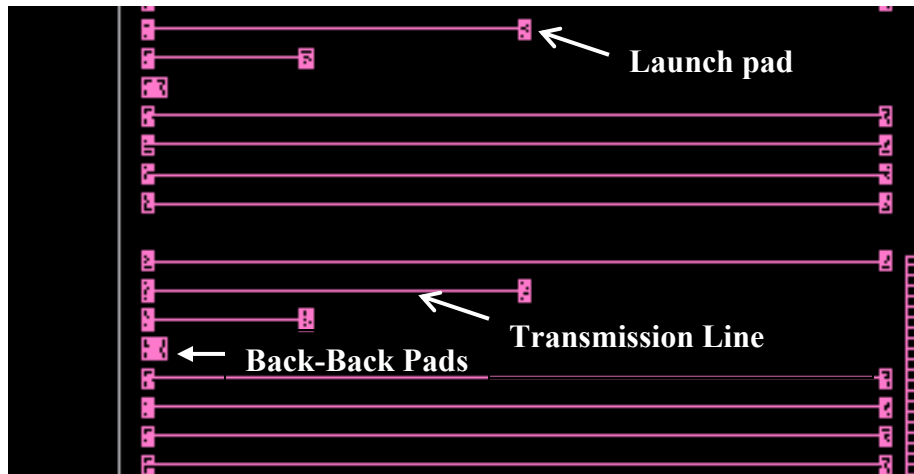


Figure 5. Test Coupon for De-Embedding

To obtain the launch pad model, we designed a “zero”-length transmission line feature with two launch pads facing each other, referred to as “back-back” pads. The whole process has two steps. First, a nominal measurement is performed on each coupon trace, and then an additional measurement is performed on the back-back pads. The latter is to be used for the launch fixture model. Still, the S-parameter file for the back-back pad includes combined effect of two pads, namely, FA and FB. The separation is accomplished by constructing an equivalent circuit with two identical portions. By curve fitting an equivalent circuit parameter to the measurement of the back-back pads, an accurate-yet-separate representation of each FA or FB can be obtained. The last step is to de-embed FA and FB from each side of the entire coupon measurement using the matrix operation as shown in the previous section.

The significance of de-embedding to the accuracy of data is very apparent from the comparison graphs below. In Figure 6, the first chart shows dielectric constant versus frequency, which is extracted with de-embedding implemented. The multiple lines represent dielectric constants extracted from coupons of different feature. In an ideal situation, all should give an identical constant at any single frequency point. In this graph, multiple lines are close to each other, indicating good convergence and validity of the result. As a comparison, the second graph demonstrates the same process *without* de-embedding. As a result, the dielectric constant scatters a wide range. It proves the experiment without de-embedding has a flaw in reaching valid values for packaging materials.

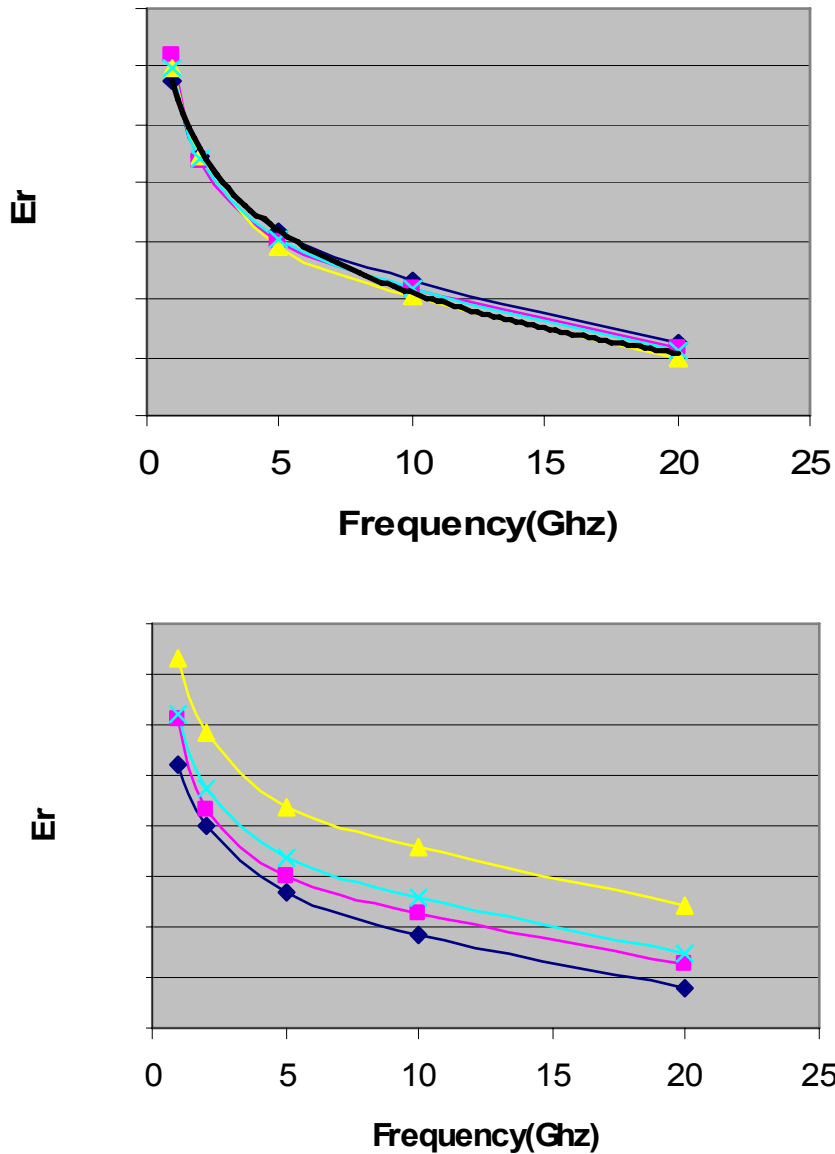


Figure 6. Comparison of Extracted Dielectric Constant With and Without De-Embedding

#### IV. FPGA Non-Insertable Test Fixture De-Embedding

A common setup for FPGA characterization is to use edge SMA connectors connecting multiple high-speed lanes from the test board to the oscilloscope and PRBS. This is important to gigabit signals because the fidelity of the connection through the coaxial connector is high in comparison to hand-held probes. One of the test boards is shown in Figure 1. As discussed in the previous section, the PCB effect needs to be removed or de-embedded to characterize the true performance of the FPGA. To make the test result

PCB independent, the portion from the FPGA ball pad to the edge SMA must be de-embedded. How to extract a representative model for this portion has become a challenging task for many test engineers.

Another application case is when performing frequency transfer response measurement between pad and SMA. A valid calibration needs to be performed prior to the S-parameter measurement, which requires SOLT calibrations between the two ports of pad and SMA. Since the probe and coaxial cable are not insertable, the calibration cannot be carried out, rendering S-parameter measurement questionable. A schematic drawing for the measurement setup is shown in Figure 7.

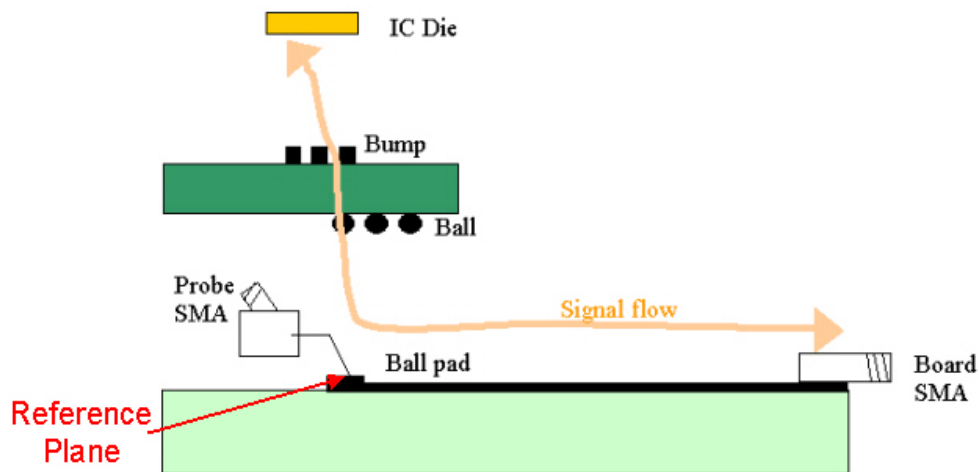


Figure 7. Schematic Drawing of Non-Insertable Measurement Case

In Figure 7, the signal flow is from the IC die through the package to the PCB, and connected to the test instrument through the SMA connector. Our objective is to characterize the signal path between the ball pads to the SMA and de-embed this portion from the final results. If we can find a way to accurately de-embed the probe, then the frequency response from the pad to the SMA is also accurate. In microwave terms, the goal becomes how to move the reference plane from the backside SMA of the probe to its tip, as indicated by the red mark.

Figure 8 shows the four-port S-parameter measurement setup with a port assignment using Agilent PNA. Ports 1 and 3 are assigned on the pad, whereas Ports 2 and 4 are on the edge SMA. If desired, the four-port S-parameters can be readily translated into differential S-parameters by Agilent PLTS software. In this measurement, the calibration is performed between coaxial cable connectors. One cable is connected to the PCB edge SMA and the other is connected to the SMA on the backside of probe. Since both are coaxial, the calibration can be readily performed. The measurement is saved and named as “Fixture” file, representing not the ball pad to the SMA, but rather SMA to SMA. Thus, work is left to de-embed the SMA (of probe) to the probe tip from the “Fixture” file.

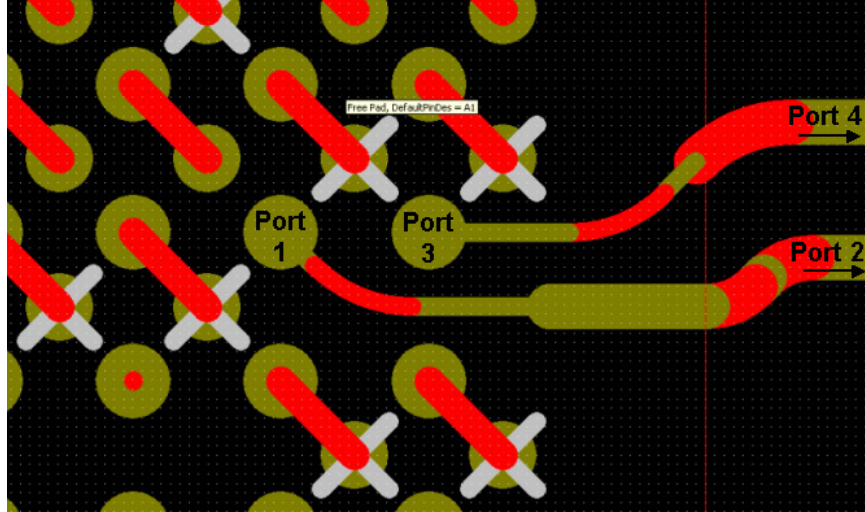


Figure 8. Four-Port S-Parameter Measurement Setup and Port Assignment

The process we proposed for the extraction of the probe model between its backside SMA and tip has two steps. First, choose two identical probes with the same pitch but reversed polarity—GS (ground-signal) and SG respectively. Locate both on the “Open” pattern of the probe calibration substrate, as shown in Figure 9.

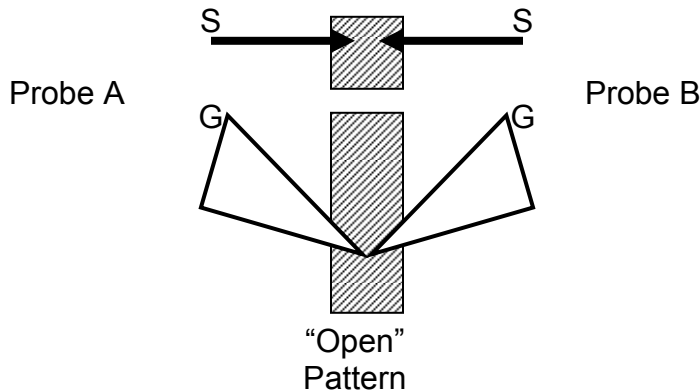


Figure 9. Probe Model Extraction Setup

Perform a two-port S-parameter measurement and save the file as a back-back probe. Construct a two-port equivalent circuit with two identical halves, simulate the S-parameter sweep and optimize circuit parameters until a good correlation is reached between the back-back probe file and equivalent circuits in all four S-parameters. One of the halves now represents the model for one probe, either A or B. Applying a half model in the de-embedding process with the “Fixture” file, the result is the frequency response of the ball pad and edge SMA. Its time domain counterpart is the impulse response for the portion and can be deconvolved from FPGA system measurements such as waveforms and eye diagrams.

Figure 10 shows the reflection comparison before and after de-embedding is performed. It is evident that by removing the probe signal, the reflection is improved. The reflection is due to two impedance discontinuities embedded in the probe: the SMA connector on the back and the contact of the probe's tip to the ball pad. Both are removed by the de-embedding process, thus the return loss is improved by as much as -6 dB in the non-resonance portion and -20 dB in the resonance portion.

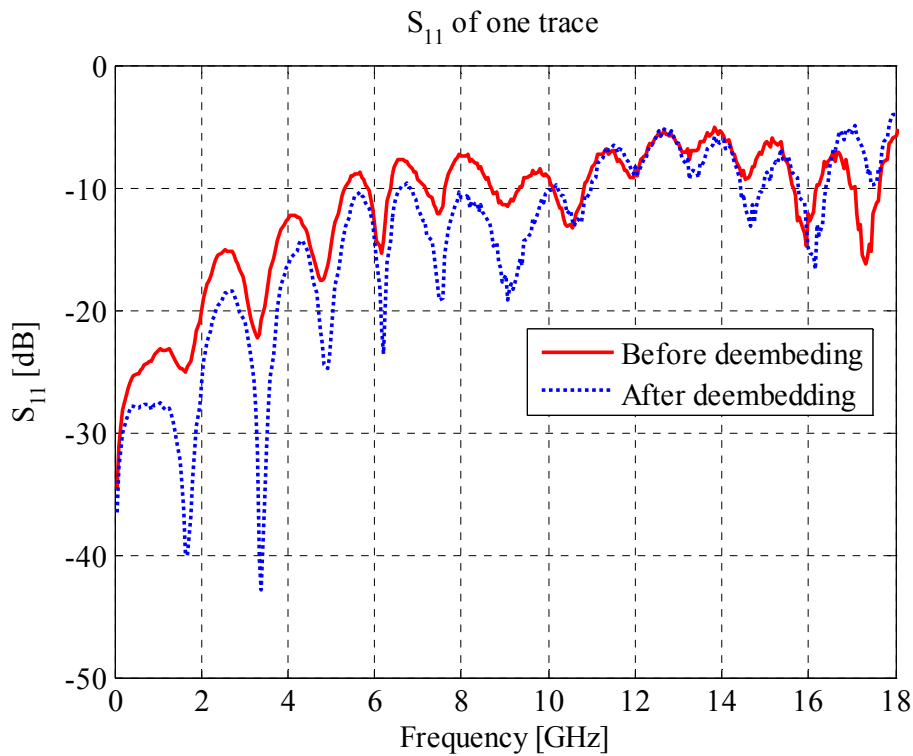


Figure 10. Return Loss of Ball-SMA Portion Before and After Probe De-Embedded

Figure 11 shows the frequency transfer response of the portion between the ball and the SMA. It is not surprising to see the enhanced frequency response as a result of the discontinuity being removed. To validate the process of de-embedding the non-insertable fixture, we resort to a 3D field solve and model the same portion including the ball pad and edge SMA. Figure 12 is a comparison between measured and modeled with CST Microwave Studio solver, in which a good correlation is achieved.

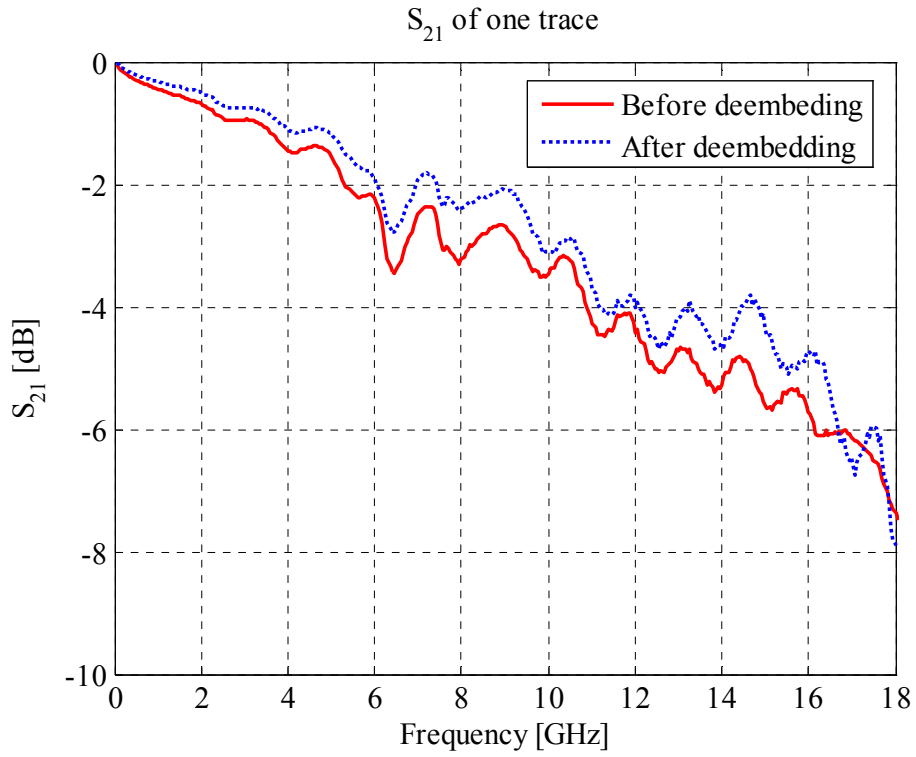
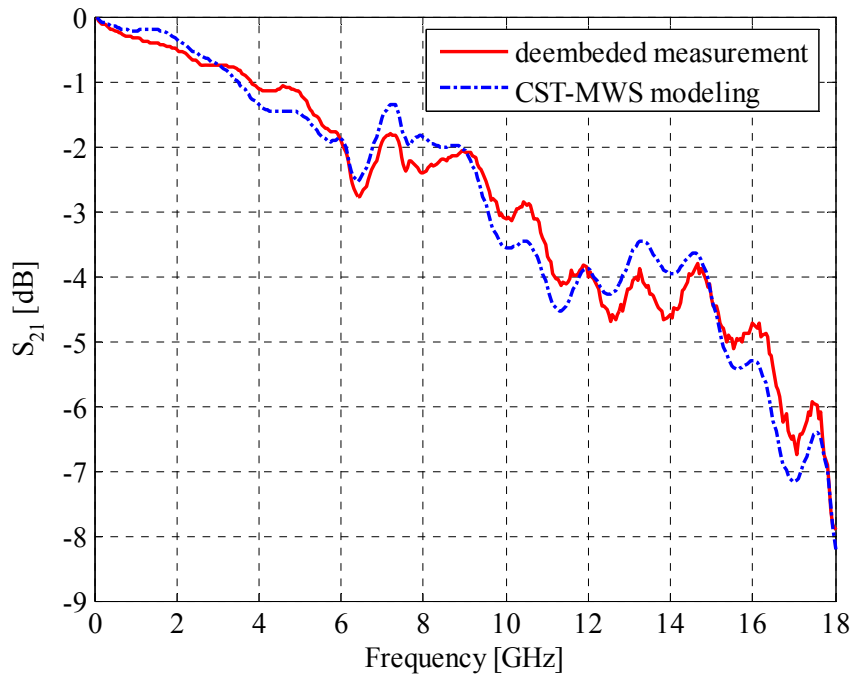


Figure 11. Frequency Response of Ball-SMA Portion Before and After De-Embedding



## **V. Summary**

We showed a process that can be used to extract models for fixtures that are not insertable. Two example cases are described to demonstrate the robustness of the methodology, one for accurate material property extraction and the second for a high-speed FPGA transceiver test board. The field solver model correlates well with our measurement-extracted result.

## **Acknowledgements**

The authors wish to thank Mike Resso of Agilent for his insightful discussions and for the equipment support of the Agilent 4-port PNA and PLTS software. The authors also wish to thank Orlando Bell of Gigatest Lab for his valuable technical discussions about material property measurement.



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