

FPGAs Provide Reconfigurable DSP Solutions

Razak Mohammedali
Product Marketing Engineer
Altera Corporation

DSP processors are widely used for implementing many DSP applications. Although DSP processors are programmable through software, the DSP processor hardware architecture is not flexible.

FPGAs provide a reconfigurable solution for implementing DSP applications as well as higher DSP throughput and raw data processing power than DSP processors. Since FPGAs can be reconfigured in hardware, FPGAs offer complete hardware customization while implementing various DSP applications.

Designing with FPGAs for DSP applications has been considered to be difficult mainly due to lack of a C-based design flow that is well-integrated with system level tools such as MATLAB and Simulink. Recently FPGA vendors have introduced new design tools and hardware features that alleviate the design flow problem by incorporating a C code-based design-flow option that mirrors the traditional DSP design flow.

FPGAs now provide a cost-effective alternative for DSP implementation that can be adopted easily for a broad range of applications such as 3G Wireless, voice over Internet protocol (VoIP), multimedia systems, radar and satellite systems, medical systems, image-processing applications and consumer electronics.

DSP-Enhanced FPGAs

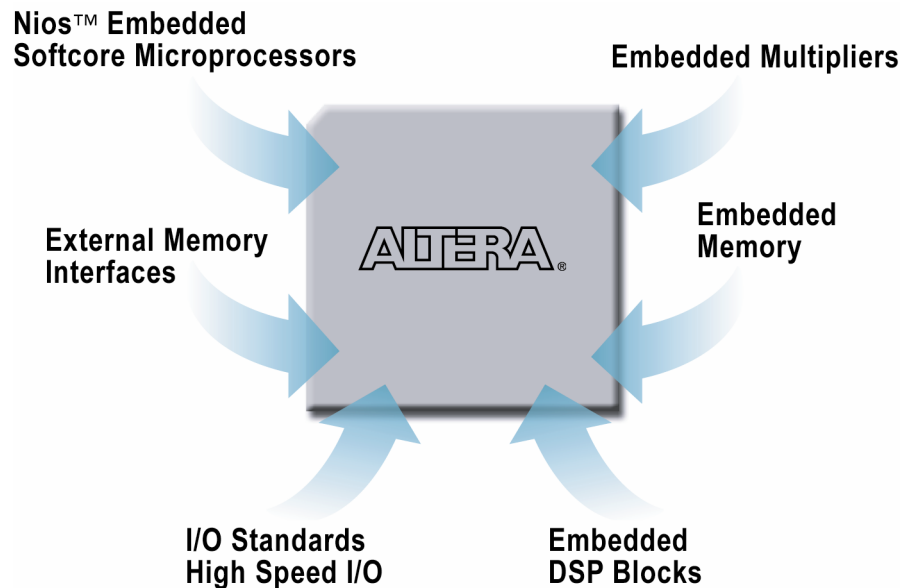
Leading-edge FPGAs, such as the Stratix devices available from Altera, incorporate embedded DSP features in their devices as shown in Figure 1. These embedded features provide functionality such as multiplication, accumulation, addition/subtraction, and summation that are commonly used in DSP functions. For example, Stratix device DSP blocks offer up to 224 multipliers that can perform 224 multiplications in a single clock cycle.

Compared to DSP processors that only offer a limited number of multipliers, Altera FPGAs offer much more multiplier bandwidth. Since one determining factor of the overall DSP bandwidth is the multiplier bandwidth, the overall DSP bandwidth of FPGAs can be much higher than the DSP processors. For example, Stratix device DSP blocks can deliver 70 GMACS of DSP throughput while leading DSP processors available today can deliver only up to 4.8 GMACS.

Various DSP applications use external memory devices to manage large amounts of data processing. The embedded memory in FPGAs meets these requirements and also eliminates the need for external memory devices in certain cases. For example, the Stratix

device family offers up to 10 Mbits of embedded memory through the TriMatrix™ memory feature.

Figure 1. DSP Features in Leading Altera FPGAs



Further designers can implement soft-core processors such as the Nios embedded processor in FPGAs and add multiple system peripherals. The Nios processor supports a user-determinable multi-master bus architecture that optimizes the bus bandwidth and removes potential bottlenecks found in DSP processors. Designers can use multi-master buses to define as many buses and as much performance as needed for a particular application. Off-the-shelf DSP processors make compromises between size and performance when they choose the number of data buses on the chip, potentially limiting performance.

Soft embedded processors in FPGAs provide access to custom instructions such as the “MUL” instruction in Nios processors that can perform a multiplication operation in two clock cycles using hardware multipliers.

Hardware Acceleration in FPGAs

FPGA devices provide a flexible platform to accelerate performance-critical functions in hardware because of the configurability of the device’s logic resources. Unlike DSP processors that have predefined hardware accelerator blocks, FPGAs can implement hardware accelerators for each application, allowing the designer to achieve the best performance through hardware acceleration. The designer can implement hardware accelerator blocks by designing such blocks using parametrizable IP functions or from scratch using HDL.

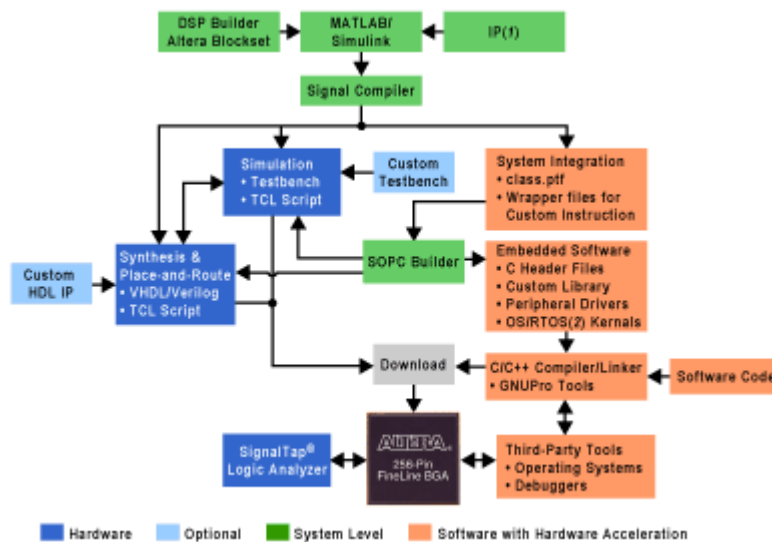
The flexibility of programmable logic and soft IP cores allows designers to quickly adapt their designs to new standards such as the Wireless 802.11a, Wireless Broadband Working Group 802.16, and HiperLAN/2 without waiting for long lead times usually associated with DSP processors.

DSP Design Flow in FPGAs

Traditionally, DSP designers had to implement their systems in FPGAs using the hardware flow based on a HDL language such as Verilog HDL and VHDL. New DSP tools such as DSP Builder, SOPC Builder, and a complete software development platform now enable DSP designers to follow a software-based design flow while targeting FPGAs as shown in Figure 2.

Altera FPGAs with embedded processors support a software-based design flow. Altera provides software development tools including the GNU Pro toolset for compiling, debugging, assembling and linking software designs. These software designs can then be downloaded to an FPGA using either on-chip RAM or an external memory device.

Figure 2. DSP Design Flow options for Altera FPGAs



Software Combined with Hardware Acceleration

Embedded processors and hardware acceleration offer the flexibility, performance, and cost effectiveness in a development flow that is familiar to software developers. A DSP designer can combine a software design flow along with hardware acceleration. For example, the developer can use Altera's DSP IP or develop their own custom instruction to accelerate those tasks in the FPGA. The system control code along with the other low-performance DSP algorithms can be run on a Nios embedded processor.

Altera also provides system-level tools such as SoPC Builder for system-level partitioning and integration. Designers can use SOPC Builder to build entire hardware systems by combining the embedded processor, such as a Nios embedded processor, system peripherals, as well as IP MegaCore functions.

Altera's DSP Builder tool provides an interface from Simulink directly to the FPGA hardware. The DSP Builder tool simplifies hardware implementation of DSP functions, provides a system-level verification tool to the system engineer who is not necessarily familiar with HDL design flow, and allows the system engineer to implement DSP functions in FPGAs without learning HDL. Additionally, designers can incorporate the designs created by DSP Builder into a SOPC Builder system for a complete DSP system implementation.

Hardware Design Flow

DSP designers can also develop a pure hardware implementation of their DSP system using an HDL-based design flow. Altera provides a complete set of FPGA development tools including the Quartus II software and interfaces to other EDA tools such as Synopsys, Synplify, and Leonardo Spectrum. These tools enable hardware design, simulation, debug, and in-system verification of the DSP system. The suite of pre-optimized DSP IP MegaCore functions can simplify this development process. DSP engineers can also follow the DSP Builder design flow implement hardware-only DSP systems in FPGAs without learning HDL.

Cost Benefits of FPGAs

Historically, FPGAs have been viewed as more expensive than DSP processors. However, FPGAs provide much higher throughput than DSP processors as well as hardware flexibility, such that a single FPGA can accommodate an order of magnitude more channels than DSP processors without any degradation in performance. Hence in multi-channel applications, the cost per channel of an FPGA based solution can be much less expensive than an equivalent DSP solution.

As suggested by a benchmark study done by BDTI, (please refer to the *Focus* report "FPGAs for DSP" available from BDTI), FPGA devices enable orders of magnitude lower cost per channel compared to leading DSP processors available from DSP vendors today.

In addition, with the introduction of very low-cost FPGA families such as the recently announced Cyclone devices from Altera that are available for unit price of less than \$10, FPGAs also provide a very cost-effective solution for DSP implementation for certain applications where the device unit cost is key decision factor for the choice of implementation.

Hence FPGAs are now available at price points that are comparable to DSP processors.



101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
www.altera.com
Applications Hotline:
(800) 800-EPLD
Literature Services:
literature@altera.com

Copyright © 2005 Altera Corporation. All rights reserved. Altera, The Programmable Solutions Company, the stylized Altera logo, specific device designations, and all other words and logos that are identified as trademarks and/or service marks are, unless noted otherwise, the trademarks and service marks of Altera Corporation in the U.S. and other countries. All other product or service names are the property of their respective holders. Altera products are protected under numerous U.S. and foreign patents and pending applications, maskwork rights, and copyrights. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera Corporation. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

All copyrights reserved.