



Bank number	I/O Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Channel with OCT Rd (Note 2)	F1152	F780	F572	DQS for X4 for F1152	DQS for X8/9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note 3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)	DQS for X4 for F572	DQS for X8/9 for F572 (Note 3)	DQS for X16/X18 for F572 (Note 3)	
Q1.2			GXB TX1n					K32	C23													
Q1.2			GXB RX1n					K31	D23													
Q1.2			GXB TX1n					L34	A24													
Q1.2			GXB RX1n					L33	B24													
Q1.2			GXB TX1p					M32	A28													
Q1.2			GXB TX1p					M31	B28													
Q1.2			GXB RX1n					N34	C28													
Q1.2			GXB RX1p					N33	C27													
Q1.2			REFCLKp					R30	D26													
Q1.2			REFCLKp					R29	D25													
Q1.2			REFCLKp					S30	E28													
Q1.2			REFCLKp					S29	E27													
Q1.2			GXB TX0n					F32	F28													
Q1.2			GXB TX0p					F31	F25													
Q1.2			GXB RX0n					R34	G28													
Q1.2			GXB RX0p					R33	G27													
Q1.2			GXB TX0n					T32	H28													
Q1.2			GXB TX0p					T31	H25													
Q1.2			GXB RX0n					U34	J28													
Q1.2			GXB RX0p					U33	J27													
Q1.1			GXB TX7n					V32	K28	B22												
Q1.1			GXB TX7p					V31	K25	B21												
Q1.1			GXB RX7n					W34	L28	D24												
Q1.1			GXB RX7p					W33	L27	D23												
Q1.1			GXB TX0n					X32	M28	D22												
Q1.1			GXB TX0p					X31	M25	D21												
Q1.1			GXB RX0n					AA34	N28	E24												
Q1.1			GXB RX0p					AA33	N27	E23												
Q1.1			REFCLKp					W30	P26	F22												
Q1.1			REFCLKp					W29	P25	F21												
Q1.1			REFCLKn					AA30	R28	G24												
Q1.1			REFCLKn					AA29	R27	G23												
Q1.1			GXB TX0n					AB32	T26	H22												
Q1.1			GXB TX0p					AB31	T25	H21												
Q1.1			GXB RX0n					AC34	U28	J24												
Q1.1			GXB RX0p					AC33	U27	J23												
Q1.1			GXB TX4n					AD32	V26	K22												
Q1.1			GXB TX4p					AD31	V25	K21												
Q1.1			GXB RX4n					AE34	W28	L24												
Q1.1			GXB RX4p					AE33	W27	L23												
Q1.0			GXB TX3n					AF32	Y26	M22												
Q1.0			GXB TX3p					AF31	Y25	M21												
Q1.0			GXB RX3n					AG34	ZA28	N24												
Q1.0			GXB RX3p					AG33	ZA27	N23												
Q1.0			GXB TX2n					AH32	AB26	P22												
Q1.0			GXB TX2p					AH31	AB25	P21												
Q1.0			GXB RX2n					AJ34	AC28	R24												
Q1.0			GXB RX2p					AJ33	AC27	R23												
Q1.0			REFCLKp					AC30	AD26	T22												
Q1.0			REFCLKp					AC29	AD25	T21												
Q1.0			REFCLKn					AE30	AE26	U22												
Q1.0			REFCLKn					AE29	AE25	U21												
Q1.0			GXB TX1n					AK32	AH27	V22												
Q1.0			GXB TX1p					AK31	AH26	V21												
Q1.0			GXB RX1n					AL34	AH28	W24												
Q1.0			GXB RX1p					AL33	AH26	W23												
Q1.0			GXB TX0p					AM32	AY24	V22												
Q1.0			GXB TX0p					AM31	AY23	V21												
Q1.0			GXB RX0n					AN34	AA28	X24												
Q1.0			GXB RX0p					AN33	AA27	X23												
IC			HCONFG		HCONFG			AC36	AA24	V20												
IC			CONF_DONE		CONF_DONE			AE35	AA23	W18												
IC			MSEL3		MSEL3			AB26	AB24	T20												
IC			MSEL2		MSEL2			AD24	Y24	W20												
IC			MSEL1		MSEL1			AC25	Y23	V19												
IC			MSEL0		MSEL0			AC27	Y24	V19												
IC			STATUS		STATUS			AD26	W23	U18												
IC			MD_PULLUP		MD_PULLUP			AC28	AB22	V18												
IC			HCE		HCE			AB25	AA22	V18												
IA		VREFBIAND		PLL4_CLKOUT1n				AH28	G24	V18												
IA		VREFBIAND		R0ND				AL27	AB19	AB20												
IA		VREFBIAND		PLL4_CLKOUT1p				AH24	V24	W16												
IA		VREFBIAND		RUPD				AL25	AC19	AA20												
IA	BI01	VREFBIAND	ID			DIFFO_TX_B1n	DIFFN_B1n	AM29			DQ18B	DQ26	DQ46	DQ26								
IA	BI01	VREFBIAND	ID			DIFFO_KX_B1n	DIFFN_B1n	AM28			DQ18B	DQ26	DQ46	DQ26								
IA	BI01	VREFBIAND	ID			DIFFO_TX_B1p	DIFFN_B1p	AL28			DQ18B	DQ26	DQ46	DQ26								
IA	BI01	VREFBIAND	ID			DIFFO_KX_B1p	DIFFN_B1p	AM27			DQ18B	DQ26	DQ46	DQ26								
IA	BI01	VREFBIAND	ID			DIFFO_KX_B2n	DIFFN_B2n	AN28			DQS118B	DQ26	DQ46	DQ26								
IA	BI01	VREFBIAND	ID			DIFFO_TX_B2n	DIFFN_B2n	AJ24			DQS118B	DQ26	DQ46	DQ26								
IA	BI01	VREFBIAND	ID			DIFFO_KX_B2p	DIFFN_B2p	AN27			DQS118B	DQ26	DQ46	DQ26								
IA	BI01	VREFBIAND	ID			DIFFO_TX_B2p	DIFFN_B2p	AM26			DQS117B	DQS118B	DQ46	DQ26								
IA	BI01	VREFBIAND	ID			DIFFO_KX_B3n	DIFFN_B3n	AK22			DQ17B	DQ26	DQ46	DQ26								
IA	BI01	VREFBIAND	ID			DIFFO_TX_B3n	DIFFN_B3n	AM25	AC27	V21	DQS17B	DQS17B	DQ46	DQ26								
IA	BI01	VREFBIAND	ID			DIFFO_KX_B3p	DIFFN_B3p	AJ22			DQ17B	DQ26	DQ46	DQ26								
IA	BI01	VREFBIAND	ID			DIFFO_TX_B3p	DIFFN_B3p	AP23			DQ17B	DQ26	DQ46	DQ26								
IA	BI01	VREFBIAND	ID			DIFFO_KX_B4n	DIFFN_B4n	AP23			DQ17B	DQ26	DQ46	DQ26								
IA	BI01	VREFBIAND	ID			DIFFO_TX_B4n	DIFFN_B4n	AP20			DQ17B	DQ26	DQ46	DQ26								
IA	BI01	VREFBIAND	ID			DIFFO_KX_B4p	DIFFN_B4p	AP21			DQ17B	DQ26	DQ46	DQ26								
IA	BI02	VREFBIAND	ID			DIFFO_TX_B5n	DIFFN_B5n	AM24	AD21	AC21	DQ16B	DQ26	DQ46	DQ26								
IA	BI02	VREFBIAND	ID			DIFFO_KX_B5n	DIFFN_B5n	AM23	AC17	AD21	DQ16B	DQ26	DQ46	DQ26								
IA	BI02	VREFBIAND	ID			DIFFO_TX_B5p	DIFFN_B5p	AL24	AC21	AD21	DQ16B	DQ26	DQ46	DQ26								
IA	BI02	VREFBIAND	ID			DIFFO_KX_B5p	DIFFN_B5p	AL23	AB17	AD20	DQ16B	DQ26	DQ46	DQ26								
IA	BI02	VREFBIAND	ID	INT_DONE		DIFFO_KX_B6n	DIFFN_B6n	AM21	V22	V19	DQS118B	DQ26	DQ46	DQ26								
IA	BI02	VREFBIAND	ID			DIFFO_KX_B6n	DIFFN_B6n	AM20	V21	W19	DQ18B	DQ26	DQ46	DQ26								
IA	BI02	VREFBIAND	ID			DIFFO_TX_B6n	DIFFN_B6n	AM22	W21	AC18	DQS118B	DQ26	DQ46	DQ26								
IA	BI02	VREFBIAND	ID			DIFFO_KX_B6p	DIFFN_B6p	AP26	AB16	AB16	DQS118B	DQ26	DQ46	DQ26								
IA	BI02	VREFBIAND	ID			DIFFO_TX_B7n	DIFFN_B7n															









Pin Information for the Arria® II GX EP2AG125 Device  
Version 1.1

Bank number	I/O Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated TX/RX Channel with DCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no DCT Rd (Note 2)	F152	F780	F572	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note 3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)	DQS for X4 for F572	DQS for X8/X9 for F572 (Note 3)	DQS for X16/X18 for F572 (Note 3)
BA	IT04	VREFBAND	ID			DIFFO_TX_T23n	DIFFIN_T23n	F19	G15	F13	DQSxT	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T
BA	IT04	VREFBAND	ID			DIFFO_KX_T24p	DIFFOUT_T24p	G19	A20	D14											
BA	IT04	VREFBAND	ID			DIFFO_TX_T25p	DIFFIN_T25p	G11	B15	D07	DQ4T	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T
BA	IT04	VREFBAND	ID			DIFFO_KX_T24n	DIFFOUT_T24n	F19	A19	D13											
BA	IT04	VREFBAND	ID			DIFFO_TX_T24n	DIFFIN_T24n	A20	B19	A14	DQ4T	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T
BA	IT03	VREFBAND	ID			DIFFO_KX_T25p	DIFFOUT_T25p	G21	D17	DQ6T	DQ4T	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T
BA	IT03	VREFBAND	ID			DIFFO_TX_T25n	DIFFIN_T25n	K20	L15												
BA	IT03	VREFBAND	ID			DIFFO_KX_T25n	DIFFOUT_T25n	G01	G17	DQ6T	DQ4T	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T
BA	IT03	VREFBAND	ID			DIFFO_TX_T25n	DIFFIN_T25n	G20	K15	DQ6T	DQ4T	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T
BA	IT03	VREFBAND	ID			DIFFO_KX_T26p	DIFFOUT_T26p	E19	D18												
BA	IT03	VREFBAND	ID			DIFFO_TX_T26p	DIFFIN_T26p	A23	D21	A18	DQSxT	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T
BA	IT03	VREFBAND	ID			DIFFO_KX_T26n	DIFFOUT_T26n	E18	C18	DQ6T	DQ4T	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T
BA	IT03	VREFBAND	ID			DIFFO_TX_T26n	DIFFIN_T26n	A22	C21	A17	DQSxT	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T
BA	IT03	VREFBAND	ID			DIFFO_KX_T27p	DIFFOUT_T27p	E22	D20												
BA	IT03	VREFBAND	ID			DIFFO_TX_T27p	DIFFIN_T27p	F19	G17	DQSxT	DQ4T/CO4T	DQ4T	DQ4T/CO4T	DQSxT	DQ4T/CO4T	DQSxT	DQ4T/CO4T	DQSxT	DQ4T/CO4T	DQSxT	DQ4T/CO4T
BA	IT03	VREFBAND	ID			DIFFO_KX_T27n	DIFFOUT_T27n	G22	D19	DQ6T	DQ4T	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T
BA	IT03	VREFBAND	ID			DIFFO_TX_T27n	DIFFIN_T27n	F19	F17	DQSxT	DQ4T	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T
BA	IT03	VREFBAND	ID			DIFFO_KX_T28p	DIFFOUT_T28p	G24	L19												
BA	IT03	VREFBAND	ID			DIFFO_TX_T28p	DIFFIN_T28p	G25	L21	DQ6T	DQ4T	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T
BA	IT03	VREFBAND	ID			DIFFO_KX_T28n	DIFFOUT_T28n	A24	K20	DQ6T	DQ4T	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T
BA	IT03	VREFBAND	ID			DIFFO_TX_T28n	DIFFIN_T28n	A25	J20	DQ6T	DQ4T	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T
BA	IT02	VREFBAND	ID			DIFFO_KX_T29p	DIFFOUT_T29p	A27	F22	D15	DQ4T	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T
BA	IT02	VREFBAND	ID			DIFFO_TX_T29p	DIFFIN_T29p	G21	K16	G14	DQ4T	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T
BA	IT02	VREFBAND	ID			DIFFO_KX_T29n	DIFFOUT_T29n	A26	G22	C19	DQ4T	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T
BA	IT02	VREFBAND	ID			DIFFO_TX_T29n	DIFFIN_T29n	G20	J16	F14	DQ4T	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T
BA	IT02	VREFBAND	ID			DIFFO_KX_T30p	DIFFOUT_T30p	G21	G24	C16											
BA	IT02	VREFBAND	ID			DIFFO_TX_T30p	DIFFIN_T30p	G28	F24	A16	DQSxT	DQ4T/CO4T	DQ4T/CO4T	DQSxT	DQ4T/CO4T	DQSxT	DQ4T/CO4T	DQSxT	DQ4T/CO4T	DQSxT	DQ4T/CO4T
BA	IT02	VREFBAND	ID			DIFFO_KX_T30n	DIFFOUT_T30n	G20	F23	B16	DQ4T	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T
BA	IT02	VREFBAND	ID			DIFFO_TX_T30n	DIFFIN_T30n	G27	E24	A15	DQSxT	DQ4T/CO4T	DQ4T/CO4T	DQSxT	DQ4T/CO4T	DQSxT	DQ4T/CO4T	DQSxT	DQ4T/CO4T	DQSxT	DQ4T/CO4T
BA	IT02	VREFBAND	ID			DIFFO_KX_T31p	DIFFOUT_T31p	G23	F21	D23											
BA	IT02	VREFBAND	ID			DIFFO_TX_T31p	DIFFIN_T31p	G23	K18	F19	DQSxT	DQ4T/CO4T	DQ4T/CO4T	DQSxT	DQ4T/CO4T	DQSxT	DQ4T/CO4T	DQSxT	DQ4T/CO4T	DQSxT	DQ4T/CO4T
BA	IT02	VREFBAND	ID			DIFFO_KX_T31n	DIFFOUT_T31n	A24	L17	DQ6T	DQ4T	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T
BA	IT02	VREFBAND	ID			DIFFO_TX_T31n	DIFFIN_T31n	G23	J17	E15	DQSxT	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T
BA	IT02	VREFBAND	ID		CRC ERROR	DIFFO_KX_T32p	DIFFOUT_T32p	E24	E19	C19											
BA	IT02	VREFBAND	ID			DIFFO_TX_T32p	DIFFIN_T32p	G24	A23	A20	DQ4T	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T
BA	IT02	VREFBAND	ID			DIFFO_KX_T32n	DIFFOUT_T32n	E24	E18	B18	DQ4T	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T
BA	IT02	VREFBAND	ID			DIFFO_TX_T32n	DIFFIN_T32n	G25	G18	A19	DQ4T	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T	DQ4T	DQSxT	DQ4T	DQ4T
BA	IT01	VREFBAND	ID			DIFFO_KX_T33p	DIFFOUT_T33p	F21	G17												
BA	IT01	VREFBAND	ID			DIFFO_TX_T33p	DIFFIN_T33p	N20													
BA	IT01	VREFBAND	ID			DIFFO_KX_T33n	DIFFOUT_T33n	G21													
BA	IT01	VREFBAND	ID			DIFFO_TX_T33n	DIFFIN_T33n	A20													
BA	IT01	VREFBAND	ID			DIFFO_KX_T34p	DIFFOUT_T34p	G27													
BA	IT01	VREFBAND	ID			DIFFO_TX_T34p	DIFFIN_T34p	G25													
BA	IT01	VREFBAND	ID			DIFFO_KX_T34n	DIFFOUT_T34n	F27													
BA	IT01	VREFBAND	ID			DIFFO_TX_T34n	DIFFIN_T34n	G26													
BA	IT01	VREFBAND	ID			DIFFO_KX_T35p	DIFFOUT_T35p	L22													
BA	IT01	VREFBAND	ID			DIFFO_TX_T35p	DIFFIN_T35p	L22													
BA	IT01	VREFBAND	ID			DIFFO_KX_T35n	DIFFOUT_T35n	G22													
BA	IT01	VREFBAND	ID			DIFFO_TX_T35n	DIFFIN_T35n	G22													
BA	IT01	VREFBAND	ID			DIFFO_KX_T36p	DIFFOUT_T36p	G29													
BA	IT01	VREFBAND	ID			DIFFO_TX_T36p	DIFFIN_T36p	G29													
BA	IT01	VREFBAND	ID			DIFFO_KX_T36n	DIFFOUT_T36n	G28													
BA	IT01	VREFBAND	ID			DIFFO_TX_T36n	DIFFIN_T36n	G29													
BA					RLP2			G28	L21	C20											
BA					PLL1_CLKOUT1p			A21	K19	H16											
BA					PLL1_CLKOUT1n			G28	K21	B19											
BA					PLL1_CLKOUT2p			L21	J18	G18											
BA					PLL1_CLKOUT2n			F26	F20	D17											
BA					PLL1_CLKOUT3p			K21	J19	F16											
BA					PLL1_CLKOUT3n			G25	F19	C18											
BA					PLL1_CLKOUT3n			G21	H19	E16											
BC					TD0			A27	L20	G22											
BC					ASD0			K27	J22	J20											
BC					RCSD			M26	H22	H19											
BC					DA7A0			N26	H22	F19											
BC					TD1			M25	H24	G19											
BC					IMS			N25	J23	G17											
BC					TC0			L24	L24	D18											
BC					DCLK		DCLK	L25	K24	P20											
BC					GND			H17	F14	H13											
BC					GND			A27	AB2	F18											
BC					GND			M28	G22	G20											
BC					GND			N27	K23	D18											
BC					GND			F24	F28	F24											
BC					GND			F23	F27	F23											
BC					GND			F30	W26	W22											
BC					GND			F28	W26	W21											
BC					GND			F27	F28	F28											
BC					GND			F25	F27	F23											
BC					GND			M32	J26	J22											
BC					GND			G01	L25	G21											
BC					GND			W28	F28	F24											
BC					GND			W26	F27	F23											
BC					GND			F24	F24	F24											
BC					GND			F33	F22	R21											
BC					GND			L29	R28	F19											
BC					GND			F29	R25	P24											
BC					GND			F27	R23	P23											
BC					GND			F25	R21	P25											



Bank number	I/O Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated TX/RX Channel with DOCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no DOCT Rd (Note 2)	F1152	F780	F572	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note 3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)	DQS for X4 for F572	DQS for X8/X9 for F572 (Note 3)	DQS for X16/X18 for F572 (Note 3)	
			GND					L32	D27	B24												
			GND					L31	D28	B23												
			GND					K34	D22	AC23												
			GND					K33	C26	AC23												
			GND					K30	C28	AB24												
			GND					K29	C24	AB23												
			GND					M32	C22	AB22												
			GND					H31	B28	AA22												
			GND					H34	B27	AA21												
			GND					M33	B25	A23												
			GND					P32	B23	V22												
			GND					G31	B22	A21												
			GND					F34	B21	F8												
			GND					F33	AF26	V5												
			GND					E32	AH24	V20												
			GND					H31	AH22	V2												
			GND					H34	AH20	V17												
			GND					D33	AG28	V14												
			GND					D32	AG26	V11												
			GND					E31	AG24	W6												
			GND					B34	AG22	U19												
			GND					B33	AG21	U6												
			GND					B30	AG20	U5												
			GND					B29	AF28	U28												
			GND					B28	AF27	U27												
			GND					AP33	AF26	U17												
			GND					AP32	AE25	U14												
			GND					AP30	AF23	U11												
			GND					AN32	AE26	T14												
			GND					AN31	AE25	T12												
			GND					AN30	AE23	T10												
			GND					AM34	AD28	H7												
			GND					AM33	AD27	H17												
			GND					AL32	AC26	R15												
			GND					AL31	AC25	R13												
			GND					AK34	AB28	R11												
			GND					AK33	AB27	H6												
			GND					AL32	AA26	PF												
			GND					AL31	AA25	P2												
			GND					AK34	AG27	P18												
			GND					AK33	AG25	P15												
			GND					AG32	AG23	P12												
			GND					AG31	AG21	N6												
			GND					AF34	Y7	N16												
			GND					AF33	W9	M6												
			GND					AF30	W22	M14												
			GND					AF29	W19	L5												
			GND					AE34	W17	L15												
			GND					AE31	W15	H6												
			GND					AD34	VB	K12												
			GND					AD33	V5	J15												
			GND					AD30	V20	H5												
			GND					AD29	V2	H4												
			GND					AC32	V18	F6												
			GND					AC31	V16	E17												
			GND					AB34	V14	BB												
			GND					AB33	V12	B14												
			GND					AB30	V10	AC20												
			GND					AM29	U6	AC17												
			GND					AM27	U17	J17												
			GND					AK32	U13	H6												
			GND					AK31	T8	H7												
			GND					AA28	T20	F18												
			GND					AA26	T18	E2												
			GND					AK33	T14	H6												
			GND					AK32	T10	B17												
			GND					AK31	R18	AC20												
			GND					AK30	R13	AC14												
			GND					A28	P18	P16												
			GND					P23	P12	N17												
			GND					F21	N9	N11												
			GND					F19	N5	M16												
			GND					F17	N19	L6												
			GND					F15	N15	L17												
			GND					F13	N11	L13												
			GND					M8	M16	K14												
			GND					M5	M12	J6												
			GND					M22	L1	J11												
			GND					M20	L20	H2												
			GND					M2	L17	H6												
			GND					M18	L11	E20												
			GND					M14	H5	E11												
			GND					M14	H17	BB												
			GND					M11	G9	AC3												
			GND					V23	E20	AC17												
			GND					V21	E17	N17												
			GND					V19	B2	M18												
			GND					V15	AG8	M10												
			GND					V13	AG14	L2												
			GND					U22	AD20	L13												
			GND					U20	AD11	K16												
			GND					M18	AK20	K16												
			GND					J16	AA11	J13												
			GND					M14	U19	H20												
			GND					F5	U15	M15												
			GND					F5	U11	E5												
			GND					F23	T5	E14												
			GND					F21	T2	B20												
			GND					F2	T16	B11												
			GND					F19	T12	AC2												
			GND					F17	R9													
			GND					F13	R17													
			GND					F13	R11													
			GND					F11	P16													
			GND					M22	P10													
			GND					AC20	N5													
			GND					R18	N2													
			GND					R16	N17													
			GND					R14	N13													
			GND					P6	M18													



Bank number	I/O Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated TX/Rx Channel with DOCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no DOCT Rd (Note 2)	F1152	F780	F572	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note 3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)	DQS for X4 for F572	DQS for X8/X9 for F572 (Note 3)	DQS for X16/X18 for F572 (Note 3)	
			GND					P19	H8													
			GND					P17	H2													
			GND					P15	H11													
			GND					P13	E23													
			GND					P11	E14													
			GND					N24	B20													
			GND					N22	B11													
			GND					N18	AD17													
			GND					N16	AD5													
			GND					N14	AD14													
			GND					N12	AD5													
			GND					L8	AA14													
			GND					L5	AA0													
			GND					L26	H14													
			GND					L23	E5													
			GND					L20	E17													
			GND					L2	B5													
			GND					L17	B14													
			GND					L14	AG2													
			GND					K10	AD8													
			GND					J9	AD17													
			GND					J8	AA8													
			GND					H5	AA17													
			GND					H29	E8													
			GND					H28	E2													
			GND					H23	BB													
			GND					H20	B17													
			GND					H2	AG5													
			GND					H17	AD11													
			GND					H14	AD2													
			GND					H11	AB23													
			GND					E5	AA2													
			GND					E29														
			GND					E26														
			GND					E23														
			GND					E20														
			GND					E2														
			GND					E17														
			GND					E14														
			GND					E11														
			GND					B8														
			GND					B5														
			GND					B26														
			GND					B23														
			GND					B20														
			GND					B2														
			GND					B17														
			GND					B11														
			GND					AN5														
			GND					AN28														
			GND					AN20														
			GND					AN17														
			GND					AN11														
			GND					AK5														
			GND					AK26														
			GND					AK20														
			GND					AK17														
			GND					AK14														
			GND					AK11														
			GND					AK5														
			GND					AG28														
			GND					AG20														
			GND					AG17														
			GND					AD11														
			GND					AD5														
			GND					AD29														
			GND					AD2														
			GND					AD14														
			GND					AB21														
			GND					AB17														
			GND					AB13														
			GND					AK25														
			GND					AK2														
			GND					AK11														
			GND					B14														
			GND					KN8														
			GND					KN28														
			GND					KN23														
			GND					KN2														
			GND					KN14														
			GND					AK8														
			GND					AK29														
			GND					AK23														
			GND					AK2														
			GND					AK14														
			GND					AG8														
			GND					AG29														
			GND					AG21														
			GND					AG2														
			GND					AG14														
			GND					AF9														
			GND					AD8														
			GND					AD20														
			GND					AD17														
			GND					AB21														
			GND					AB19														
			GND					AB15														
			GND					AK5														
			GND					AK20														
			GND					AK14														
			GND					AK8														
			GND					AK22														
			GND					AK18														
			GND					AA18														
			VCC					V16	P15	BM3												
			VCC					V24	V20	V22												
			VCC					V22	W18	19												
			VCC					V20	W16	117												
			VCC					V18	W14	115												
			VCC					V16	V8	113												
			VCC					V14	V21	111												
			VCC					V23	V19	86												
			VCC					W21	V17	R16												



Bank number	I/O Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated TX/RX Channel with DOCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with DOCT Rd (Note 2)	F1152	F780	F572	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note 3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)	DQS for X4 for F572	DQS for X8/X9 for F572 (Note 3)	DQS for X16/X18 for F572 (Note 3)
			VCC					M19	V15	R14											
			VCC					M17	V13	R12											
			VCC					M15	V11	R10											
			VCC					M13	U20	P9											
			VCC					U24	U18	P17											
			VCC					U22	U16	P15											
			VCC					V20	U14	P13											
			VCC					V18	U12	P11											
			VCC					V14	U10	N8											
			VCC					U21	T9	N18											
			VCC					V19	T5	N16											
			VCC					U15	T17	N14											
			VCC					U13	T15	N10											
			VCC					T24	T13	M8											
			VCC					T22	T11	M16											
			VCC					T20	R18	M11											
			VCC					T18	R16	L8											
			VCC					T16	R14	L16											
			VCC					T14	R12	L14											
			VCC					R23	R10	L12											
			VCC					R21	P9	L10											
			VCC					R19	P19	R8											
			VCC					R17	P17	K17											
			VCC					R15	P13	K15											
			VCC					R13	P11	K13											
			VCC					P24	N20	K11											
			VCC					P22	N18	J8											
			VCC					P20	N16	J18											
			VCC					P18	N14	J16											
			VCC					P16	N12	J14											
			VCC					P14	N10	J12											
			VCC					P12	N8	J10											
			VCC					N25	M20	H15											
			VCC					N21	M19	J8											
			VCC					N17	M17	J8											
			VCC					N15	M15	J8											
			VCC					N13	M13	J8											
			VCC					N23	M11	J8											
			VCC					AB24	L18	J8											
			VCC					AB22	L16	J8											
			VCC					AB20	L14	J8											
			VCC					AB18	L12	J8											
			VCC					AB16	L10	J8											
			VCC					AB14	K17	J8											
			VCC					AB12	J8	J8											
			VCC					AA23	J8	J8											
			VCC					AA21	J8	J8											
			VCC					AA19	J8	J8											
			VCC					AA17	J8	J8											
			VCC					AA15	J8	J8											
			VCC					AA13	J8	J8											
			DN0					C26	H23	G18											
			DN1					V17	R15	N12											
			DN1L					G4	D6	J8											
			VCCBAT					L27	J24	F18											
			VCCA_PLL_1					M26	G20	F17											
			VCCA_PLL_2					V19	H9	E6											
			VCCA_PLL_3					AF10	Y8	Y6											
			VCCA_PLL_4					AG29	AB20	W17											
			VCCA_PLL_5					V9	PE	LE											
			VCCA_PLL_6					M99	R17	P6											
			VCCD_PLL_1					G28	H21	F13											
			VCCD_PLL_2					K9	G8	P5											
			VCCD_PLL_3					AE9	AA7	W5											
			VCCD_PLL_4					AF26	AG21	V18											
			VCCD_PLL_5					UB	P7	M5											
			VCCD_PLL_6					W8	PH	N6											
			VCCIOA					AM20	AD16	AC16											
			VCCIOA					AK24	AD19	AA17											
			VCCIOA					AD20	AD16	J8											
			VCCIOA					AD22	J8	J8											
			VCCIOA					AD25	AC20	V18											
			VCCIOA					AM14	AG17	V16											
			VCCIOA					AM11	AG13	AC7											
			VCCIOA					AL17	AD10	AC10											
			VCCIOA					AL17	AD13	J8											
			VCCIOA					AL14	AD10	J8											
			VCCIOA					AM11	J8	J8											
			VCCIOA					AG3	Y2	V2											
			VCCIOA					AD3	U2	R2											
			VCCIOA					AM6	R2	AA2											
			VCCIOA					AA3	AE2	J8											
			VCCIOA					V6	K2	M2											
			VCCIOA					V3	D2	E2											
			VCCIOA					P3	D2	F2											
			VCCIOA					J3	J8	J8											
			VCCIO7A					F14	B7	C8											
			VCCIO7A					F11	BA	C5											
			VCCIO7A					U4	B13	J8											
			VCCIO7A					C11	B10	J8											
			VCCIO7B					B8	J8	J8											
			VCCIO8A					T22	F18	D16											
			VCCIO8A					F20	E16	C17											
			VCCIO8A					G23	G16	C14											
			VCCIO8A					C20	B18	J8											
			VCCIO8A					C17	J8	J8											
			VCCIO8B					C26	G23	E18											
			VCCIO8A					AC20	AB18	U15											
			VCCIO8A					AC19	AA18	J8											
			VCCIO8A					AC24	Y11	V17											
			VCCIO8A					AD16	AA13	U10											
			VCCIO8A					AC18	AA12	J8											
			VCCIO8A					AC13	J8	J8											
			VCCIO8A					V12	UB	T8											
			VCCIO8A					AA12	UP7	T7											
			VCCIO8A					V12	UB	R7											
			VCCIO8A					R12	M7	M6											
			VCCIO8A					M15	L13	H13											
			VCCIO8A					M14	H13	J8											
			VCCIO8A					L12	H16	H13											
			VCCIO8A					M19	H16	H13											
			VCCIO8A					L19	G16	J8											
			VCCIO8A					M14	G16	J8											







Bank number	IO Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated TX/Rx Channel with DOCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no DOCT Rd (Note 2)	F1152	F780	F572	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note 3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)	DQS for X4 for F572	DQS for X8/X9 for F572 (Note 3)	DQS for X16/X18 for F572 (Note 3)
			VCCH_GXB					Ab28	M22												
			VCCH_GXB					A2z7	L22												

- Notes:
- (1) An IO module is a group of 16 I/O pins.
  - (2) When not used as DIFFIN or DIFFIO\_TX, all pins marked with \* (DIFFIN\_#pin) can be configured as emulated LVDS output channels (DIFFOUT). Only DIFFIN pins of the same index group (e.g. DIFFIN\_B1p and DIFFIN\_B1n) can be used to form an emulated LVDS output channel.
  - (3) When not used as clocks, the C0n and DQ0n pins can be used as DQ pins.



Pin Name	Pin Type (1st and 2nd Function)	Pin Description
<b>Clock and PLL Pins</b>		
CLK[4:15]	Clock, Input	Single ended clock input pin.
DIFFCLK[0:5]p	Clock, Input	Clock input pin for differential clock input. OCT Rd is not supported.
DIFFCLK[0:5]n	Clock, Input	Negative clock input for differential clock input. OCT Rd is not supported
PLL_[1:4]_CLKOUT1p	I/O, Clock	PLL[1:4]_CLKOUT1 (except PLL1 and PLL3 in EP2AGX125 and EP2AGX260) supports 2 clock I/O pins, configured either as one single ended I/O or one differential I/O pair. PLL1 and PLL3 in EP2AGX125 and EP2AGX260 support 6 clock I/O pins, configured either as 3 single ended I/Os or 3 differential I/O pairs.
PLL_[1:4]_CLKOUT1n	I/O, Clock	
PLL_[1:3]_CLKOUT[2:3]p (Note 4)	I/O, Clock	PLL1 and PLL3 in EP2AGX125 and EP2AGX260 support 6 clock I/O pins, configured either as 3 single ended I/Os or 3 differential I/O pairs.
PLL_[1:3]_CLKOUT[2:3]n (Note 4)	I/O, Clock	
<b>Dedicated Configuration/JTAG Pins</b>		
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (nCSO, ASDO, DATA[7:0], CLKUSR, INIT_DONE, DEV_OE, DEV_CLRn) are on or off before and during configuration. A logic high (1.5V, 1.8V, 2.5V, 3.0V or 3.3V) turns off the weak pull-up, while a logic low turns them on.
MSEL[0:3]	Input	Configuration input pins that set the FPGA device configuration scheme.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user-mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration done pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin.
nCEO	I/O, Output (open-drain)	Output that drives low when device configuration is complete. This pin can be used as a regular I/O if not used for device configuration.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as a user I/O pin.
TCK	Input	Dedicated JTAG test clock input pin.
TMS	Input	Dedicated JTAG test mode select input pin.
TDI	Input	Dedicated JTAG test data input pin.
TDO	Output	Dedicated JTAG test data output pin.
<b>Optional/Dual-Purpose Configuration Pins</b>		
nCSO	Output	Dedicated output control signal from the FPGA to the serial configuration device in AS mode that enables the configuration device.
ASDO	Output	Control signal from the FPGA to the serial configuration device in AS mode used to read out configuration data.
DCLK	I/O (PS, FPP) Output (AS)	Dedicated configuration clock pin. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into the FPGA. In AS mode, DCLK is an output from the FPGA that provides timing for the configuration interface.
CRC_ERROR	I/O, Output (open-drain)	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled. This pin can be used as regular I/O if not used for CRC error detection.
DEV_CLRn	I/O, Input	Optional pin that allows designers to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed.
DEV_OE	I/O, Input	Optional pin that allows designers to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
DATA0	Input	DATA[0] is a dedicated pin that is used for both the passive and active configuration modes
DATA[1:7]	I/O, Input	Dual-purpose configuration input data pins. The DATA[0:7] pins can be used for byte-wide configuration. DATA[1:7] pins can also be used as user I/O pins after configuration, but not DATA0.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin.
<b>Differential I/O Pins</b>		
DIFFIO_RX_[T,B,R][##]p, DIFFIO_RX_[T,B,R][##]n	I/O, RX channel	These are true LVDS receiver channels with OCT Rd support. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX_[T,B,R][##]p, DIFFIO_TX_[T,B,R][##]n	I/O, TX channel	These are true LVDS transmitter channels. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used as true LVDS transmitter channels, these pins can be configured as true LVDS receiver channels without OCT Rd support (DIFFIN_[T,B,R][##][p,n]). If not used for differential signaling, these pins are available as user I/O pins.
DIFFIN_[T,B,R][##]p, DIFFIN_[T,B,R][##]n	I/O, RX channel	These are true LVDS receiver channels without OCT Rd support. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used as true LVDS receiver channels without OCT Rd support, these pins can be configured as true LVDS transmitter channels (DIFFIO_TX_[T,B,R][##][p,n]). If not used for differential signaling, these pins are available as user I/O pin.
DIFFOUT_[##]p, DIFFOUT_[##]n	I/O, TX channel	These are emulated LVDS output channels. On I/O banks, there are true LVDS input buffers but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, (DIFFIO_RX_[T,B,R][##][p,n], DIFFIN_[T,B,R][##][p,n]) can be configured as emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
<b>External Memory Interface Pins</b>		
DQS[##][T,B,R]	I/O, DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.
DQSn[##][T,B,R] (Note 5)	I/O, DQSn	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.
DQ[##][T,B,R]	I/O, DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
CQ[##][T,B,R]	DQS	Optional data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.
CQn[##][T,B,R] (Note 5)	DQS	Optional complementary data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.



Pin Name	Pin Type (1st and 2nd Function)	Pin Description
<b>Reference Pins</b>		
RUP[0:2]	I/O, Input	Reference pins for I/O banks. The RUP pins share the same VCCIO with the I/O bank where they are located. The external precision resistor RUP must be connected to the designated RUP pin within the bank. If not required, this pin is a regular I/O pin.
RDN[0:2]	I/O, Input	Reference pins for I/O banks. The RDN pins share the same GND with the I/O bank where they are located. The external precision resistor RDN must be connected to the designated RDN pin within the bank. If not required, this pin is a regular I/O pin.
DNU	Do Not Use	Do Not Use (DNU).
NC	No Connect	Do not drive signals into these pins.
<b>Supply Pins</b>		
VCC	Power	VCC supplies power to the core and periphery.
VCCD_PLL [1:6]	Power	Digital power for PLL[1:6]. All of these pins must be connected even if the PLL is not used
VCCCB	Power	Configuration RAM bits power supply.
VCCA_PLL [1:6]	Power	Analog power for PLL [1:6]. All of these pins must be connected even if the PLL is not used
VCCIO[3:8][A,B]	Power	These are I/O supply voltage pins for banks 3 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all LVDS, LVCMOS(1.2V, 1.5V, 1.8V, 2.5V, 3.0V, 3.3V), HSTL(12,15,18), SSTL(15,18,2), 3.0V PCI/PCI-X I/O as well as LVTTTL (1.8V, 2.5V, 3.0V, 3.3V) I/O standards. VCCIO also supplies power to the input buffers used for LVCMOS(1.2V, 1.5V, 1.8V, 2.5V, 3.0V, 3.3V), 3.0V PCI/PCI-X and LVTTTL (1.8V, 2.5V, 3.0V, 3.3V) I/O standards.
VCCIO[3,8]C	Power	These are configuration and JTAG supply voltage pins for banks 3C and 8C. Each bank can support a different voltage level. For AS/PP/FPP configuration schemes, VCCIO8C supports 1.8V, 2.5V, 3.0V or 3.3V. JTAG can support 1.5V, 1.8V, 2.5V, 3.0V or 3.3V.
VCCPD[3:8][A,B], VCCPD[3,8]C	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers and the input buffers for HSTL/SSTL input buffers. This can be connected to 3.3V, 3.0V or 2.5V. For 3.3V I/O standard connect VCCPD to 3.3V, for 3.0V I/O standard connect VCCPD to 3.0V and for 2.5V/1.8V/1.2V I/O standards connect VCCPD to 2.5V.
VCCBAT	Power	Battery back-up power supply for design security volatile key register.
GND	Ground	Device ground pins.
VREF[3:8][A,B]N0	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. These pins cannot be used as regular I/Os.
<b>Transceiver Pins</b>		
VCCL_GXB	Power	Supplies power to the transceiver PMA TX, PMA RX and clocking.
VCCH_GXB	Power	Supplies power to the transceiver PMA output (TX) buffer.
VCCA	Power	Supplies power to the transceiver PMA regulator.
GXB_RX[0:15]p (Note 6)	Input	High speed positive differential receiver channels.
GXB_RX[0:15]n (Note 6)	Input	High speed negative differential receiver channels.
GXB_TX[0:15]p (Note 6)	Output	High speed positive differential transmitter channels.
GXB_TX[0:15]n (Note 6)	Output	High speed negative differential transmitter channels.
REFCLK[0:7]p	Input	High speed differential reference clock positive.
REFCLK[0:7]n	Input	High speed differential reference clock complement.
RREF[0:1]	Input	Reference resistor for transceiver.

**Notes:**

1. Refer to the Arria II GX Device Datasheet and Pin Connection Guidelines for the recommended operating conditions.
2. This pin definition is prepared based on the EP2AGX260.
3. Some of the pull-up /pull down resistors mentioned in the table above may not be required, depending on the exact device configuration scheme.  
The ability to NC or short them may be valuable during the debug phase, should you be required to use a different configuration scheme.  
Refer to the Configuring Arria II GX Devices chapter in the Arria II GX Device Handbook for more information.
4. PLL[1..3]\_CLKOUT[2..3][p..n] are only available in PLL1 and PLL3 in EP2AGX125 and EP2AGX260.
5. When not used as clocks, the CQn and DQSn pins can be used as DQ pin.
6. Transceiver signals GXB\_RX[15..0] and GXB\_TX[15..0] are device specific.

PLL_1	8C	8A	7A	7B	PLL_2	
		VREFB8AN0	VREFB7AN0	VREFB7BN0		
Transceiver Block (QL2)					6A	VREFB6AN0
Transceiver Block (QL1)						
Transceiver Block (QL0)					5A	VREFB5AN0
PLL_4	3C	3A	4A	4B		
		VREFB3AN0	VREFB4CN0	VREFB4BN0		

This is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only.



**Pin Information for the Arria® II GX EP2AGX125 Device**  
**Version 1.1**

<b>Version Number</b>	<b>Date</b>	<b>Changes Made</b>
1.0	2/27/2009	Initial release.
1.1	5/29/2009	Added DNU in Pin List and Pin Definitions.