



Bank number	IO Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note 3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)
Q1.3			GXB TX1m					A31									
Q1.3			GXB TX15p					B31									
Q1.3			GXB RX15n					C31									
Q1.3			GXB TX15p					D31									
Q1.3			GXB TX14n					E31									
Q1.3			GXB TX14p					F31									
Q1.3			GXB RX14n					G31									
Q1.3			GXB RX14p					H31									
Q1.3			REFCLK7n					I31									
Q1.3			REFCLK7p					L31									
Q1.3			REFCLK2n					M31									
Q1.3			REFCLK3p					N31									
Q1.3			GXB TX13n					O31									
Q1.3			GXB TX13p					P31									
Q1.3			GXB RX13n					Q31									
Q1.3			GXB RX13p					R31									
Q1.3			GXB TX12n					S31									
Q1.3			GXB TX12p					T31									
Q1.3			GXB RX12n					U31									
Q1.3			GXB RX12p					V31									
Q1.2			GXB TX11n					W31									
Q1.2			GXB TX11p					X31									
Q1.2			GXB RX11n					Y31									
Q1.2			GXB RX11p					Z31									
Q1.2			GXB TX10n					AA31									
Q1.2			GXB TX10p					AB31									
Q1.2			GXB RX10n					AC31									
Q1.2			GXB RX10p					AD31									
Q1.2			REFCLK6n					AE31									
Q1.2			REFCLK6p					AF31									
Q1.2			REFCLK2n					AG31									
Q1.2			REFCLK2p					AH31									
Q1.2			GXB TX9n					AI31									
Q1.2			GXB TX9p					AJ31									
Q1.2			GXB RX9n					AK31									
Q1.2			GXB RX9p					AL31									
Q1.2			GXB TX8n					AM31									
Q1.2			GXB TX8p					AN31									
Q1.2			GXB RX8n					AO31									
Q1.2			GXB RX8p					AP31									
Q1.2			GXB TX7n					AQ31									
Q1.1			GXB TX7p					AR31									
Q1.1			GXB RX7n					AS31									
Q1.1			GXB RX7p					AT31									
Q1.1			GXB TX6n					AV31									
Q1.1			GXB TX6p					AW31									
Q1.1			GXB RX6n					AX31									
Q1.1			GXB RX6p					AY31									
Q1.1			REFCLK5n					AZ31									
Q1.1			REFCLK5p					BA31									
Q1.1			REFCLK1n					BB31									
Q1.1			REFCLK1p					BC31									
Q1.1			GXB TX5n					BD31									
Q1.1			GXB TX5p					BE31									
Q1.1			GXB RX5n					BF31									
Q1.1			GXB RX5p					BG31									
Q1.1			GXB TX4n					BH31									
Q1.1			GXB TX4p					BI31									
Q1.1			GXB RX4n					BJ31									
Q1.1			GXB RX4p					BK31									
Q1.0			GXB TX3n					BL31									
Q1.0			GXB TX3p					BM31									
Q1.0			GXB RX3n					BN31									
Q1.0			GXB RX3p					BO31									
Q1.0			GXB TX2n					BP31									
Q1.0			GXB TX2p					BQ31									
Q1.0			GXB RX2n					BR31									
Q1.0			GXB RX2p					BS31									
Q1.0			REFCLK4n					BT31									
Q1.0			REFCLK4p					BV31									
Q1.0			REFCLK0n					BW31									
Q1.0			REFCLK0p					BX31									
Q1.0			GXB TX1n					BY31									
Q1.0			GXB TX1p					BZ31									
Q1.0			GXB RX1n					CA31									
Q1.0			GXB RX1p					CB31									
Q1.0			GXB TX0n					CC31									
Q1.0			GXB TX0p					CD31									
Q1.0			GXB RX0n					CE31									
Q1.0			GXB RX0p					CF31									
3C			iCONFIG		iCONFIG			CG31									
3C			CONF_DONE		CONF_DONE			CH31									
3C			MSEL1		MSEL1			CI31									
3C			MSEL2		MSEL2			CJ31									
3C			MSEL3		MSEL3			CK31									
3C			MSEL4		MSEL4			CL31									
3C			MSEL5		MSEL5			CM31									
3C			MSEL6		MSEL6			CN31									
3C			iSTATUS		iSTATUS			CO31									
3C			IND_PULLUP		IND_PULLUP			CP31									
3C			iCE		iCE			CQ31									
3B	BI01	VREFB3BND	IO			DIFFIO_TX_B1n	DIFFIN_B1n*	AH26		DQ24B		DQ12B				DQ6B	
3B	BI01	VREFB3BND	IO			DIFFIO_RX_B1n	DIFFOUT_B1n	AG24		DQ24B		DQ12B				DQ6B	
3B	BI01	VREFB3BND	IO			DIFFIO_TX_B1p	DIFFIN_B1p*	AG27		DQ24B		DQ12B				DQ6B	
3B	BI01	VREFB3BND	IO			DIFFIO_RX_B1p	DIFFOUT_B1p	AF25									
3B	BI01	VREFB3BND	IO			DIFFIO_TX_B2n	DIFFIN_B2n*	AD22		DQS24B		DQ12B				DQ6B	
3B	BI01	VREFB3BND	IO			DIFFIO_RX_B2n	DIFFOUT_B2n	AF27									
3B	BI01	VREFB3BND	IO			DIFFIO_TX_B2p	DIFFIN_B2p*	AC22		DQS24B		DQ12B/CCQ12B				DQ6B	
3B	BI01	VREFB3BND	IO			DIFFIO_RX_B2p	DIFFOUT_B2p	AE28									
3B	BI01	VREFB3BND	IO			DIFFIO_TX_B3n	DIFFIN_B3n*	AK29		DQS23B		DQS12B/DQ12B				DQ6B	
3B	BI01	VREFB3BND	IO			DIFFIO_RX_B3n	DIFFOUT_B3n	AE27		DQ23B		DQ12B				DQ6B	
3B	BI01	VREFB3BND	IO			DIFFIO_TX_B3p	DIFFIN_B3p*	AH28		DQS23B		DQS12B/CCQ12B				DQ6B	
3B	BI01	VREFB3BND	IO			DIFFIO_RX_B3p	DIFFOUT_B3p	AE28									
3B	BI01	VREFB3BND	IO			DIFFIO_TX_B4n	DIFFIN_B4n*	AF24		DQ23B		DQ12B				DQ6B	
3B	BI01	VREFB3BND	IO			DIFFIO_RX_B4n	DIFFOUT_B4n	AG28		DQ23B		DQ12B				DQ6B	
3B	BI01	VREFB3BND	IO			DIFFIO_TX_B4p	DIFFIN_B4p*	AE24									
3B	BI01	VREFB3BND	IO			DIFFIO_RX_B4p	DIFFOUT_B4p	AF28		DQ23B		DQ12B				DQ6B	
3B	BI02	VREFB3BND	IO			DIFFIO_TX_B5n	DIFFIN_B5n*	AJ29		DQ22B		DQ11B				DQ6B	



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3B	BIO2	VREFB3N0	IO			DIFFIO_RX_B6n	DIFFN_B6n	AJ27	AC28	DO22B	DO11B	DO22B	DO11B				
3B	BIO2	VREFB3N0	IO			DIFFIO_TX_B6p	DIFFN_B6p	AJ28	AC29	DO22B	DO11B	DO22B	DO11B				
3B	BIO2	VREFB3N0	IO			DIFFIO_RX_B6p	DIFFN_B6p	AH27	AF23	DOSn22B	DO11B	DO22B	DO11B	DO6B			
3B	BIO2	VREFB3N0	IO			DIFFIO_TX_B6n	DIFFN_B6n	AL28	AL28	DO22B	DO11B	DO22B	DO11B	DO6B			
3B	BIO2	VREFB3N0	IO			DIFFIO_RX_B6p	DIFFN_B6p	AE23	AE23	DOS22B	DO11B/CQn11B	DO22B	DO11B/CQn11B	DO6B/CQn6B			
3B	BIO2	VREFB3N0	IO			DIFFIO_TX_B6n	DIFFN_B6n	AK28	AK28	DOSn21B	DOSn11B/DO11B	DO21B	DO11B	DO6B			
3B	BIO2	VREFB3N0	IO			DIFFIO_RX_B7n	DIFFN_B7n	AK27	AK27	DO21B	DO11B	DO21B	DO11B	DO6B			
3B	BIO2	VREFB3N0	IO			DIFFIO_TX_B7p	DIFFN_B7p	AJ30	AJ30	DOS21B	DOSn11B/CQ11B	DO21B	DO11B	DO6B/CQ6B			
3B	BIO2	VREFB3N0	IO			DIFFIO_RX_B7n	DIFFN_B7n	AJ29	AJ29	DO21B	DO11B	DO21B	DO11B	DO6B			
3B	BIO2	VREFB3N0	IO			DIFFIO_TX_B8n	DIFFN_B8n	AE21	AE21	DO21B	DO11B	DO21B	DO11B	DO6B			
3B	BIO2	VREFB3N0	IO			DIFFIO_RX_B8n	DIFFN_B8n	AF30	AF30	DO21B	DO11B	DO21B	DO11B	DO6B			
3B	BIO2	VREFB3N0	IO			DIFFIO_TX_B8p	DIFFN_B8p	AD21	AD21	DO21B	DO11B	DO21B	DO11B	DO6B			
3B	BIO2	VREFB3N0	IO			DIFFIO_RX_B8p	DIFFN_B8p	AG30	AG30	DO21B	DO11B	DO21B	DO11B	DO6B			
3A		VREFB3A0	IO	PLL4_CLKOUT1n				AH25	U24								
3A		VREFB3A0	IO	PLL4_CLKOUT1p				AL27	AE19								
3A		VREFB3A0	IO	RUP0				AH24	V24								
3A		VREFB3A0	IO					AL28	AC19								
3A	BIO3	VREFB3A0	IO			DIFFIO_TX_B9n	DIFFN_B9n	AK29	AK29	DO20B	DO10B	DO20B	DO10B	DO2B			
3A	BIO3	VREFB3A0	IO			DIFFIO_RX_B9n	DIFFN_B9n	AM28	AM28	DO20B	DO10B	DO20B	DO10B	DO2B			
3A	BIO3	VREFB3A0	IO			DIFFIO_TX_B9p	DIFFN_B9p	AL29	AL29	DO20B	DO10B	DO20B	DO10B	DO2B			
3A	BIO3	VREFB3A0	IO			DIFFIO_RX_B9p	DIFFN_B9p	AK27	AK27	DO20B	DO10B	DO20B	DO10B	DO2B			
3A	BIO3	VREFB3A0	IO			DIFFIO_TX_B10n	DIFFN_B10n	AJ25	AJ25	DOSn20B	DO10B	DO20B	DO10B	DO2B			
3A	BIO3	VREFB3A0	IO			DIFFIO_RX_B10n	DIFFN_B10n	AN28	AN28	DO20B	DO10B	DO20B	DO10B	DO2B			
3A	BIO3	VREFB3A0	IO			DIFFIO_TX_B10p	DIFFN_B10p	AJ24	AJ24	DOS20B	DO10B/CQn10B	DO20B	DO10B	DO2B			
3A	BIO3	VREFB3A0	IO			DIFFIO_RX_B10p	DIFFN_B10p	AN27	AN27	DO20B	DO10B	DO20B	DO10B	DO2B			
3A	BIO3	VREFB3A0	IO			DIFFIO_TX_B11n	DIFFN_B11n	AM26	AM26	DOSn19B	DOSn10B/DO10B	DO19B	DO10B	DO2B			
3A	BIO3	VREFB3A0	IO			DIFFIO_RX_B11n	DIFFN_B11n	AK21	AK21	DO19B	DO10B	DO19B	DO10B	DO2B			
3A	BIO3	VREFB3A0	IO			DIFFIO_TX_B11p	DIFFN_B11p	AM25	AM25	DOS19B	DOS10B/DO10B	DO19B	DO10B	DO2B			
3A	BIO3	VREFB3A0	IO			DIFFIO_RX_B11p	DIFFN_B11p	AJ22	AJ22	DO19B	DO10B	DO19B	DO10B	DO2B			
3A	BIO3	VREFB3A0	IO			DIFFIO_TX_B12n	DIFFN_B12n	AD21	AD21	DO19B	DO10B	DO19B	DO10B	DO2B			
3A	BIO3	VREFB3A0	IO			DIFFIO_RX_B12n	DIFFN_B12n	AF29	AF29	DO19B	DO10B	DO19B	DO10B	DO2B			
3A	BIO3	VREFB3A0	IO			DIFFIO_TX_B12p	DIFFN_B12p	AF20	AF20	DO19B	DO10B	DO19B	DO10B	DO2B			
3A	BIO4	VREFB3A0	IO			DIFFIO_RX_B13n	DIFFN_B13n	AM24	AD21	DO18B	DO9B	DO18B	DO9B	DO2B		DO14B	DO7B
3A	BIO4	VREFB3A0	IO			DIFFIO_TX_B13n	DIFFN_B13n	AM23	AC17	DO18B	DO9B	DO18B	DO9B	DO2B		DO14B	DO7B
3A	BIO4	VREFB3A0	IO			DIFFIO_RX_B13p	DIFFN_B13p	AL24	AC21	DO18B	DO9B	DO18B	DO9B	DO2B		DO14B	DO7B
3A	BIO4	VREFB3A0	IO	INIT_DONE		DIFFIO_TX_B13p	DIFFN_B13p	AL23	AB17	DO18B	DO9B	DO18B	DO9B	DO2B		DO14B	DO7B
3A	BIO4	VREFB3A0	IO			DIFFIO_RX_B14n	DIFFN_B14n	AH21	Y22	DOSn18B	DO9B	DO18B	DO9B	DO2B		DOSn14B	DO7B
3A	BIO4	VREFB3A0	IO			DIFFIO_TX_B14n	DIFFN_B14n	AP27	AC16	DO18B	DO9B	DO18B	DO9B	DO2B		DO14B	DO7B
3A	BIO4	VREFB3A0	IO			DIFFIO_RX_B14p	DIFFN_B14p	AG22	AG22	DOS18B	DOSn18B/CQn18B	DO18B	DO9B	DO2B		DOS14B	DO7B/CQn7B
3A	BIO4	VREFB3A0	IO			DIFFIO_TX_B14p	DIFFN_B14p	AP26	AB16	DO18B	DO9B	DO18B	DO9B	DO2B		DO14B	DO7B
3A	BIO4	VREFB3A0	IO			DIFFIO_RX_B15n	DIFFN_B15n	AP24	AD23	DOSn17B	DOSn18B/CQn18B	DO17B	DO9B	DO2B		DOSn13B	DOSn7B/CQn7B
3A	BIO4	VREFB3A0	IO			DIFFIO_TX_B15n	DIFFN_B15n	AP25	AD24	DO17B	DO9B	DO17B	DO9B	DO2B		DO13B	DO7B
3A	BIO4	VREFB3A0	IO			DIFFIO_RX_B15p	DIFFN_B15p	AN24	AD22	DOS17B	DOS18B/CQn18B	DO17B	DO9B	DO2B		DOS13B	DOS7B/CQn7B
3A	BIO4	VREFB3A0	IO			DIFFIO_TX_B15p	DIFFN_B15p	AN25	AC18	DO17B	DO9B	DO17B	DO9B	DO2B		DO13B	DO7B
3A	BIO4	VREFB3A0	IO			DIFFIO_RX_B16n	DIFFN_B16n	AE19	Y23	DO17B	DO9B	DO17B	DO9B	DO2B		DO13B	DO7B
3A	BIO4	VREFB3A0	IO			DIFFIO_TX_B16n	DIFFN_B16n	AJ23	AC23	DO17B	DO9B	DO17B	DO9B	DO2B		DO13B	DO7B
3A	BIO4	VREFB3A0	IO			DIFFIO_RX_B16p	DIFFN_B16p	AD19	Y19	DO17B	DO9B	DO17B	DO9B	DO2B		DO13B	DO7B
3A	BIO4	VREFB3A0	IO			DIFFIO_TX_B16p	DIFFN_B16p	AK23	AC23	DO17B	DO9B	DO17B	DO9B	DO2B		DO13B	DO7B
3A	BIO5	VREFB3A0	IO			DIFFIO_RX_B17n	DIFFN_B17n	AL25	AD24	DO16B	DO8B	DO16B	DO8B	DO2B		DO12B	DO6B
3A	BIO5	VREFB3A0	IO			DIFFIO_TX_B17n	DIFFN_B17n	AL25	AD24	DO16B	DO8B	DO16B	DO8B	DO2B		DO12B	DO6B
3A	BIO5	VREFB3A0	IO			DIFFIO_RX_B17p	DIFFN_B17p	AM22	AE22	DO16B	DO8B	DO16B	DO8B	DO2B		DO12B	DO6B
3A	BIO5	VREFB3A0	IO			DIFFIO_TX_B17p	DIFFN_B17p	AK25	AG24	DO16B	DO8B	DO16B	DO8B	DO2B		DO12B	DO6B
3A	BIO5	VREFB3A0	IO			DIFFIO_RX_B17p	DIFFN_B17p	AL22	AE21	DO16B	DO8B	DO16B	DO8B	DO2B		DO12B	DO6B
3A	BIO5	VREFB3A0	IO			DIFFIO_TX_B18n	DIFFN_B18n	AJ21	V23	DOSn16B	DO8B	DO16B	DO8B	DO2B		DOSn12B	DO6B
3A	BIO5	VREFB3A0	IO			DIFFIO_RX_B18n	DIFFN_B18n	AJ21	AF20	DO16B	DO8B	DO16B	DO8B	DO2B		DO12B	DO6B
3A	BIO5	VREFB3A0	IO			DIFFIO_TX_B18p	DIFFN_B18p	AH20	V22	DOS16B	DOSn16B/CQn16B	DO16B	DO8B	DO2B		DOS12B	DO6B/CQn6B
3A	BIO5	VREFB3A0	IO			DIFFIO_RX_B18p	DIFFN_B18p	AK21	AE20	DO16B	DO8B	DO16B	DO8B	DO2B		DO12B	DO6B
3A	BIO5	VREFB3A0	IO			DIFFIO_TX_B19n	DIFFN_B19n	AP22	AF18	DOSn15B	DOSn16B/CQn16B	DO15B	DO8B	DO2B		DOSn11B	DOSn16B/CQn16B
3A	BIO5	VREFB3A0	IO			DIFFIO_RX_B19n	DIFFN_B19n	AP23	AF19	DO15B	DO8B	DO15B	DO8B	DO2B		DO11B	DO6B
3A	BIO5	VREFB3A0	IO			DIFFIO_TX_B19p	DIFFN_B19p	AP21	AE18	DOS15B	DOS16B/CQn16B	DO15B	DO8B	DO2B		DOS11B	DOS16B/CQn16B
3A	BIO5	VREFB3A0	IO			DIFFIO_RX_B19p	DIFFN_B19p	AN22	AE19	DO15B	DO8B	DO15B	DO8B	DO2B		DO11B	DO6B
3A	BIO5	VREFB3A0	IO			DIFFIO_TX_B20n	DIFFN_B20n	AG19	AA16	DO15B	DO8B	DO15B	DO8B	DO2B		DO11B	DO6B
3A	BIO5	VREFB3A0	IO			DIFFIO_RX_B20n	DIFFN_B20n	AL20	AF17	DO15B	DO8B	DO15B	DO8B	DO2B		DO11B	DO6B
3A	BIO5	VREFB3A0	IO			DIFFIO_TX_B20p	DIFFN_B20p	AF19	Y16	DO15B	DO8B	DO15B	DO8B	DO2B		DO11B	DO6B
3A	BIO5	VREFB3A0	IO			DIFFIO_RX_B20p	DIFFN_B20p	AL19	AE17	DO15B	DO8B	DO15B	DO8B	DO2B		DO11B	DO6B
3A	BIO6	VREFB3A0	IO			DIFFIO_TX_B21n	DIFFN_B21n	AN21	AD45	DO14B	DO7B	DO14B	DO7B	DO2B		DO10B	DO5B
3A	BIO6	VREFB3A0	IO			DIFFIO_RX_B21n	DIFFN_B21n	AP20	AF16	DO14B	DO7B	DO14B	DO7B	DO2B		DO10B	DO5B
3A	BIO6	VREFB3A0	IO			DIFFIO_TX_B21p	DIFFN_B21p	AK21	AC15	DO14B	DO7B	DO14B	DO7B	DO2B		DO10B	DO5B
3A	BIO6	VREFB3A0	IO			DIFFIO_RX_B21p	DIFFN_B21p	AF19	AE16	DO14B	DO7B	DO14B	DO7B	DO2B		DO10B	DO5B
3A	BIO6	VREFB3A0	IO			DIFFIO_TX_B22n	DIFFN_B22n	AF18	AA19	DOSn14B	DO7B	DO14B	DO7B	DO2B		DOSn10B	DO5B
3A	BIO6	VREFB3A0	IO			DIFFIO_RX_B22n	DIFFN_B22n	AN19	AH19	DO14B	DO7B	DO14B	DO7B	DO2B		DO10B	DO5B
3A	BIO6	VREFB3A0	IO			DIFFIO_TX_B22p	DIFFN_B22p	AE18	Y18	DOS14B	DO7B/CQn7B	DO14B	DO7B	DO2B		DOS10B	DOS16B/CQn16B
3A	BIO6	VREFB3A0	IO			DIFFIO_RX_B22p	DIFFN_B22p	AM19	AG19	DO14B	DO7B	DO14B	DO7B	DO2B		DO10B	DO5B
3A	BIO6	VREFB3A0	IO			DIFFIO_TX_B23n	DIFFN_B23n	AM18	AH17	DOSn13B	DOSn14B/CQn14B	DO13B	DO7B	DO2B		DOSn9B	DOSn16B/CQn16B
3A	BIO6	VREFB3A0	IO			DIFFIO_RX_B23n	DIFFN_B23n	AP18	AH18	DO13B	DO7B	DO13B	DO7B	DO2B		DO9B	DO5B
3A	BIO6	VREFB3A0	IO			DIFFIO_TX_B23p	DIFFN_B23p	AL18	AH16	DOS13B	DOS14B/CQn14B	DO13B	DO7B	DO2B		DOS9B	DOS16B/CQn16B
3A	BIO6	VREFB3A0	IO			DIFFIO_RX_B23p	DIFFN_B23p	AN18	AG18	DO13B	DO7B	DO13B	DO7B	DO2B		DO9B	DO5B
3A	BIO6	VREFB3A0	IO			DIFFIO_TX_B24n	DIFFN_B24n	AH19	AB15	DO13B	DO7B	DO13B	DO7B	DO2B		DO9B	DO5B
3A	BIO6	VREFB3A0	IO			DIFFIO_RX_B24n	DIFFN_B24n	AK18	AH15	DO13B	DO7B	DO13B	DO7B	DO2B		DO9B	DO5B
3A	BIO6	VREFB3A0	IO			DIFFIO_TX_B24p	DIFFN_B24p	AG18	AA15	DO13B	DO7B	DO13B	DO7B	DO2B		DO9B	DO5B
3A	BIO6	VREFB3A0	IO			DIFFIO_RX_B24p	DIFFN_B24p	AJ19	AG15	DO13B	DO7B	DO13B	DO7B	DO2B		DO9B	DO5B
3A		VREFB3A0	IO	DIFFCLK_0n				AK19	AF15								
4A		VREFB3A0	IO	DIFFCLK_1n				AP17	AF14								
4A		VREFB3A0	IO	DIFFCLK_0p				AJ19	AE15								
4A		VREFB3A0	IO	DIFFCLK_1p				AP16	AE14								
4A	BIO7	VREFB3A0	IO														



Bank number	IO Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with no OCT Rd (Note 2)	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with F1152 F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note 3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)	
4A	BI06	VREFB4ND	IO			DIFFIO_RX_B30p	AP11	AE13								
4A	BI08	VREFB4ND	IO			DIFFIO_TX_B30n	AH16	AC13	DQSn10B	DQ5B	DQ3B	DQ1B	DQ5n4B	DQ3B	DQ2B	
4A	BI08	VREFB4ND	IO			DIFFIO_RX_B30n	AN12	AF12	DQ10B	DQ5B	DQ3B	DQ1B	DQ5B	DQ3B	DQ2B	
4A	BI08	VREFB4ND	IO			DIFFIO_TX_B30p	AK16	AE13	DQSn10B	DQ5B	DQ3B	DQ1B	DQ5n4B	DQ3B	DQ2B	
4A	BI08	VREFB4ND	IO			DIFFIO_RX_B30p	AM12	AE12								
4A	BI08	VREFB4ND	IO			DIFFIO_TX_B31n	DIFFN_B31n*	AL15	AF10	DQSn9B	DQ5n5B/DQ5B	DQ3B	DQ3n1B/DQ1B	DQ5n5B	DQ3n1B/DQ1B	
4A	BI08	VREFB4ND	IO			DIFFIO_RX_B31n	DIFFOUT_B31n	AP10	AF11	DQ9B	DQ5B	DQ3B	DQ1B	DQ5B	DQ3B	
4A	BI08	VREFB4ND	IO			DIFFIO_TX_B31p	DIFFN_B31p*	AK15	AE10	DQSn9B	DQ5n5B/CQ5B	DQ3B	DQ3n1B/CQ1B	DQ5n5B	DQ3n1B/CQ1B	
4A	BI08	VREFB4ND	IO			DIFFIO_RX_B31p	DIFFOUT_B31p	AN10	AE11							
4A	BI08	VREFB4ND	IO			DIFFIO_TX_B32n	DIFFN_B32n*	AH15	W13	DQ9B	DQ5B	DQ3B	DQ1B	DQ5B	DQ3B	
4A	BI08	VREFB4ND	IO			DIFFIO_RX_B32n	DIFFOUT_B32n	AP9	AF9	DQ9B	DQ5B	DQ3B	DQ1B	DQ5B	DQ3B	
4A	BI08	VREFB4ND	IO			DIFFIO_TX_B32p	DIFFN_B32p*	AG15	W12							
4A	BI08	VREFB4ND	IO			DIFFIO_RX_B32p	DIFFOUT_B32p	AP9	AF9	DQ9B	DQ5B	DQ3B	DQ1B	DQ5B	DQ3B	
4A	BI09	VREFB4ND	IO			DIFFIO_TX_B33n	DIFFN_B33n*	AP7	AF8	DQ8B	DQ4B	DQ2B	DQ1B	DQ4B	DQ2B	
4A	BI09	VREFB4ND	IO			DIFFIO_RX_B33n	DIFFOUT_B33n	AL14	AF7	DQ8B	DQ4B	DQ2B	DQ1B	DQ4B	DQ2B	
4A	BI09	VREFB4ND	IO			DIFFIO_TX_B33p	DIFFN_B33p*	AN7	AE8	DQ8B	DQ4B	DQ2B	DQ1B	DQ4B	DQ2B	
4A	BI09	VREFB4ND	IO			DIFFIO_RX_B33p	DIFFOUT_B33p	AL13	AE7							
4A	BI09	VREFB4ND	IO			DIFFIO_TX_B34n	DIFFN_B34n*	AF16	Y12	DQSn8B	DQ4B	DQ2B	DQ1B	DQSn4B	DQ2B	
4A	BI09	VREFB4ND	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	AP6	AF6	DQ8B	DQ4B	DQ2B	DQ1B	DQ4B	DQ2B	
4A	BI09	VREFB4ND	IO			DIFFIO_TX_B34p	DIFFN_B34p*	AE16	W11	DQSn8B	DQ4B/CQ4B	DQ2B	DQ1B	DQSn4B	DQ2B	
4A	BI09	VREFB4ND	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	AN6	AE6							
4A	BI09	VREFB4ND	IO			DIFFIO_TX_B35n	DIFFN_B35n*	AL12	AD12	DQSn7B	DQSn4B/DQ4B	DQ2B	DQ1B	DQSn3B	DQSn1B/DQ1B	
4A	BI09	VREFB4ND	IO			DIFFIO_RX_B35n	DIFFOUT_B35n	AP5	AF5	DQ7B	DQ4B	DQ2B	DQ1B	DQ4B	DQ2B	
4A	BI09	VREFB4ND	IO			DIFFIO_TX_B35p	DIFFN_B35p*	AK13	AC12	DQSn7B	DQSn4B/CQ4B	DQ2B	DQ1B	DQSn3B	DQSn1B/CQ1B	
4A	BI09	VREFB4ND	IO			DIFFIO_RX_B35p	DIFFOUT_B35p	AP4	AE5							
4A	BI09	VREFB4ND	IO			DIFFIO_TX_B36n	DIFFN_B36n*	AC15	AC11	DQ7B	DQ4B	DQ2B	DQ1B	DQ3B	DQ2B	
4A	BI09	VREFB4ND	IO			DIFFIO_RX_B36n	DIFFOUT_B36n	AL11	AG4	DQ7B	DQ4B	DQ2B	DQ1B	DQ3B	DQ2B	
4A	BI09	VREFB4ND	IO			DIFFIO_TX_B36p	DIFFN_B36p*	AC14	AB11							
4A	BI09	VREFB4ND	IO			DIFFIO_RX_B36p	DIFFOUT_B36p	AK12	DQ7B	DQ4B	DQ2B	DQ1B	DQ3B	DQ2B	DQ1B	
4A	BI09	VREFB4ND	IO			DIFFIO_TX_B37n	DIFFN_B37n*	AP3	AH3	DQ6B	DQ3B	DQ2B	DQ1B	DQ2B	DQ1B	
4A	BI09	VREFB4ND	IO			DIFFIO_RX_B37n	DIFFOUT_B37n	AN9	AF4	DQ6B	DQ3B	DQ2B	DQ1B	DQ2B	DQ1B	
4A	BI09	VREFB4ND	IO			DIFFIO_TX_B37p	DIFFN_B37p*	AP2	AH2	DQ6B	DQ3B	DQ2B	DQ1B	DQ2B	DQ1B	
4A	BI09	VREFB4ND	IO			DIFFIO_RX_B37p	DIFFOUT_B37p	AN9	AE4							
4A	BI09	VREFB4ND	IO			DIFFIO_TX_B38n	DIFFN_B38n*	AF15	Y11	DQSn6B	DQ3B	DQ2B	DQ1B	DQSn2B	DQ1B	
4A	BI09	VREFB4ND	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	AM10	AF3	DQ6B	DQ3B	DQ2B	DQ1B	DQ2B	DQ1B	
4A	BI09	VREFB4ND	IO			DIFFIO_TX_B38p	DIFFN_B38p*	AE15	AE5	DQSn6B	DQ3B/CQ3B	DQ2B	DQ1B	DQSn2B	DQ1B	
4A	BI09	VREFB4ND	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	AL10	AF2							
4A	BI09	VREFB4ND	IO			DIFFIO_TX_B39n	DIFFN_B39n*	AM8	AD6	DQSn5B	DQSn3B/DQ3B	DQ2B	DQ1B	DQSn1B	DQSn1B/DQ1B	
4A	BI09	VREFB4ND	IO			DIFFIO_RX_B39n	DIFFOUT_B39n	AN4	AG1	DQ5B	DQ3B	DQ2B	DQ1B	DQ2B	DQ1B	
4A	BI09	VREFB4ND	IO			DIFFIO_TX_B39p	DIFFN_B39p*	AM7	AC6	DQSn5B	DQSn3B/CQ3B	DQ2B	DQ1B	DQSn1B	DQSn1B/CQ1B	
4A	BI09	VREFB4ND	IO			DIFFIO_RX_B39p	DIFFOUT_B39p	AN3	AF1							
4A	BI09	VREFB4ND	IO			DIFFIO_TX_B40n	DIFFN_B40n*	AJ16	AX10	DQ5B	DQ3B	DQ2B	DQ1B	DQ1B	DQ1B	
4A	BI09	VREFB4ND	IO			DIFFIO_RX_B40n	DIFFOUT_B40n	AJ12	AD9	DQ5B	DQ3B	DQ2B	DQ1B	DQ1B	DQ1B	
4A	BI09	VREFB4ND	IO			DIFFIO_TX_B40p	DIFFN_B40p*	AJ15	Y10							
4A	BI09	VREFB4ND	IO			DIFFIO_RX_B40p	DIFFOUT_B40p	AL11	AC9	DQ5B	DQ3B	DQ2B	DQ1B	DQ1B	DQ1B	
4A	VREFB4ND	IO	PLL3_CLKOUT1n				AJ13	AC10								
4A	VREFB4ND	IO	PLL3_CLKOUT1p			DIFFIO_RX_B41n	DIFFOUT_B41n	AH13	AD7							
4A	VREFB4ND	IO	PLL3_CLKOUT1p				AH14									
4A	VREFB4ND	IO	PLL3_CLKOUT2n			DIFFIO_RX_B41p	DIFFOUT_B41p	AG13	AC7							
4A	VREFB4ND	IO	PLL3_CLKOUT2n				AF14	AB9								
4A	VREFB4ND	IO	PLL3_CLKOUT2p				AK12	AC8								
4A	VREFB4ND	IO	PLL3_CLKOUT2p				AE14	AA9								
4A	VREFB4ND	IO	PLL3_CLKOUT3p				AG12	AB8								
4B	BI011	VREFB4ND	IO			DIFFIO_TX_B41n	DIFFN_B41n*	AK10	DQ4B	DQ2B	DQ1B					
4B	BI011	VREFB4ND	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	AL9	DQ4B	DQ2B	DQ1B					
4B	BI011	VREFB4ND	IO			DIFFIO_TX_B41p	DIFFN_B41p*	AJ10	DQ4B	DQ2B	DQ1B					
4B	BI011	VREFB4ND	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	AK9	DQ4B	DQ2B	DQ1B					
4B	BI011	VREFB4ND	IO			DIFFIO_TX_B42n	DIFFN_B42n*	AF13	DQSn4B	DQ2B	DQ1B					
4B	BI011	VREFB4ND	IO			DIFFIO_RX_B43n	DIFFOUT_B43n	AL8	DQ4B	DQ2B	DQ1B					
4B	BI011	VREFB4ND	IO			DIFFIO_TX_B42p	DIFFN_B42p*	AE13	DQSn4B	DQ2B/CQ2B	DQ1B/CQ1B					
4B	BI011	VREFB4ND	IO			DIFFIO_RX_B43p	DIFFOUT_B43p	AL7								
4B	BI011	VREFB4ND	IO			DIFFIO_TX_B43n	DIFFN_B43n*	AL6	DQSn3B	DQSn2B/DQ2B	DQSn1B/DQ1B					
4B	BI011	VREFB4ND	IO			DIFFIO_RX_B44n	DIFFOUT_B44n	AM6	DQ3B	DQ2B	DQ1B					
4B	BI011	VREFB4ND	IO			DIFFIO_TX_B43p	DIFFN_B43p*	AW6	W10	DQSn3B	DQSn2B/CQ2B	DQSn1B/CQ1B				
4B	BI011	VREFB4ND	IO			DIFFIO_RX_B44p	DIFFOUT_B44p	AM5								
4B	BI011	VREFB4ND	IO			DIFFIO_TX_B44n	DIFFN_B44n*	AF12	DQ3B	DQ2B	DQ1B					
4B	BI011	VREFB4ND	IO			DIFFIO_RX_B45n	DIFFOUT_B45n	AK7	DQ3B	DQ2B	DQ1B					
4B	BI011	VREFB4ND	IO			DIFFIO_TX_B44p	DIFFN_B44p*	AE12								
4B	BI011	VREFB4ND	IO			DIFFIO_RX_B45p	DIFFOUT_B45p	AJ7	DQ3B	DQ2B	DQ1B					
4B	BI012	VREFB4ND	IO			DIFFIO_TX_B45n	DIFFN_B45n*	AK4	DQ2B	DQ1B	DQ1B					
4B	BI012	VREFB4ND	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	AJ9	DQ2B	DQ1B	DQ1B					
4B	BI012	VREFB4ND	IO			DIFFIO_TX_B45p	DIFFN_B45p*	AL5	DQ2B	DQ1B	DQ1B					
4B	BI012	VREFB4ND	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	AH9								
4B	BI012	VREFB4ND	IO			DIFFIO_TX_B46n	DIFFN_B46n*	AE11	DQSn2B	DQ1B	DQ1B					
4B	BI012	VREFB4ND	IO			DIFFIO_RX_B47n	DIFFOUT_B47n	AH10	DQ2B	DQ1B	DQ1B					
4B	BI012	VREFB4ND	IO			DIFFIO_TX_B46p	DIFFN_B46p*	AD12	AB10							
4B	BI012	VREFB4ND	IO			DIFFIO_RX_B47p	DIFFOUT_B47p	AG9								
4B	BI012	VREFB4ND	IO			DIFFIO_TX_B47n	DIFFN_B47n*	AM2	DQSn1B	DQSn1B/DQ1B	DQ1B					
4B	BI012	VREFB4ND	IO			DIFFIO_RX_B48n	DIFFOUT_B48n	AK8	DQ1B	DQ1B	DQ1B					
4B	BI012	VREFB4ND	IO			DIFFIO_TX_B47p	DIFFN_B47p*	AL3	DQSn1B	DQSn1B/CQ1B	DQ1B					
4B	BI012	VREFB4ND	IO			DIFFIO_RX_B48p	DIFFOUT_B48p	AL4								
4B	BI012	VREFB4ND	IO			DIFFIO_TX_B48n	DIFFN_B48n*	AD10	DQ1B	DQ1B	DQ1B					
4B	BI012	VREFB4ND	IO			DIFFIO_RX_B49n	DIFFOUT_B49n	AN1	DQ1B	DQ1B	DQ1B					
4B	BI012	VREFB4ND	IO			DIFFIO_TX_B48p	DIFFN_B48p*	AF11								
5B	RI01	VREFB5ND	IO			DIFFIO_TX_R51n	DIFFN_R51n*	AM1	DQ1B	DQ1B	DQ1B					
5B	RI01	VREFB5ND	IO			DIFFIO_RX_R11n	DIFFOUT_R11n	AJ8	DQ24R	DQ12R	DQ6R					
5B	RI01	VREFB5ND	IO			DIFFIO_TX_R11p	DIFFN_R11p*	AF7	DQ24R	DQ12R	DQ6R					
5B	RI01	VREFB5ND	IO			DIFFIO_RX_R12n	DIFFOUT_R12n	AF8								
5B	RI01	VREFB5ND	IO			DIFFIO_TX_R2n	DIFFN_R2n*	AD9	DQSn24R	DQ12R	DQ6R					
5B	RI01	VREFB5ND	IO			DIFFIO_RX_R2n	DIFFOUT_R2n	AK3	DQ24R	DQ12R	DQ6R					
5B	RI01	VREFB5ND	IO			DIFFIO_TX_R2p	DIFFN_R2p*	AD10	DQSn24R	DQ12R/CQ12R	DQ6R					
5B	RI01	VREFB5ND	IO			DIFFIO_RX_R2p	DIFFOUT_R2p	AK4								
5B	RI01	VREFB5ND	IO			DIFFIO_TX_R3n	DIFFN_R3n*	AH5	DQSn23R	DQSn12R/DQ12R	DQ6R					
5B	RI01	VREFB5ND	IO			DIFFIO_RX_R3n	DIFFOUT_R3n	AG6								
5B	RI01	VREFB5ND	IO			DIFFIO_TX_R3p	DIFFN_R3p*	AH7	DQSn23R	DQSn12R/CQ12R	DQ6R					
5B	RI01	VREFB5ND	IO			DIFFIO_RX_R3p	DIFFOUT_R3p	AG6								
5B	RI01	VREFB5ND	IO			DIFFIO_TX_R4n	DIFFN_R4n*	AE7	DQ23R	DQ12R	DQ6R					
5B	RI01	VREFB5ND	IO			DIFFIO_RX_R4n	DIFFOUT_R4n	AL1	DQ23R	DQ12R	DQ6R					
5B	RI01	VREFB5ND	IO			DIFFIO_TX_R4p	DIFFN_R4p*	AE8								
5B	RI01	VREFB5ND	IO			DIFFIO_RX_R4p	DIFFOUT_R4p	AL3	DQ23R	DQ12R	DQ6R					
5B	RI02	VREFB5ND	IO			DIFFIO_TX_R5n	DIFFN_R5n*	AK1	DQ22R	DQ11R	DQ6R					
5B	RI02	VREFB5ND	IO			DIFFIO_RX_R5n	DIFFOUT_R5n	AJ3	DQ22R	DQ11R	DQ6R					
5B	RI02	VREFB5ND	IO			DIFFIO_TX_R5p										



Pin Information for the Arria® II GX EP2AGX190 Device  
Version 1.1

Bank number	IO Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with no OCT Rd (Note 2)	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note 3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)
5B	RI02	VREFB5ND	IO			DIFFIO_RX_R6n	DIFFN_R6n	AJ2	DQ22R	DQ11R	DQ26R					
5B	RI02	VREFB5ND	IO			DIFFIO_TX_R6p	DIFFN_R6p	AC11	DQS22R	DQ11R/CQn1R	DQ26R/CQn6R					
5B	RI02	VREFB5ND	IO			DIFFIO_RX_R6p	DIFFN_R6p	AH3		DQS21R/DQ11R	DQ26R/DQ6R					
5B	RI02	VREFB5ND	IO			DIFFIO_TX_R7n	DIFFN_R7n	AF9	DQS21R	DQ11R	DQ26R					
5B	RI02	VREFB5ND	IO			DIFFIO_RX_R7n	DIFFN_R7n	AH4	DQ21R	DQ11R	DQ26R					
5B	RI02	VREFB5ND	IO			DIFFIO_TX_R7p	DIFFN_R7p	AF6	DQS21R	DQS11R/CQ11R	DQ26R/CQ6R					
5B	RI02	VREFB5ND	IO			DIFFIO_RX_R7p	DIFFN_R7p	AG4								
5B	RI02	VREFB5ND	IO			DIFFIO_TX_R8n	DIFFN_R8n	AG5	DQ21R	DQ11R	DQ26R					
5B	RI02	VREFB5ND	IO			DIFFIO_RX_R8n	DIFFN_R8n	AES	DQ21R	DQ11R	DQ26R					
5B	RI02	VREFB5ND	IO			DIFFIO_TX_R8p	DIFFN_R8p	AC9								
5B	RI02	VREFB5ND	IO			DIFFIO_RX_R8p	DIFFN_R8p	AES								
5A	RI03	VREFB5ND	IO			DIFFIO_TX_R9n	DIFFN_R9n	AD6	AA6	DQ20R	DQ10R	DQ26R	DQ14R	DQ7R	DQ3R	DQ1R
5A	RI03	VREFB5ND	IO			DIFFIO_RX_R9n	DIFFN_R9n	AD6	AD4	DQ20R	DQ10R	DQ26R	DQ14R	DQ7R	DQ3R	DQ1R
5A	RI03	VREFB5ND	IO			DIFFIO_TX_R9p	DIFFN_R9p	AD7	AB7	DQ20R	DQ10R	DQ26R	DQ14R	DQ7R	DQ3R	DQ1R
5A	RI03	VREFB5ND	IO			DIFFIO_RX_R9p	DIFFN_R9p	AC7	AC5							
5A	RI03	VREFB5ND	IO			DIFFIO_TX_R10n	DIFFN_R10n	AB9	WB	DQS20R	DQ10R	DQ26R	DQS14R	DQ7R	DQ3R	DQ1R
5A	RI03	VREFB5ND	IO			DIFFIO_RX_R10n	DIFFN_R10n	AB7	AB5	DQ20R	DQ10R	DQ26R	DQ14R	DQ7R	DQ3R	DQ1R
5A	RI03	VREFB5ND	IO			DIFFIO_TX_R10p	DIFFN_R10p	AB10	Y9	DQS20R	DQ10R/CQn10R	DQ26R	DQS14R	DQ7R/CQn7R	DQ3R	DQ1R
5A	RI03	VREFB5ND	IO			DIFFIO_RX_R10p	DIFFN_R10p	AB8	AB6							
5A	RI03	VREFB5ND	IO			DIFFIO_TX_R11n	DIFFN_R11n	AH1	AC4	DQS19R	DQS19R/DQ19R	DQ26R	DQS13R	DQ3R/DQ7R	DQ3R	DQ1R
5A	RI03	VREFB5ND	IO			DIFFIO_RX_R11n	DIFFN_R11n	AF4	Y5	DQ19R	DQ10R	DQ26R	DQ13R	DQ3R	DQ1R	DQ1R
5A	RI03	VREFB5ND	IO			DIFFIO_TX_R11p	DIFFN_R11p	AH2	AB4	DQS19R	DQS19R/CQ19R	DQ26R	DQS13R	DQ3R/CQ7R	DQ3R	DQ1R
5A	RI03	VREFB5ND	IO			DIFFIO_RX_R11p	DIFFN_R11p	AES	Y6							
5A	RI03	VREFB5ND	IO			DIFFIO_TX_R12n	DIFFN_R12n	Y6	WB	DQ19R	DQ10R	DQ26R	DQ13R	DQ3R	DQ1R	DQ1R
5A	RI03	VREFB5ND	IO			DIFFIO_RX_R12n	DIFFN_R12n	AG1	AE3	DQ19R	DQ10R	DQ26R	DQ13R	DQ3R	DQ1R	DQ1R
5A	RI03	VREFB5ND	IO			DIFFIO_TX_R12p	DIFFN_R12p	AA7	Y7							
5A	RI03	VREFB5ND	IO			DIFFIO_RX_R12p	DIFFN_R12p	AF1	AD3	DQ19R	DQ10R	DQ26R	DQ13R	DQ3R	DQ1R	DQ1R
5A	RI04	VREFB5ND	IO			DIFFIO_TX_R13n	DIFFN_R13n	AF2	AC2	DQ18R	DQ9R	DQ26R	DQ12R	DQ3R	DQ1R	DQ1R
5A	RI04	VREFB5ND	IO			DIFFIO_RX_R13n	DIFFN_R13n	AE3	AA8	DQ18R	DQ9R	DQ26R	DQ12R	DQ3R	DQ1R	DQ1R
5A	RI04	VREFB5ND	IO			DIFFIO_TX_R13p	DIFFN_R13p	AF3	AC3	DQ18R	DQ9R	DQ26R	DQ12R	DQ3R	DQ1R	DQ1R
5A	RI04	VREFB5ND	IO			DIFFIO_RX_R13p	DIFFN_R13p	AE2	AA4							
5A	RI04	VREFB5ND	IO			DIFFIO_TX_R14n	DIFFN_R14n	AA9	VB	DQS18R	DQ8R	DQ26R	DQS12R	DQ6R	DQ2R	DQ1R
5A	RI04	VREFB5ND	IO			DIFFIO_RX_R14n	DIFFN_R14n	AB5	WB	DQ18R	DQ9R	DQ26R	DQ12R	DQ3R	DQ1R	DQ1R
5A	RI04	VREFB5ND	IO			DIFFIO_TX_R14p	DIFFN_R14p	AA10	U6	DQS18R	DQS18R/CQn18R	DQ26R	DQS12R	DQ6R/CQn6R	DQ2R/CQn2R	DQ1R
5A	RI04	VREFB5ND	IO			DIFFIO_RX_R14p	DIFFN_R14p	AA8	U5							
5A	RI04	VREFB5ND	IO			DIFFIO_TX_R15n	DIFFN_R15n	AE3	AB2	DQS17R	DQS17R/DQ17R	DQ26R	DQS11R	DQ3R/DQ7R	DQ3R	DQ1R
5A	RI04	VREFB5ND	IO			DIFFIO_RX_R15n	DIFFN_R15n	AC4	Y3	DQ17R	DQ9R	DQ26R	DQ11R	DQ3R	DQ1R	DQ1R
5A	RI04	VREFB5ND	IO			DIFFIO_TX_R15p	DIFFN_R15p	AD4	AB3	DQS17R	DQS17R/CQ17R	DQ26R	DQS11R	DQ3R/CQ7R	DQ3R	DQ1R
5A	RI04	VREFB5ND	IO			DIFFIO_RX_R15p	DIFFN_R15p	AC5	Y4							
5A	RI04	VREFB5ND	IO			DIFFIO_TX_R16n	DIFFN_R16n	Y7	T6	DQ17R	DQ9R	DQ26R	DQ11R	DQ3R	DQ1R	DQ1R
5A	RI04	VREFB5ND	IO			DIFFIO_RX_R16n	DIFFN_R16n	AD1	AE1	DQ17R	DQ9R	DQ26R	DQ11R	DQ3R	DQ1R	DQ1R
5A	RI04	VREFB5ND	IO			DIFFIO_TX_R16p	DIFFN_R16p	Y8	Y8							
5A	RI04	VREFB5ND	IO			DIFFIO_RX_R16p	DIFFN_R16p	AC1	AD1	DQ17R	DQ9R	DQ26R	DQ11R	DQ3R	DQ1R	DQ1R
5A	RI05	VREFB5ND	IO			DIFFIO_TX_R17n	DIFFN_R17n	AC2	AC1	DQ16R	DQ8R	DQ26R	DQ10R	DQ3R	DQ1R	DQ1R
5A	RI05	VREFB5ND	IO			DIFFIO_RX_R17n	DIFFN_R17n	AB3	AC1	DQ16R	DQ8R	DQ26R	DQ10R	DQ3R	DQ1R	DQ1R
5A	RI05	VREFB5ND	IO			DIFFIO_TX_R17p	DIFFN_R17p	AC3	AB1	DQ16R	DQ8R	DQ26R	DQ10R	DQ3R	DQ1R	DQ1R
5A	RI05	VREFB5ND	IO			DIFFIO_RX_R17p	DIFFN_R17p	AB4	Y1							
5A	RI05	VREFB5ND	IO			DIFFIO_TX_R18n	DIFFN_R18n	Y10	NA	DQS16R	DQ8R	DQ26R	DQS10R	DQ6R	DQ2R	DQ1R
5A	RI05	VREFB5ND	IO			DIFFIO_RX_R18n	DIFFN_R18n	U3	DQ16R	DQ8R	DQ26R	DQ10R	DQ6R	DQ2R	DQ1R	DQ1R
5A	RI05	VREFB5ND	IO			DIFFIO_TX_R18p	DIFFN_R18p	Y11	P5	DQS16R	DQ8R/CQn8R	DQ26R	DQS10R	DQ6R/CQn6R	DQ2R/CQn2R	DQ1R
5A	RI05	VREFB5ND	IO			DIFFIO_RX_R18p	DIFFN_R18p	AB3	V4							
5A	RI05	VREFB5ND	IO			DIFFIO_TX_R19n	DIFFN_R19n	AA4	W1	DQS15R	DQS15R/DQ15R	DQ26R	DQS9R	DQ3R/DQ7R	DQ3R	DQ1R
5A	RI05	VREFB5ND	IO			DIFFIO_RX_R19n	DIFFN_R19n	AA1	W2	DQ15R	DQ4R	DQ26R	DQ9R	DQ3R	DQ1R	DQ1R
5A	RI05	VREFB5ND	IO			DIFFIO_TX_R19p	DIFFN_R19p	Y5	V7	DQS15R	DQS15R/CQ15R	DQ26R	DQS9R	DQ3R/CQ7R	DQ3R	DQ1R
5A	RI05	VREFB5ND	IO			DIFFIO_RX_R19p	DIFFN_R19p	Y1	W3							
5A	RI05	VREFB5ND	IO			DIFFIO_TX_R20n	DIFFN_R20n	Y9	R6	DQ15R	DQ8R	DQ26R	DQ9R	DQ3R	DQ1R	DQ1R
5A	RI05	VREFB5ND	IO			DIFFIO_RX_R20n	DIFFN_R20n	Y3	U9	DQ15R	DQ8R	DQ26R	DQ9R	DQ3R	DQ1R	DQ1R
5A	RI05	VREFB5ND	IO			DIFFIO_TX_R20p	DIFFN_R20p	W10	P6							
5A	RI05	VREFB5ND	IO			DIFFIO_RX_R20p	DIFFN_R20p	Y4	U5	DQ15R	DQ8R	DQ26R	DQ9R	DQ3R	DQ1R	DQ1R
5A	RI06	VREFB5ND	IO			DIFFIO_TX_R21n	DIFFN_R21n	WB	U3	DQ14R	DQ7R	DQ26R	DQ8R	DQ3R	DQ1R	DQ1R
5A	RI06	VREFB5ND	IO			DIFFIO_RX_R21n	DIFFN_R21n	W1	T3	DQ14R	DQ7R	DQ26R	DQ8R	DQ3R	DQ1R	DQ1R
5A	RI06	VREFB5ND	IO			DIFFIO_TX_R21p	DIFFN_R21p	W7	T4	DQ14R	DQ7R	DQ26R	DQ8R	DQ3R	DQ1R	DQ1R
5A	RI06	VREFB5ND	IO			DIFFIO_RX_R21p	DIFFN_R21p	V2	R3							
5A	RI06	VREFB5ND	IO			DIFFIO_TX_R22n	DIFFN_R22n	V10	N6	DQS14R	DQ7R	DQ26R	DQS8R	DQ4R	DQ2R	DQ1R
5A	RI06	VREFB5ND	IO			DIFFIO_RX_R22n	DIFFN_R22n	W3	U1	DQ14R	DQ7R	DQ26R	DQ8R	DQ3R	DQ1R	DQ1R
5A	RI06	VREFB5ND	IO			DIFFIO_TX_R22p	DIFFN_R22p	V11	M6	DQS14R	DQ7R/CQn7R	DQ26R	DQS8R	DQ4R/CQn4R	DQ2R/CQn2R	DQ1R
5A	RI06	VREFB5ND	IO			DIFFIO_RX_R22p	DIFFN_R22p	W4	T1							
5A	RI06	VREFB5ND	IO			DIFFIO_TX_R23n	DIFFN_R23n	V3	R1	DQS13R	DQS13R/DQ13R	DQ26R	DQS7R	DQ3R/DQ7R	DQ3R	DQ1R
5A	RI06	VREFB5ND	IO			DIFFIO_RX_R23n	DIFFN_R23n	V1	R4	DQ13R	DQ7R	DQ26R	DQ7R	DQ3R	DQ1R	DQ1R
5A	RI06	VREFB5ND	IO			DIFFIO_TX_R23p	DIFFN_R23p	V4	P1	DQS13R	DQS13R/CQ13R	DQ26R	DQS7R	DQ3R/CQ7R	DQ3R	DQ1R
5A	RI06	VREFB5ND	IO			DIFFIO_RX_R23p	DIFFN_R23p	V2	R5							
5A	RI06	VREFB5ND	IO			DIFFIO_TX_R24n	DIFFN_R24n	W12	M5	DQ13R	DQ7R	DQ26R	DQ7R	DQ3R	DQ1R	DQ1R
5A	RI06	VREFB5ND	IO			DIFFIO_RX_R24n	DIFFN_R24n	V7	P3	DQ13R	DQ7R	DQ26R	DQ7R	DQ3R	DQ1R	DQ1R
5A	RI06	VREFB5ND	IO			DIFFIO_TX_R24p	DIFFN_R24p	V12	L6							
5A	RI06	VREFB5ND	IO			DIFFIO_RX_R24p	DIFFN_R24p	U7	P4	DQ13R	DQ7R	DQ26R	DQ7R	DQ3R	DQ1R	DQ1R
5A	VREFB5ND	CLK8	IO	DIFFCLK_8n				U5	P2							
5A	VREFB5ND	CLK10	IO	DIFFCLK_10n				U6	M7							
5A	VREFB5ND	CLK9	IO	DIFFCLK_9n				U5	N1							
5A	VREFB5ND	CLK11	IO	DIFFCLK_11n				U6	M7							
6A	RI07	VREFB6ND	IO			DIFFIO_TX_R25n	DIFFN_R25n	Y7	L1	DQ12R	DQ6R	DQ26R	DQ6R	DQ3R	DQ1R	DQ1R
6A	RI07	VREFB6ND	IO			DIFFIO_RX_R25n	DIFFN_R25n	U1	M2	DQ12R	DQ6R	DQ26R	DQ6R	DQ3R	DQ1R	DQ1R
6A	RI07	VREFB6ND	IO			DIFFIO_TX_R25p	DIFFN_R25p	R7	K1	DQ12R	DQ6R	DQ26R	DQ6R	DQ3R	DQ1R	DQ1R
6A	RI07	VREFB6ND	IO			DIFFIO_RX_R25p	DIFFN_R25p	U2	L3							
6A	RI07	VREFB6ND	IO			DIFFIO_TX_R26n	DIFFN_R26n	U10	K6	DQS12R	DQ6R	DQ26R	DQ6R	DQ3R	DQ1R	DQ1R
6A	RI07	VREFB6ND	IO			DIFFIO_RX_R26n	DIFFN_R26n	U11	M3	DQ12R	DQ6R	DQ26R	DQ6R	DQ3R	DQ1R	DQ1R
6A	RI07	VREFB6ND	IO			DIFFIO_TX_R26p	DIFFN_R26p	U11	L7	DQS12R	DQS12R/CQ12R	DQ26R	DQ6R/CQ6R	DQ3R/CQ3R	DQ1R/CQ1R	DQ1R
6A	RI07	VREFB6ND	IO			DIFFIO_RX_R26p	DIFFN_R26p	R1	M4							
6A	RI07	VREFB6ND	IO			DIFFIO_TX_R27n	DIFFN_R27n	P1	J2	DQS11R	DQS11R/DQ11R	DQ26R	DQ5R	DQ3R/DQ7R	DQ3R	DQ1R
6A	RI07	VREFB6ND	IO			DIFFIO_RX_R27n	DIFFN_R27n	U3	J3	DQ11R	DQ5R	DQ26R	DQ5R	DQ3R	DQ1R	DQ1R
6A	RI07	VREFB6ND	IO			DIFFIO_TX_R27p	DIFFN_R27p	R2	J3	DQS11R	DQS11R/CQ11R	DQ26R	DQ5R	DQ3R/CQ3R	DQ1R/CQ1R	DQ1R
6A	RI07	VREFB6ND	IO			DIFFIO_RX_R27p	DIFFN_R27p	U4	H1							
6A	RI07	VREFB6ND	IO			DIFFIO_TX_R28n	DIFFN_R28n	U9	J8	DQ11R	DQ5R	DQ26R	DQ5R	DQ3R	DQ1R	DQ1R
6A	RI07	VREFB6ND	IO			DIFFIO_RX_R28n	DIFFN_R28n</									



Bank number	IO Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note 3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)
6A	RC08	VREFBAND	IO			DIFFIO_RX_R31p	DIFFN_R31p	P4	H4								
6A	RC08	VREFBAND	IO			DIFFIO_TX_R32n	DIFFN_R32n	R9	K8	DQ0R	DQ0R	DQ3R	DQ1R	DQ3R	DQ2R	DQ1R	
6A	RC08	VREFBAND	IO			DIFFIO_RX_R32n	DIFFOUT_R32n	J1	K4	DQ0R	DQ0R	DQ3R	DQ1R	DQ3R	DQ2R	DQ1R	
6A	RC08	VREFBAND	IO			DIFFIO_TX_R32p	DIFFN_R32p	H10	K9								
6A	RC08	VREFBAND	IO			DIFFIO_RX_R32p	DIFFOUT_R32p	L2	K5	DQ0R	DQ0R	DQ3R	DQ1R	DQ3R	DQ2R	DQ1R	
6A	RC09	VREFBAND	IO			DIFFIO_TX_R33n	DIFFN_R33n	H1		DQ0R	DQ0R	DQ2R	DQ1R				
6A	RC09	VREFBAND	IO			DIFFIO_RX_R33n	DIFFOUT_R33n	F1		DQ0R	DQ0R	DQ2R	DQ1R				
6A	RC09	VREFBAND	IO			DIFFIO_TX_R33p	DIFFN_R33p	G1		DQ0R	DQ0R	DQ2R	DQ1R				
6A	RC09	VREFBAND	IO			DIFFIO_RX_R33p	DIFFOUT_R33p	E1									
6A	RC09	VREFBAND	IO			DIFFIO_TX_R34n	DIFFN_R34n	P7		DQ0nR	DQ0R	DQ2R	DQ1R				
6A	RC09	VREFBAND	IO			DIFFIO_RX_R34n	DIFFOUT_R34n	D1		DQ0R	DQ0R	DQ2R	DQ1R				
6A	RC09	VREFBAND	IO			DIFFIO_TX_R34p	DIFFN_R34p	R8		DQ0nR	DQ0R/CQ0R	DQ2R/CQ2R	DQ1R				
6A	RC09	VREFBAND	IO			DIFFIO_RX_R34p	DIFFOUT_R34p	D2									
6A	RC09	VREFBAND	IO			DIFFIO_TX_R35n	DIFFN_R35n	N3		DQ0n7R	DQ0n4R/DQ0R	DQ0n2R/DQ0R	DQ1R				
6A	RC09	VREFBAND	IO			DIFFIO_RX_R35n	DIFFOUT_R35n	N4		DQ0R	DQ0R	DQ2R	DQ1R				
6A	RC09	VREFBAND	IO			DIFFIO_TX_R35p	DIFFN_R35p	M3		DQ07R	DQ054R/CQ0R	DQ052R/CQ0R	DQ1R				
6A	RC09	VREFBAND	IO			DIFFIO_RX_R35p	DIFFOUT_R35p	N5									
6A	RC09	VREFBAND	IO			DIFFIO_TX_R36n	DIFFN_R36n	P9		DQ0R	DQ0R	DQ2R	DQ1R				
6A	RC09	VREFBAND	IO			DIFFIO_RX_R36n	DIFFOUT_R36n	C1		DQ0R	DQ0R	DQ2R	DQ1R				
6A	RC09	VREFBAND	IO			DIFFIO_TX_R36p	DIFFN_R36p	P10									
6A	RC09	VREFBAND	IO			DIFFIO_RX_R36p	DIFFOUT_R36p	C2		DQ0R	DQ0R	DQ2R	DQ1R				
6A	RC10	VREFBAND	IO		DATA7	DIFFIO_TX_R37n	DIFFN_R37n	K2	B1	DQ0R	DQ0R	DQ2R	DQ1R	DQ2R	DQ1R		
6A	RC10	VREFBAND	IO		DATA8	DIFFIO_RX_R37n	DIFFOUT_R37n	M4	C2	DQ0R	DQ0R	DQ2R	DQ1R	DQ2R	DQ1R		
6A	RC10	VREFBAND	IO		DATA5	DIFFIO_TX_R37p	DIFFN_R37p	K3	A2	DQ0R	DQ0R	DQ2R	DQ1R	DQ2R	DQ1R		
6A	RC10	VREFBAND	IO		DATA4	DIFFIO_RX_R37p	DIFFOUT_R37p	L4	C3								
6A	RC10	VREFBAND	IO		DATA3	DIFFIO_TX_R38n	DIFFN_R38n	P6	H6	DQ0nR	DQ0R	DQ2R	DQ1R	DQ0n2R	DQ0R		
6A	RC10	VREFBAND	IO		DATA2	DIFFIO_RX_R38n	DIFFOUT_R38n	G2	G3	DQ0R	DQ0R	DQ2R	DQ1R	DQ0R	DQ0R		
6A	RC10	VREFBAND	IO		DATA1	DIFFIO_TX_R38p	DIFFN_R38p	N6	H7	DQ0nR	DQ0R/CQ0R	DQ2R	DQ1R	DQ0n2R	DQ0R		
6A	RC10	VREFBAND	IO		CLK0nR	DIFFIO_RX_R38p	DIFFOUT_R38p	F7	G4								
6A	RC10	VREFBAND	IO			DIFFIO_TX_R39n	DIFFN_R39n	J4	E3	DQ0n5R	DQ0n3R/DQ0R	DQ2R	DQ1R	DQ0n1R	DQ0R		
6A	RC10	VREFBAND	IO			DIFFIO_RX_R39n	DIFFOUT_R39n	J3	F3	DQ0R	DQ0R	DQ2R	DQ1R	DQ0R	DQ0R		
6A	RC10	VREFBAND	IO			DIFFIO_TX_R39p	DIFFN_R39p	L5	D3	DQ0nR	DQ0n3R/CQ0R	DQ2R	DQ1R	DQ0n1R	DQ0R		
6A	RC10	VREFBAND	IO		DEV_OE	DIFFIO_RX_R39p	DIFFOUT_R39p	H3	F4								
6A	RC10	VREFBAND	IO			DIFFIO_TX_R40n	DIFFN_R40n	N9	G5	DQ0R	DQ0R	DQ2R	DQ1R	DQ0R	DQ0R		
6A	RC10	VREFBAND	IO			DIFFIO_RX_R40n	DIFFOUT_R40n	K4	E4	DQ0R	DQ0R	DQ2R	DQ1R	DQ0R	DQ0R		
6A	RC10	VREFBAND	IO		DEV_CLRn	DIFFIO_TX_R40p	DIFFN_R40p	N10									
6A	RC10	VREFBAND	IO			DIFFIO_RX_R40p	DIFFOUT_R40p	K5	F5	DQ0R	DQ0R	DQ2R	DQ1R	DQ0R	DQ0R		
6B	RC11	VREFBAND	IO			DIFFIO_TX_R41n	DIFFN_R41n	M5	C3	DQ0R	DQ0R	DQ2R	DQ1R				
6B	RC11	VREFBAND	IO			DIFFIO_RX_R41n	DIFFOUT_R41n	C3	D3	DQ0R	DQ0R	DQ2R	DQ1R				
6B	RC11	VREFBAND	IO			DIFFIO_TX_R41p	DIFFN_R41p	M6	D4	DQ0R	DQ0R	DQ2R	DQ1R				
6B	RC11	VREFBAND	IO			DIFFIO_RX_R41p	DIFFOUT_R41p	H4									
6B	RC11	VREFBAND	IO			DIFFIO_TX_R42n	DIFFN_R42n	N7		DQ0n4R	DQ0R	DQ1R					
6B	RC11	VREFBAND	IO			DIFFIO_RX_R42n	DIFFOUT_R42n	F3		DQ0R	DQ0R	DQ1R					
6B	RC11	VREFBAND	IO			DIFFIO_TX_R42p	DIFFN_R42p	N9		DQ04R	DQ0R/CQ0R	DQ1R/CQ0R					
6B	RC11	VREFBAND	IO			DIFFIO_RX_R42p	DIFFOUT_R42p	F4									
6B	RC11	VREFBAND	IO			DIFFIO_TX_R43n	DIFFN_R43n	D3		DQ0n3R	DQ0n2R/DQ0R	DQ0n1R/DQ0R					
6B	RC11	VREFBAND	IO			DIFFIO_RX_R43n	DIFFOUT_R43n	E3		DQ0R	DQ0R	DQ1R					
6B	RC11	VREFBAND	IO			DIFFIO_TX_R43p	DIFFN_R43p	D4		DQ0nR	DQ0n3R/CQ0R	DQ0n1R/CQ0R					
6B	RC11	VREFBAND	IO			DIFFIO_RX_R43p	DIFFOUT_R43p	E4									
6B	RC11	VREFBAND	IO			DIFFIO_TX_R44n	DIFFN_R44n	M9		DQ0R	DQ0R	DQ1R					
6B	RC11	VREFBAND	IO			DIFFIO_RX_R44n	DIFFOUT_R44n	K6		DQ0R	DQ0R	DQ1R					
6B	RC11	VREFBAND	IO			DIFFIO_TX_R44p	DIFFN_R44p	M10									
6B	RC11	VREFBAND	IO			DIFFIO_RX_R44p	DIFFOUT_R44p	K7		DQ0R	DQ0R	DQ1R					
6B	RC12	VREFBAND	IO			DIFFIO_TX_R45n	DIFFN_R45n	L6		DQ0R	DQ0R	DQ1R					
6B	RC12	VREFBAND	IO			DIFFIO_RX_R45n	DIFFOUT_R45n	G4		DQ0R	DQ0R	DQ1R					
6B	RC12	VREFBAND	IO			DIFFIO_TX_R45p	DIFFN_R45p	J7		DQ0R	DQ0R	DQ1R					
6B	RC12	VREFBAND	IO			DIFFIO_RX_R45p	DIFFOUT_R45p	C5									
6B	RC12	VREFBAND	IO			DIFFIO_TX_R46n	DIFFN_R46n	M7		DQ0n2R	DQ0R	DQ1R					
6B	RC12	VREFBAND	IO			DIFFIO_RX_R46n	DIFFOUT_R46n	C5		DQ0R	DQ0R	DQ1R					
6B	RC12	VREFBAND	IO			DIFFIO_TX_R46p	DIFFN_R46p	M8		DQ02R	DQ0R/CQ0R	DQ1R					
6B	RC12	VREFBAND	IO			DIFFIO_RX_R46p	DIFFOUT_R46p	D5									
6B	RC12	VREFBAND	IO			DIFFIO_TX_R47n	DIFFN_R47n	P5		DQ0n1R	DQ0n1R/DQ0R	DQ1R					
6B	RC12	VREFBAND	IO			DIFFIO_RX_R47n	DIFFOUT_R47n	C6		DQ0R	DQ0R	DQ1R					
6B	RC12	VREFBAND	IO			DIFFIO_TX_R47p	DIFFN_R47p	S6		DQ01R	DQ0n1R/CQ0R	DQ1R					
6B	RC12	VREFBAND	IO			DIFFIO_RX_R47p	DIFFOUT_R47p	D6									
6B	RC12	VREFBAND	IO			DIFFIO_TX_R48n	DIFFN_R48n	L7		DQ0R	DQ0R	DQ1R					
6B	RC12	VREFBAND	IO			DIFFIO_RX_R48n	DIFFOUT_R48n	H7		DQ0R	DQ0R	DQ1R					
6B	RC12	VREFBAND	IO			DIFFIO_TX_R48p	DIFFN_R48p	K8									
6B	RC12	VREFBAND	IO			DIFFIO_RX_R48p	DIFFOUT_R48p	J8		DQ0R	DQ0R	DQ1R					
7B	TIO12	VREFBAND	IO			DIFFIO_TX_T1p	DIFFN_T1p	L11		DQ24T	DQ12T	DQ0T					
7B	TIO12	VREFBAND	IO			DIFFIO_RX_T1n	DIFFOUT_T1n	E6		DQ24T	DQ12T	DQ0T					
7B	TIO12	VREFBAND	IO			DIFFIO_TX_T1p	DIFFN_T1p	K11		DQ24T	DQ12T	DQ0T					
7B	TIO12	VREFBAND	IO			DIFFIO_RX_T2p	DIFFOUT_T2p	G7									
7B	TIO12	VREFBAND	IO			DIFFIO_TX_T2p	DIFFN_T2p	H9		DQ024T	DQ012T/CQ012T	DQ0T					
7B	TIO12	VREFBAND	IO			DIFFIO_RX_T2n	DIFFOUT_T2n	F7		DQ24T	DQ12T	DQ0T					
7B	TIO12	VREFBAND	IO			DIFFIO_TX_T2n	DIFFN_T2n	G9		DQ0n24T	DQ0n12T/DQ012T	DQ0T					
7B	TIO12	VREFBAND	IO			DIFFIO_RX_T3p	DIFFOUT_T3p	E7									
7B	TIO12	VREFBAND	IO			DIFFIO_TX_T3n	DIFFN_T3n	L10		DQ023T	DQ012T/CQ012T	DQ0T					
7B	TIO12	VREFBAND	IO			DIFFIO_RX_T3n	DIFFOUT_T3n	D7		DQ23T	DQ12T	DQ0T					
7B	TIO12	VREFBAND	IO			DIFFIO_TX_T3n	DIFFN_T3n	L9		DQ0n23T	DQ012T	DQ0T					
7B	TIO12	VREFBAND	IO			DIFFIO_RX_T4p	DIFFOUT_T4p	H10									
7B	TIO12	VREFBAND	IO			DIFFIO_TX_T4p	DIFFN_T4p	F9		DQ23T	DQ12T	DQ0T					
7B	TIO12	VREFBAND	IO			DIFFIO_RX_T4n	DIFFOUT_T4n	G10		DQ23T	DQ12T	DQ0T					
7B	TIO12	VREFBAND	IO			DIFFIO_TX_T4n	DIFFN_T4n	H10		DQ23T	DQ12T	DQ0T					
7B	TIO11	VREFBAND	IO			DIFFIO_RX_T5p	DIFFOUT_T5p	C8		DQ22T	DQ11T	DQ0T					
7B	TIO11	VREFBAND	IO			DIFFIO_TX_T5p	DIFFN_T5p	K7		DQ22T	DQ11T	DQ0T					
7B	TIO11	VREFBAND	IO			DIFFIO_RX_T5n	DIFFOUT_T5n	C7		DQ22T	DQ11T	DQ0T					
7B	TIO11	VREFBAND	IO			DIFFIO_TX_T5n	DIFFN_T5n	H11		DQ22T	DQ11T	DQ0T					
7B	TIO11	VREFBAND	IO			DIFFIO_RX_T6p	DIFFOUT_T6p	F10									
7B	TIO11	VREFBAND	IO			DIFFIO_TX_T6p	DIFFN_T6p	J12		DQ022T	DQ011T/CQ011T	DQ00T/CQ00T					
7B	TIO11	VREFBAND	IO			DIFFIO_RX_T6n	DIFFOUT_T6n	E8		DQ21T	DQ11T	DQ0T					
7B	TIO11	VREFBAND	IO			DIFFIO_TX_T6n	DIFFN_T6n	H12		DQ0n22T	DQ011T/DQ011T	DQ0n0T/DQ00T					
7B	TIO11	VREFBAND	IO			DIFFIO_RX_T7p	DIFFOUT_T7p	E10									
7B	TIO11	VREFBAND	IO			DIFFIO_TX_T7p	DIFFN_T7p	M13		DQ021T	DQ011T/CQ011T	DQ00T/CQ00T					
7B	TIO11	VREFBAND	IO			DIFFIO_RX_T7n	DIFFOUT_T7n	D9		DQ21T	DQ11T	DQ0T					
7B	TIO11	VREFBAND	IO			DIFFIO_TX_T7n	DIFFN_T7n	L13		DQ0n21T	DQ011T	DQ0T					
7B	TIO11	VREFBAND	IO			DIFFIO_RX_T8p	DIFFOUT_T8p	D10									
7B	TIO11	VREFBAND	IO			DIFFIO_TX_T8p	DIFFN_T8p	J13		DQ21T	DQ11T	DQ0T					
7B	TIO11	VREFBAND	IO														





Bank number	IO Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with no OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note 3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)
8A	T104	VREFBAND	IO			DIFFIO_TX_T34n	DIFFN_T34n	802	E24	DQSn8T	DQSn4T/DQ4T	DQSn2T/CQ2T	DQ1T	DQSn2T	DQSn1T/DQ1T		
8A	T104	VREFBAND	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	023	F21								
8A	T104	VREFBAND	IO			DIFFIO_TX_T35p	DIFFN_T35p	023	K18	DQ87T	DQ4T/CQ4T	DQ2T/CQ2T	DQ1T	DQ81T	DQ1T/CQ1T		
8A	T104	VREFBAND	IO			DIFFIO_RX_T35n	DIFFOUT_T35n	C34	L21	DQ4T	DQ4T	DQ2T	DQ1T	DQ4T	DQ1T		
8A	T104	VREFBAND	IO			DIFFIO_TX_T35n	DIFFN_T35n	P23	J17	DQ8n7T	DQ4T	DQ2T	DQ1T	DQ8n1T	DQ1T		
8A	T104	VREFBAND	IO		CRC_ERROR	DIFFIO_RX_T36p	DIFFOUT_T36p	F24	E19	DQ7T	DQ4T	DQ2T	DQ1T	DQ7T	DQ1T		
8A	T104	VREFBAND	IO			DIFFIO_TX_T36p	DIFFN_T36p	024	G18	DQ7T	DQ4T	DQ2T	DQ1T	DQ7T	DQ1T		
8A	T104	VREFBAND	IO			DIFFIO_RX_T36n	DIFFOUT_T36n	E24	E18	DQ7T	DQ4T	DQ2T	DQ1T	DQ7T	DQ1T		
8A	T104	VREFBAND	IO			DIFFIO_TX_T36n	DIFFN_T36n	C25	G18	DQ7T	DQ4T	DQ2T	DQ1T	DQ7T	DQ1T		
8A	T103	VREFBAND	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	P21	J18	DQ6T	DQ3T	DQ2T	DQ1T	DQ6T	DQ1T		
8A	T103	VREFBAND	IO			DIFFIO_TX_T37p	DIFFN_T37p	N29									
8A	T103	VREFBAND	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	E21	J18	DQ6T	DQ3T	DQ2T	DQ1T	DQ6T	DQ1T		
8A	T103	VREFBAND	IO			DIFFIO_TX_T37n	DIFFN_T37n	M20		DQ6T	DQ3T	DQ2T	DQ1T	DQ6T	DQ1T		
8A	T103	VREFBAND	IO			DIFFIO_RX_T38p	DIFFOUT_T38p	D27									
8A	T103	VREFBAND	IO			DIFFIO_TX_T38p	DIFFN_T38p	D25	DQ8T	DQ8T	DQ3T/CQ3T	DQ2T	DQ1T	DQ8T	DQ1T		
8A	T103	VREFBAND	IO			DIFFIO_RX_T38n	DIFFOUT_T38n	C27	DQ6T	DQ6T	DQ3T	DQ2T	DQ1T	DQ6T	DQ1T		
8A	T103	VREFBAND	IO			DIFFIO_TX_T38n	DIFFN_T38n	C26	DQ8nT	DQ8nT	DQ3T/DQ3T	DQ2T	DQ1T	DQ8nT	DQ1T		
8A	T103	VREFBAND	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	E22									
8A	T103	VREFBAND	IO			DIFFIO_TX_T39p	DIFFN_T39p	H21	DQ8ST	DQ3T/CQ3T	DQ2T	DQ1T	DQ8ST	DQ1T			
8A	T103	VREFBAND	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	D22	DQ6T	DQ3T	DQ2T	DQ1T	DQ6T	DQ1T			
8A	T103	VREFBAND	IO			DIFFIO_TX_T39n	DIFFN_T39n	G22	DQ8n5T	DQ3T	DQ2T	DQ1T	DQ8n5T	DQ1T			
8A	T103	VREFBAND	IO			DIFFIO_RX_T40p	DIFFOUT_T40p	D29									
8A	T103	VREFBAND	IO			DIFFIO_TX_T40p	DIFFN_T40p	C30	DQ6T	DQ3T	DQ2T	DQ1T	DQ6T	DQ1T			
8A	T103	VREFBAND	IO			DIFFIO_RX_T40n	DIFFOUT_T40n	D28	DQ6T	DQ3T	DQ2T	DQ1T	DQ6T	DQ1T			
8A	T103	VREFBAND	IO			DIFFIO_TX_T40n	DIFFN_T40n	C29	DQ6T	DQ3T	DQ2T	DQ1T	DQ6T	DQ1T			
8A	VREFBAND	IO		RUP2				E26	L21								
8A	VREFBAND	IO	PLL1_CLKOUT1p					M21	K19								
8A	VREFBAND	IO	RDN2					D26	K21								
8A	VREFBAND	IO	PLL1_CLKOUT1n					L21	J18								
8A	VREFBAND	IO	PLL1_CLKOUT2p					F26	F20								
8A	VREFBAND	IO	PLL1_CLKOUT3p					K21	J18								
8A	VREFBAND	IO	PLL1_CLKOUT2n					E26	F19								
8A	VREFBAND	IO	PLL1_CLKOUT3n					L21	H19								
8B	T102	VREFBAND	IO			DIFFIO_RX_T41p	DIFFOUT_T41p	S25	DQ4T	DQ4T	DQ2T	DQ1T	DQ4T	DQ1T			
8B	T102	VREFBAND	IO			DIFFIO_TX_T41p	DIFFN_T41p	K23	DQ4T	DQ4T	DQ2T	DQ1T	DQ4T	DQ1T			
8B	T102	VREFBAND	IO			DIFFIO_RX_T41n	DIFFOUT_T41n	S24	DQ4T	DQ4T	DQ2T	DQ1T	DQ4T	DQ1T			
8B	T102	VREFBAND	IO			DIFFIO_TX_T41n	DIFFN_T41n	L22	DQ4T	DQ4T	DQ2T	DQ1T	DQ4T	DQ1T			
8B	T102	VREFBAND	IO			DIFFIO_RX_T42p	DIFFOUT_T42p	027									
8B	T102	VREFBAND	IO			DIFFIO_TX_T42p	DIFFN_T42p	H27	DQ84T	DQ82T/CQ2T	DQ81T/CQ1T						
8B	T102	VREFBAND	IO			DIFFIO_RX_T42n	DIFFOUT_T42n	L28	DQ4T	DQ4T	DQ2T	DQ1T	DQ4T	DQ1T			
8B	T102	VREFBAND	IO			DIFFIO_TX_T42n	DIFFN_T42n	S26	DQ8n4T	DQ8n2T/DQ2T	DQ8n1T/DQ1T						
8B	T102	VREFBAND	IO			DIFFIO_RX_T43p	DIFFOUT_T43p	C28									
8B	T102	VREFBAND	IO			DIFFIO_TX_T43p	DIFFN_T43p	L22	DQ83T	DQ2T/CQ2T	DQ1T/CQ1T						
8B	T102	VREFBAND	IO			DIFFIO_RX_T43n	DIFFOUT_T43n	S27	DQ3T	DQ3T	DQ2T	DQ1T	DQ3T	DQ1T			
8B	T102	VREFBAND	IO			DIFFIO_TX_T43n	DIFFN_T43n	K27	DQ8n3T	DQ2T	DQ2T	DQ1T	DQ8n3T	DQ1T			
8B	T102	VREFBAND	IO			DIFFIO_RX_T44p	DIFFOUT_T44p	L28									
8B	T102	VREFBAND	IO			DIFFIO_TX_T44p	DIFFN_T44p	F27	DQ3T	DQ3T	DQ2T	DQ1T	DQ3T	DQ1T			
8B	T102	VREFBAND	IO			DIFFIO_RX_T44n	DIFFOUT_T44n	K28	DQ3T	DQ3T	DQ2T	DQ1T	DQ3T	DQ1T			
8B	T102	VREFBAND	IO			DIFFIO_TX_T44n	DIFFN_T44n	E27	DQ3T	DQ3T	DQ2T	DQ1T	DQ3T	DQ1T			
8B	T101	VREFBAND	IO			DIFFIO_RX_T45p	DIFFOUT_T45p	J29	DQ2T	DQ2T	DQ1T	DQ1T	DQ2T	DQ1T			
8B	T101	VREFBAND	IO			DIFFIO_TX_T45p	DIFFN_T45p	K24									
8B	T101	VREFBAND	IO			DIFFIO_RX_T45n	DIFFOUT_T45n	H28	DQ2T	DQ2T	DQ1T	DQ1T	DQ2T	DQ1T			
8B	T101	VREFBAND	IO			DIFFIO_TX_T45n	DIFFN_T45n	J24	DQ2T	DQ2T	DQ1T	DQ1T	DQ2T	DQ1T			
8B	T101	VREFBAND	IO			DIFFIO_RX_T46p	DIFFOUT_T46p	C30									
8B	T101	VREFBAND	IO			DIFFIO_TX_T46p	DIFFN_T46p	J30	DQ82T	DQ81T/CQ1T	DQ1T	DQ1T	DQ82T	DQ1T			
8B	T101	VREFBAND	IO			DIFFIO_RX_T46n	DIFFOUT_T46n	F30	DQ2T	DQ2T	DQ1T	DQ1T	DQ2T	DQ1T			
8B	T101	VREFBAND	IO			DIFFIO_TX_T46n	DIFFN_T46n	H30	DQ8n2T	DQ8n1T/DQ1T	DQ1T	DQ1T	DQ8n2T	DQ1T			
8B	T101	VREFBAND	IO			DIFFIO_RX_T47p	DIFFOUT_T47p	F28									
8B	T101	VREFBAND	IO			DIFFIO_TX_T47p	DIFFN_T47p	L25	DQ81T	DQ81T/CQ1T	DQ1T	DQ1T	DQ81T	DQ1T			
8B	T101	VREFBAND	IO			DIFFIO_RX_T47n	DIFFOUT_T47n	E28	DQ1T	DQ1T	DQ1T	DQ1T	DQ1T	DQ1T			
8B	T101	VREFBAND	IO			DIFFIO_TX_T47n	DIFFN_T47n	H24	DQ8n1T	DQ1T	DQ1T	DQ1T	DQ8n1T	DQ1T			
8B	T101	VREFBAND	IO			DIFFIO_RX_T48p	DIFFOUT_T48p	S29									
8B	T101	VREFBAND	IO			DIFFIO_TX_T48p	DIFFN_T48p	E30	DQ1T	DQ1T	DQ1T	DQ1T	DQ1T	DQ1T			
8B	T101	VREFBAND	IO			DIFFIO_RX_T48n	DIFFOUT_T48n	F29	DQ1T	DQ1T	DQ1T	DQ1T	DQ1T	DQ1T			
8B	T101	VREFBAND	IO			DIFFIO_TX_T48n	DIFFN_T48n	D30	DQ1T	DQ1T	DQ1T	DQ1T	DQ1T	DQ1T			
8C			ID0		ID0			M27	L23								
8C			ACSO		ACSO			K27	I22								
8C			ACSO		ACSO			M26	H22								
8C			DATA		DATA			N26	K22								
8C			ID1		ID1			M25	H24								
8C			TMS		TMS			N25	J23								
8C			TCX		TCX			L24	L24								
8C			DCLK		DCLK			L25	K24								
			GND					J17	P14								
			GND					AD27	AB21								
			GND					M28	C22								
			GND					N27	K23								
			GND					V34	V28								
			GND					V33	V27								
			GND					V30	W26								
			GND					V29	W25								
			GND					V27	V29								
			GND					V25	V27								
			GND					W32	U26								
			GND					W31	U25								
			GND					W28	V28								
			GND					W26	V27								
			GND					V34	V24								
			GND					W33	V22								
			GND					V30	R26								
			GND					V27	R23								
			GND					V25	R21								
			GND					U32	P26								
			GND					U31	P27								
			GND					U28	P24								
			GND					U26	P22								
			GND					T34	N28								
			GND					T33	N25								
			GND					T30	N23								
			GND					T29	N21								
			GND					T27	M28								
			GND					T26	M27								
			GND					R29	M24								
			GND					R31	L26								
			GND					R28	L25								



Bank number	IO Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note 3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)
			GND					K0	K25								
			GND					P34	K27								
			GND					P33	J26								
			GND					P30	J25								
			GND					P29	H28								
			GND					P28	H27								
			GND					P26	G26								
			GND					K32	G25								
			GND					N31	F28								
			GND					M34	F27								
			GND					M33	F26								
			GND					M30	E25								
			GND					M29	D28								
			GND					L32	D27								
			GND					L31	D24								
			GND					K34	D22								
			GND					K33	C26								
			GND					K30	C25								
			GND					K29	C24								
			GND					K32	C22								
			GND					J31	B28								
			GND					H34	B27								
			GND					H33	B25								
			GND					G32	B23								
			GND					G31	B22								
			GND					F34	B21								
			GND					F33	AH28								
			GND					E32	AH24								
			GND					E31	AH22								
			GND					D34	AH20								
			GND					D33	AG28								
			GND					C32	AG26								
			GND					C31	AG24								
			GND					B34	AG22								
			GND					B33	AG21								
			GND					B30	AG20								
			GND					B29	AF28								
			GND					B28	AF27								
			GND					AP33	AF26								
			GND					AP32	AF25								
			GND					AP30	AF23								
			GND					AK32	AE26								
			GND					AN31	AE25								
			GND					AN30	AE23								
			GND					AM34	AD28								
			GND					AM33	AD27								
			GND					AL32	AC28								
			GND					AL31	AC25								
			GND					AK34	AB28								
			GND					AK33	AB27								
			GND					AL32	AA28								
			GND					AL31	AA25								
			GND					AH34	A27								
			GND					AH33	A26								
			GND					AG32	A23								
			GND					AG31	A21								
			GND					AF34	I27								
			GND					AF33	W9								
			GND					AF30	W22								
			GND					AF29	W19								
			GND					AE32	W17								
			GND					AE31	W15								
			GND					AD34	V8								
			GND					AD33	V6								
			GND					AD30	V20								
			GND					AD29	V2								
			GND					AC32	V16								
			GND					AC31	V16								
			GND					AB34	V14								
			GND					AB33	V12								
			GND					AB30	V10								
			GND					AB29	U9								
			GND					AB27	U17								
			GND					AA32	U13								
			GND					AA31	T8								
			GND					AA28	T25								
			GND					AA26	T18								
			GND					A33	T14								
			GND					A32	T10								
			GND					A31	R19								
			GND					A30	R13								
			GND					A28	P18								
			GND					V23	P12								
			GND					V21	N9								
			GND					V19	N5								
			GND					Y17	N19								
			GND					Y16	N15								
			GND					Y13	N11								
			GND					W8	M16								
			GND					W5	M12								
			GND					W22	L8								
			GND					W20	L20								
			GND					W2	L17								
			GND					W18	L11								
			GND					W16	H8								
			GND					W14	H17								
			GND					W11	G9								
			GND					V23	E23								
			GND					V21	E11								
			GND					V19	B2								
			GND					Y16	AG8								
			GND					V13	AG14								
			GND					J22	AD20								
			GND					L20	AD11								
			GND					U18	AA20								
			GND					U16	AA11								



Bank number	IO Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note 3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)
			GND					U14	U15								
			GND					T8	U15								
			GND					T5	U11								
			GND					V23	V5								
			GND					V21	V2								
			GND					T2	T16								
			GND					T16	T12								
			GND					T17	R9								
			GND					T15	R17								
			GND					T13	R11								
			GND					T11	P16								
			GND					R22	P10								
			GND					R20	N8								
			GND					R18	N2								
			GND					R16	N17								
			GND					R14	N13								
			GND					P8	M16								
			GND					P5	M14								
			GND					P25	M10								
			GND					P23	L5								
			GND					P21	L2								
			GND					P2	L14								
			GND					P13	H8								
			GND					P17	H2								
			GND					P15	H11								
			GND					P13	E23								
			GND					P11	E14								
			GND					N24	B20								
			GND					N22	B11								
			GND					N18	AG17								
			GND					N16	AD5								
			GND					N14	AD14								
			GND					N12	AA5								
			GND					L8	AA14								
			GND					L5	H20								
			GND					L28	H14								
			GND					L23	E5								
			GND					L20	E17								
			GND					L2	B6								
			GND					L17	B14								
			GND					L14	AG2								
			GND					K10	AD6								
			GND					J9	AD17								
			GND					H8	AA8								
			GND					H5	AA17								
			GND					H29	E8								
			GND					H26	E2								
			GND					H23	B6								
			GND					H20	B17								
			GND					H2	AG5								
			GND					H17	AG11								
			GND					H14	AD2								
			GND					H11	AB23								
			GND					E8	AA2								
			GND					E5									
			GND					E29									
			GND					E28									
			GND					E23									
			GND					E20									
			GND					E2									
			GND					E17									
			GND					E14									
			GND					E11									
			GND					B8									
			GND					B5									
			GND					B26									
			GND					B23									
			GND					B20									
			GND					B2									
			GND					B17									
			GND					B11									
			GND					AN5									
			GND					AN26									
			GND					AN20									
			GND					AN17									
			GND					AN11									
			GND					AK5									
			GND					AK26									
			GND					AK20									
			GND					AK17									
			GND					AK11									
			GND					AG5									
			GND					AG26									
			GND					AG20									
			GND					AG17									
			GND					AG11									
			GND					AE10									
			GND					AD5									
			GND					AD23									
			GND					AD2									
			GND					AD14									
			GND					AB21									
			GND					AB17									
			GND					AB13									
			GND					AA25									
			GND					AA2									
			GND					AA11									
			GND					B14									
			GND					AN8									
			GND					AN29									
			GND					AN23									
			GND					AN2									
			GND					AN14									
			GND					AN2									
			GND					AK29									
			GND					AK23									



Bank number	IO Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note 3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)
			GND				AG7										
			GND				AK14										
			GND				AG8										
			GND				AG09										
			GND				AG23										
			GND				AG2										
			GND				AG14										
			GND				AF9										
			GND				AD8										
			GND				AD26										
			GND				AD20										
			GND				AD17										
			GND				AB23										
			GND				AB19										
			GND				AB15										
			GND				AA5										
			GND				AA20										
			GND				AA14										
			GND				AA8										
			GND				AA22										
			GND				AA16										
			GND				AA18										
			VCC				V18	P15									
			VCC				V24	W20									
			VCC				V22	W18									
			VCC				V20	W16									
			VCC				V18	W14									
			VCC				V16	W9									
			VCC				V14	V21									
			VCC				W23	V19									
			VCC				W21	V17									
			VCC				W19	V15									
			VCC				W17	V13									
			VCC				W15	V11									
			VCC				W13	U20									
			VCC				V24	U18									
			VCC				V22	U16									
			VCC				V20	U14									
			VCC				V18	U12									
			VCC				V14	U10									
			VCC				U21	T9									
			VCC				U19	T19									
			VCC				U15	T17									
			VCC				U13	T15									
			VCC				T24	T13									
			VCC				T22	T11									
			VCC				T20	R18									
			VCC				T18	R16									
			VCC				T16	R14									
			VCC				T14	R12									
			VCC				R23	R10									
			VCC				R21	P9									
			VCC				R19	P19									
			VCC				R17	P17									
			VCC				R15	P13									
			VCC				R13	P11									
			VCC				P24	N20									
			VCC				P22	N18									
			VCC				P20	N16									
			VCC				P18	N14									
			VCC				P16	N12									
			VCC				P14	N10									
			VCC				P12	M9									
			VCC				N23	M20									
			VCC				N21	M19									
			VCC				N17	M17									
			VCC				N15	M15									
			VCC				N13	M13									
			VCC				AC23	M11									
			VCC				AB24	L18									
			VCC				AB22	L16									
			VCC				AB20	L13									
			VCC				AB18	L12									
			VCC				AB16	L10									
			VCC				AB14	K17									
			VCC				AB12										
			VCC				AA23										
			VCC				AA21										
			VCC				AA19										
			VCC				AA17										
			VCC				AA15										
			VCC				AA13										
			DMU				PC5	H23									
			DMU				V17	R15									
			DMU				CA	F8									
			VCCBAT				L27	J24									
			VCCA_PLL_1				H25	G20									
			VCCA_PLL_2				D10	H9									
			VCCA_PLL_3				AF10	V8									
			VCCA_PLL_4				AG25	AB20									
			VCCA_PLL_5				T9	P8									
			VCCA_PLL_6				W9	P7									
			VCCD_PLL_1				J26	H21									
			VCCD_PLL_2				K9	G8									
			VCCD_PLL_3				AE9	AA7									
			VCCD_PLL_4				AF26	AA21									
			VCCD_PLL_5				U8	P7									
			VCCD_PLL_6				V8	R8									
			VCCIO3A				AM20	AG16									
			VCCIO3A				AK24	AD19									
			VCCIO3A				AL20	AD16									
			VCCIO3A				AH22										
			VCCIO3B				AF22										
			VCCIO3B				AF21										
			VCCIO3C				AD25	AC20									
			VCCIO4A				AM14	AG7									



Bank number	IO Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note 3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)
			VCCIO4A					AH11	AG13								
			VCCIO4A					AL17	AG10								
			VCCIO4A					AJ17	AD13								
			VCCIO4B					AJ14	AD10								
			VCCIO4B					AH11									
			VCCIO4B					AJB									
			VCCIO5A					AD3	I2								
			VCCIO5A					AD3	I2								
			VCCIO5A					AA6	R2								
			VCCIO5B					AK3	AE2								
			VCCIO5B					AJB									
			VCCIO5B					AH6									
			VCCIO6A					I6	K2								
			VCCIO6A					I3	G2								
			VCCIO6A					P3	D2								
			VCCIO6A					L3									
			VCCIO6B					I6									
			VCCIO6B					HE									
			VCCIO7A					F14	B7								
			VCCIO7A					F11	B4								
			VCCIO7A					C14	B13								
			VCCIO7A					C11	B10								
			VCCIO7B					D8									
			VCCIO7B					G8									
			VCCIO8A					P22	F18								
			VCCIO8A					P20	E18								
			VCCIO8A					C23	C20								
			VCCIO8A					C20	B18								
			VCCIO8A					C17									
			VCCIO8B					J23									
			VCCIO8B					H22									
			VCCIO8C					H26	G20								
			VCCPD3A					AC20	AB18								
			VCCPD3A					AC19	AA18								
			VCCPD3B					AC21									
			VCCPD3C					AC24	Y21								
			VCCPD4A					AD16	AA13								
			VCCPD4A					AC18	AA12								
			VCCPD4B					AC13									
			VCCPD5A					Y12	U8								
			VCCPD5A					AA22	U7								
			VCCPD5B					AC12									
			VCCPD6A					T12	M8								
			VCCPD6A					R12	M7								
			VCCPD6B					M11									
			VCCPD7A					M15	J13								
			VCCPD7A					M14	H13								
			VCCPD7B					L12									
			VCCPD8A					M19	H16								
			VCCPD8A					L19	G16								
			VCCPD8B					M23									
			VCCPD8C					M24	G21								
3A		VREFB3AND	VREFB3AND	VREFB3AND				AE20	Y17								
3B		VREFB3BND	VREFB3BND	VREFB3BND				AE22									
4A		VREFB4AND	VREFB4AND	VREFB4AND				AD15	AB12								
4B		VREFB4BND	VREFB4BND	VREFB4BND				AD13									
5A		VREFB5AND	VREFB5AND	VREFB5AND				AD11	W7								
5B		VREFB5BND	VREFB5BND	VREFB5BND				AD11									
6A		VREFB6AND	VREFB6AND	VREFB6AND				N11	L9								
6B		VREFB6BND	VREFB6BND	VREFB6BND				M12									
7A		VREFB7AND	VREFB7AND	VREFB7AND				L9	H12								
7B		VREFB7BND	VREFB7BND	VREFB7BND				K13									
8A		VREFB8AND	VREFB8AND	VREFB8AND				K19	H18								
8B		VREFB8BND	VREFB8BND	VREFB8BND				M23									
		NC						AL30	AF21								
		NC						AM30	AF22								
		VCCL_GXB						W25	R22								
		VCCL_GXB						V28	P23								
		VCCL_GXB						V26	P21								
		VCCL_GXB						U27	N24								
		VCCL_GXB						U25	N22								
		VCCL_GXB						T28	M23								
		VCCL_GXB						T26	T23								
		VCCL_GXB						R27	T21								
		VCCL_GXB						R25	R24								
		VCCL_GXB						T28									
		VCCL_GXB						V28									
		VCCL_GXB						W27									
		VCCCB						U23	Y18								
		VCCCB						U12	N7								
		VCCCB						L18	J15								
		VCCCB						AD18	P28								
		RREF0						AP31	AH21								
		RREF1						A29	A22								
		VCCA						U24	R20								
		VCCA						R24	M21								
		VCCA						AA24	U21								
		VCCA						W24									
		VCCD_GXB						P27	U23								
		VCCD_GXB						N28	U22								
		VCCD_GXB						AB28	M22								
		VCCD_GXB						AK27	L22								

- Notes:
- (1) An IO module is a group of 16 IO pins.
  - (2) When not used as DIFFIN or DIFFIO\_TX, all pins marked with \* (DIFFIN\_#/#pin) can be configured as emulated LVDS output channels (DIFFOUT). Only DIFFIN pins of the same index group (e.g DIFFIN\_B1p and DIFFIN\_B1n) can be used to form an emulated LVDS output channel.
  - (3) When not used as clocks, the CQn and DQSn pins can be used as DQ pins.



Pin Name	Pin Type (1st and 2nd Function)	Pin Description
<b>Clock and PLL Pins</b>		
CLK[4:15]	Clock, Input	Single ended clock input pin.
DIFFCLK[0:5]p	Clock, Input	Clock input pin for differential clock input. OCT Rd is not supported.
DIFFCLK[0:5]n	Clock, Input	Negative clock input for differential clock input. OCT Rd is not supported.
PLL_[1:4]_CLKOUT1p	I/O, Clock	PLL[1:4]_CLKOUT1 (except PLL1 and PLL3 in EP2AGX125 and EP2AGX260) supports 2 clock I/O pins, configured either as one single ended I/O or one differential I/O pair. PLL1 and PLL3 in EP2AGX125 and EP2AGX260 support 6 clock I/O pins, configured either as 3 single ended I/Os or 3 differential I/O pairs.
PLL_[1:4]_CLKOUT1n	I/O, Clock	
PLL_[1:3]_CLKOUT[2:3]p (Note 4)	I/O, Clock	PLL1 and PLL3 in EP2AGX125 and EP2AGX260 support 6 clock I/O pins, configured either as 3 single ended I/Os or 3 differential I/O pairs.
PLL_[1:3]_CLKOUT[2:3]n (Note 4)	I/O, Clock	
<b>Dedicated Configuration/JTAG Pins</b>		
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (nCSO, ASDO, DATA[7:0], CLKUSR, INIT_DONE, DEV_OE, DEV_CLRn) are on or off before and during configuration. A logic high (1.5V, 1.8V, 2.5V, 3.0V or 3V) turns off the weak pull-up, while a logic low turns them on.
MSEL[0:3]	Input	Configuration input pins that set the FPGA device configuration scheme.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user-mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration done pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin.
nCEO	I/O, Output (open-drain)	Output that drives low when device configuration is complete. This pin can be used as a regular I/O if not used for device configuration.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as a user I/O pin.
TCK	Input	Dedicated JTAG test clock input pin.
TMS	Input	Dedicated JTAG test mode select input pin.
TDI	Input	Dedicated JTAG test data input pin.
TDO	Output	Dedicated JTAG test data output pin.
<b>Optional/Dual-Purpose Configuration Pins</b>		
nCSO	Output	Dedicated output control signal from the FPGA to the serial configuration device in AS mode that enables the configuration device.
ASDO	Output	Control signal from the FPGA to the serial configuration device in AS mode used to read out configuration data.
DCLK	I/O (PS, FPP) Output (AS)	Dedicated configuration clock pin. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into the FPGA. In AS mode, DCLK is an output from the FPGA that provides timing for the configuration interface.
CRC_ERROR	I/O, Output (open-drain)	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled. This pin can be used as regular I/O if not used for CRC error detection.
DEV_CLRn	I/O, Input	Optional pin that allows designers to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed.
DEV_OE	I/O, Input	Optional pin that allows designers to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
DATA0	Input	DATA[0] is a dedicated pin that is used for both the passive and active configuration modes.
DATA[1:7]	I/O, Input	Dual-purpose configuration input data pins. The DATA[0:7] pins can be used for byte-wide configuration. DATA[1:7] pins can also be used as user I/O pins after configuration, but not DATA0.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin.
<b>Differential I/O Pins</b>		
DIFFIO_RX_[T,B,R][##]p, DIFFIO_RX_[T,B,R][##]n	I/O, RX channel	These are true LVDS receiver channels with OCT Rd support. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX_[T,B,R][##]p, DIFFIO_TX_[T,B,R][##]n	I/O, TX channel	These are true LVDS transmitter channels. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used as true LVDS transmitter channels, these pins can be configured as true LVDS receiver channels without OCT Rd support (DIFFIN_[T,B,R][##]p,n). If not used for differential signaling, these pins are available as user I/O pins.
DIFFIN_[T,B,R][##]p, DIFFIN_[T,B,R][##]n	I/O, RX channel	These are true LVDS receiver channels without OCT Rd support. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used as true LVDS receiver channels without OCT Rd support, these pins can be configured as true LVDS transmitter channels (DIFFIO_TX_[T,B,R][##]p,n). If not used for differential signaling, these pins are available as user I/O pins.
DIFFFOUT_[##]p, DIFFFOUT_[##]n	I/O, TX channel	These are emulated LVDS output channels. On I/O banks, there are true LVDS input buffers but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, (DIFFIO_RX_[T,B,R][##]p,n), DIFFIN_[T,B,R][##]p,n) can be configured as emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
<b>External Memory Interface Pins</b>		
DQS[##][T,B,R]	I/O, DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.
DQSn[##][T,B,R] (Note 5)	I/O, DQSn	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.
DQ[##][T,B,R]	I/O, DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
CQ[##][T,B,R]	DQS	Optional data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.
CQn[##][T,B,R] (Note 5)	DQS	Optional complementary data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.
<b>Reference Pins</b>		
RUP[0:2]	I/O, Input	Reference pins for I/O banks. The RUP pins share the same VCCIO with the I/O bank where they are located. The external precision resistor RUP must be connected to the designated RUP pin within the bank. If not required, this pin is a regular I/O pin.
RDN[0:2]	I/O, Input	Reference pins for I/O banks. The RDN pins share the same GND with the I/O bank where they are located. The external precision resistor RDN must be connected to the designated RDN pin within the bank. If not required, this pin is a regular I/O pin.
DNU	No Connect	Do Not Use (DNU).
NC	No Connect	Do not drive signals into these pins.
<b>Supply Pins</b>		
VCC	Power	VCC supplies power to the core and periphery.
VCCD_PLL_[1:6]	Power	Digital power for PLL[1:6]. All of these pins must be connected even if the PLL is not used.
VCCCB	Power	Configuration RAM bits power supply.
VCCA_PLL_[1:6]	Power	Analog power for PLL [1:6]. All of these pins must be connected even if the PLL is not used.
VCCIO[3:8][A,B]	Power	These are I/O supply voltage pins for banks 3 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all LVDS, LVCMOS(1.2V, 1.5V, 1.8V, 2.5V, 3.0V, 3.3V), HSTL(12,15,18), SSTL(15,18,2), 3.0V PCI/PCI-X I/O as well as LVTTTL (1.8V, 2.5V, 3.0V, 3.3V) I/O standards. VCCIO also supplies power to the input buffers used for LVCMOS(1.2V, 1.5V, 1.8V, 2.5V, 3.0V, 3.3V), 3.0V PCI/PCI-X and LVTTTL (1.8V, 2.5V, 3.0V, 3.3V) I/O standards.
VCCIO[3:8]C	Power	These are configuration and JTAG supply voltage pins for banks 3C and 8C. Each bank can support a different voltage level. For AS/PFP configuration schemes, VCCIO[3:8]C supports 1.8V, 2.5V, 3.0V or 3.3V. JTAG can support 1.5V, 1.8V, 2.5V, 3.0V or 3.3V.
VCCPD[3:8][A,B], VCCPD[3:8]C	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers and the input buffers for HSTL/SSTL input buffers. This can be connected to 3.3V, 3.0V or 2.5V. For 3.3V I/O standard connect VCCPD to 3.3V, for 3.0V I/O standard connect VCCPD to 3.0V and for 2.5V/1.8V/1.2V I/O standards connect VCCPD to 2.5V.
VCCBAT	Power	Battery back-up power supply for design security volatile key register.
GND	Ground	Device ground pins.
VREF[3:8][A,B]n0	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. These pins cannot be used as regular I/Os.
<b>Transceiver Pins</b>		
VCCL_GXB	Power	Supplies power to the transceiver PMA TX, PMA RX and clocking.
VCCH_GXB	Power	Supplies power to the transceiver PMA output (TX) buffer.
VCCA	Power	Supplies power to the transceiver PMA regulator.



Pin Name	Pin Type (1st and 2nd Function)	Pin Description
GXB_RX[0:15]p (Note 6)	Input	High speed positive differential receiver channels.
GXB_RX[0:15]n (Note 6)	Input	High speed negative differential receiver channels.
GXB_TX[0:15]p (Note 6)	Output	High speed positive differential transmitter channels.
GXB_TX[0:15]n (Note 6)	Output	High speed negative differential transmitter channels.
REFCLK[0:7]p	Input	High speed differential reference clock positive.
REFCLK[0:7]n	Input	High speed differential reference clock complement.
RREF[0:1]	Input	Reference resistor for transceiver.

**Notes:**

1. Refer to the Arria II GX Device Datasheet and Pin Connection Guidelines for the recommended operating conditions.
2. This pin definition is prepared based on the EP2AGX260.
3. Some of the pull-up/pull down resistors mentioned in the table above may not be required, depending on the exact device configuration scheme.  
The ability to NC or short them may be valuable during the debug phase, should you be required to use a different configuration scheme.  
Refer to the Configuring Arria II GX Devices chapter in the Arria II GX Device Handbook for more information.
4. PLL[1:3]\_CLKOUT[2..3]p,n are only available in PLL1 and PLL3 in EP2AGX125 and EP2AGX260.
5. When not used as clocks, the Q0n and Q0Sn pins can be used as DQ pin.
6. Transceiver signals GXB\_RX[15..0] and GXB\_TX[15..0] are device specific.

PLL_1	8C	8B VREFB8BN0	8A VREFB8AN0	7A VREFB7AN0	7B VREFB7BN0	PLL_2
Transceiver Block (QL3)						6B VREFB6BN0
Transceiver Block (QL2)						6A VREFB6AN0
Transceiver Block (QL1)						PLL_5
Transceiver Block (QL0)						PLL_6
PLL_4	3C	3B VREFB3BN0	3A VREFB3AN0	4A VREFB4CN0	4B VREFB4BN0	PLL_3
						5A VREFB5AN0
						5B VREFB5BN0

This is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only.



**Pin Information for the Arria<sup>®</sup> II GX EP2AGX190 Device  
Version 1.1**

<b>Version Number</b>	<b>Date</b>	<b>Changes Made</b>
1.0	2/27/2009	Initial release.
1.1	5/29/2009	Added DNU in Pin List and Pin Definitions.