



Bank number	IO Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)
Q13			GXB_TX15n					B31									
Q13			GXB_RX15n					C34									
Q13			GXB_RX15p					G33									
Q13			GXB_TX14n					D32									
Q13			GXB_TX14p					D31									
Q13			GXB_RX14n					E34									
Q13			GXB_RX14p					E33									
Q13			REFCLK7n					L30									
Q13			REFCLK7p					L29									
Q13			REFCLK3n					N30									
Q13			REFCLK3p					N29									
Q13			GXB_TX13n					P32									
Q13			GXB_TX13p					P31									
Q13			GXB_RX13n					G34									
Q13			GXB_RX13p					G33									
Q13			GXB_TX12n					H32									
Q13			GXB_TX12p					H31									
Q13			GXB_RX12n					J34									
Q13			GXB_RX12p					J33									
Q12			GXB_TX11n					K32	G23								
Q12			GXB_TX11p					K31	D23								
Q12			GXB_RX11n					L34	A24								
Q12			GXB_RX11p					L33	B24								
Q12			GXB_TX10n					M32	A26								
Q12			GXB_TX10p					M31	B26								
Q12			GXB_RX10n					N34	C28								
Q12			GXB_RX10p					N33	C27								
Q12			REFCLK6n					P30	D26								
Q12			REFCLK6p					P29	D25								
Q12			REFCLK2n					U30	E28								
Q12			REFCLK2p					U29	E27								
Q12			GXB_TX8n					V32	F28								
Q12			GXB_TX8p					V31	F25								
Q12			GXB_RX8n					W34	G28								
Q12			GXB_RX8p					W33	G27								
Q12			GXB_TX8n					T32	H26								
Q12			GXB_TX8p					T31	H25								
Q12			GXB_RX8n					U34	I28								
Q12			GXB_RX8p					U33	I27								
Q11			GXB_TX7n					V32	K26								
Q11			GXB_TX7p					V31	K25								
Q11			GXB_RX7n					W34	L28								
Q11			GXB_RX7p					W33	L27								
Q11			GXB_TX6n					Y32	M26								
Q11			GXB_TX6p					Y31	M25								
Q11			GXB_RX6n					AA34	N28								
Q11			GXB_RX6p					AA33	N27								
Q11			REFCLK5n					W30	P26								
Q11			REFCLK5p					W29	P25								
Q11			REFCLK1n					AA38	R28								
Q11			REFCLK1p					AA29	R27								
Q11			GXB_TX5n					AB32	T26								
Q11			GXB_TX5p					AB31	T25								
Q11			GXB_RX5n					AC34	U28								
Q11			GXB_RX5p					AC33	U27								
Q11			GXB_TX4n					AD32	V26								
Q11			GXB_TX4p					AD31	V25								
Q11			GXB_RX4n					AE34	W28								
Q11			GXB_RX4p					AE33	W27								
Q10			GXB_TX3n					AF32	Y26								
Q10			GXB_TX3p					AF31	Y25								
Q10			GXB_RX3n					AG34	AA28								
Q10			GXB_RX3p					AG33	AA27								
Q10			GXB_TX2n					AH32	AB26								
Q10			GXB_TX2p					AH31	AB25								
Q10			GXB_RX2n					AI34	AC28								
Q10			GXB_RX2p					AI33	AC27								
Q10			REFCLK4n					AC30	AD26								
Q10			REFCLK4p					AC29	AD25								
Q10			REFCLK0n					AE30	AE28								
Q10			REFCLK0p					AE29	AE27								
Q10			GXB_TX1n					AK32	AH27								
Q10			GXB_TX1p					AK31	AG27								
Q10			GXB_RX1n					AL34	AH25								
Q10			GXB_RX1p					AL33	AG25								
Q10			GXB_TX0n					AM32	AF24								
Q10			GXB_TX0p					AM31	AE24								
Q10			GXB_RX0n					AN38	AH23								
Q10			GXB_RX0p					AN33	AG23								
3C			ICONFIG		ICONFIG			AC26	AA24								
3C			CONF_DONE		CONF_DONE			AE25	AA23								
3C			MSEL3		MSEL3			AB26	AB24								
3C			MSEL2		MSEL2			AD24	Y24								
3C			MSEL1		MSEL1			AC25	Y23								
3C			MSEL0		MSEL0			AE27	W24								
3C			HSTATUS		HSTATUS			AD28	W23								
3C			HI0_PULLUP		HI0_PULLUP			AC28	AE22								
3C			HI1_PULLUP		HI1_PULLUP			AE25	AA22								
3B	BIO1	VREFB3BNO	IO					AH26	DQ24B					DQ12B			DQ6B
3B	BIO1	VREFB3BNO	IO					AG24	DQ24B					DQ12B			DQ6B
3B	BIO1	VREFB3BNO	IO					AG27	DQ24B					DQ12B			DQ6B
3B	BIO1	VREFB3BNO	IO					AF25									
3B	BIO1	VREFB3BNO	IO					AD22					DQ5n24B				DQ6B
3B	BIO1	VREFB3BNO	IO					AD21									DQ6B
3B	BIO1	VREFB3BNO	IO					AC22					DQ5n24B				DQ6B
3B	BIO1	VREFB3BNO	IO					AE28									DQ6B
3B	BIO1	VREFB3BNO	IO					AD28					DQ5n23B				DQ6B
3B	BIO1	VREFB3BNO	IO					AE27					DQ23B				DQ6B
3B	BIO1	VREFB3BNO	IO					AH28					DQ5n23B				DQ6B
3B	BIO1	VREFB3BNO	IO					AE28					DQ5n23B				DQ6B
3B	BIO1	VREFB3BNO	IO					AF24					DQ23B				DQ6B
3B	BIO1	VREFB3BNO	IO					AG28					DQ23B				DQ6B
3B	BIO1	VREFB3BNO	IO					AE24					DQ23B				DQ6B
3B	BIO1	VREFB3BNO	IO					AF28					DQ23B				DQ6B
3B	BIO1	VREFB3BNO	IO					AE28					DQ23B				DQ6B
3B	BIO2	VREFB3BNO	IO					AI29					DQ22B				DQ6B



Bank number	I/O Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)
3B	BI02	VREFB3N0	IO			DIFFIO_RX_B55	DIFFIO_RX_B55	AE23		DQ22B	DQ22B	DQ22B	DQ22B				
3B	BI02	VREFB3N0	IO			DIFFIO_TX_B55	DIFFIO_TX_B55	AJ28		DQ22B	DQ22B	DQ22B	DQ22B				
3B	BI02	VREFB3N0	IO			DIFFIO_RX_B56	DIFFIO_RX_B56	AE23		DQ22B	DQ22B	DQ22B	DQ22B				
3B	BI02	VREFB3N0	IO			DIFFIO_TX_B56	DIFFIO_TX_B56	AE23		DQ22B	DQ22B	DQ22B	DQ22B				
3B	BI02	VREFB3N0	IO			DIFFIO_RX_B57	DIFFIO_RX_B57	AE23		DQ22B	DQ22B	DQ22B	DQ22B				
3B	BI02	VREFB3N0	IO			DIFFIO_TX_B57	DIFFIO_TX_B57	AE23		DQ22B	DQ22B	DQ22B	DQ22B				
3B	BI02	VREFB3N0	IO			DIFFIO_RX_B76	DIFFIO_RX_B76	AE23		DQ22B	DQ22B	DQ22B	DQ22B				
3B	BI02	VREFB3N0	IO			DIFFIO_TX_B76	DIFFIO_TX_B76	AE23		DQ22B	DQ22B	DQ22B	DQ22B				
3B	BI02	VREFB3N0	IO			DIFFIO_RX_B77	DIFFIO_RX_B77	AE23		DQ22B	DQ22B	DQ22B	DQ22B				
3B	BI02	VREFB3N0	IO			DIFFIO_TX_B77	DIFFIO_TX_B77	AE23		DQ22B	DQ22B	DQ22B	DQ22B				
3B	BI02	VREFB3N0	IO			DIFFIO_RX_B86	DIFFIO_RX_B86	AE23		DQ22B	DQ22B	DQ22B	DQ22B				
3B	BI02	VREFB3N0	IO			DIFFIO_TX_B86	DIFFIO_TX_B86	AE23		DQ22B	DQ22B	DQ22B	DQ22B				
3B	BI02	VREFB3N0	IO			DIFFIO_RX_B87	DIFFIO_RX_B87	AE23		DQ22B	DQ22B	DQ22B	DQ22B				
3B	BI02	VREFB3N0	IO			DIFFIO_TX_B87	DIFFIO_TX_B87	AE23		DQ22B	DQ22B	DQ22B	DQ22B				
3A	VREFB3N0	IO		PLL4_CLKOUT1n				AH25	U24								
3A	VREFB3N0	IO		PLL4_CLKOUT1p				AE27	AB19								
3A	VREFB3N0	IO		RUP0				AH24	V24								
3A	BI03	VREFB3N0	IO			DIFFIO_RX_B9n	DIFFIO_RX_B9n	AM29		DQ20B	DQ20B	DQ20B	DQ20B				
3A	BI03	VREFB3N0	IO			DIFFIO_TX_B9n	DIFFIO_TX_B9n	AM28		DQ20B	DQ20B	DQ20B	DQ20B				
3A	BI03	VREFB3N0	IO			DIFFIO_RX_B9p	DIFFIO_RX_B9p	AL29		DQ20B	DQ20B	DQ20B	DQ20B				
3A	BI03	VREFB3N0	IO			DIFFIO_TX_B9p	DIFFIO_TX_B9p	AM27		DQ20B	DQ20B	DQ20B	DQ20B				
3A	BI03	VREFB3N0	IO			DIFFIO_RX_B10n	DIFFIO_RX_B10n	AJ25		DQ20n20B	DQ20B	DQ20B	DQ20B				
3A	BI03	VREFB3N0	IO			DIFFIO_TX_B10n	DIFFIO_TX_B10n	AN28		DQ20B	DQ20B	DQ20B	DQ20B				
3A	BI03	VREFB3N0	IO			DIFFIO_RX_B10p	DIFFIO_RX_B10p	AJ24		DQ20B	DQ20B	DQ20B	DQ20B				
3A	BI03	VREFB3N0	IO			DIFFIO_TX_B10p	DIFFIO_TX_B10p	AN27		DQ20B	DQ20B	DQ20B	DQ20B				
3A	BI03	VREFB3N0	IO			DIFFIO_RX_B11n	DIFFIO_RX_B11n	AM26		DQ20n19B	DQ20n10B/DQ10B	DQ20B	DQ20B				
3A	BI03	VREFB3N0	IO			DIFFIO_TX_B11n	DIFFIO_TX_B11n	AM28		DQ20B	DQ20B	DQ20B	DQ20B				
3A	BI03	VREFB3N0	IO			DIFFIO_RX_B11p	DIFFIO_RX_B11p	AM25		DQ20n19B	DQ20B	DQ20B	DQ20B				
3A	BI03	VREFB3N0	IO			DIFFIO_TX_B11p	DIFFIO_TX_B11p	AJ22		DQ20B	DQ20B	DQ20B	DQ20B				
3A	BI03	VREFB3N0	IO			DIFFIO_RX_B12n	DIFFIO_RX_B12n	AE24		DQ19B	DQ19B	DQ19B	DQ19B				
3A	BI03	VREFB3N0	IO			DIFFIO_TX_B12n	DIFFIO_TX_B12n	AE23		DQ19B	DQ19B	DQ19B	DQ19B				
3A	BI03	VREFB3N0	IO			DIFFIO_RX_B12p	DIFFIO_RX_B12p	AF20		DQ19B	DQ19B	DQ19B	DQ19B				
3A	BI03	VREFB3N0	IO			DIFFIO_TX_B12p	DIFFIO_TX_B12p	AF28		DQ19B	DQ19B	DQ19B	DQ19B				
3A	BI04	VREFB3N0	IO			DIFFIO_RX_B13n	DIFFIO_RX_B13n	AM29	AD21	DQ18B	DQ18B	DQ18B	DQ18B			DQ14B	DO7B
3A	BI04	VREFB3N0	IO			DIFFIO_TX_B13n	DIFFIO_TX_B13n	AM23	AC17	DQ18B	DQ18B	DQ18B	DQ18B			DQ14B	DO7B
3A	BI04	VREFB3N0	IO		INIT_DONE	DIFFIO_RX_B13p	DIFFIO_RX_B13p	AL24	AC21	DQ18B	DQ18B	DQ18B	DQ18B			DQ14B	DO7B
3A	BI04	VREFB3N0	IO			DIFFIO_TX_B13p	DIFFIO_TX_B13p	AL23	AB17	DQ18B	DQ18B	DQ18B	DQ18B			DQ14B	DO7B
3A	BI04	VREFB3N0	IO			DIFFIO_RX_B14n	DIFFIO_RX_B14n	AH21	Y22	DQ20n18B	DQ20B	DQ20B	DQ20B			DQ20n14B	DO7B
3A	BI04	VREFB3N0	IO			DIFFIO_TX_B14n	DIFFIO_TX_B14n	AP27	AC16	DQ18B	DQ18B	DQ18B	DQ18B			DQ14B	DO7B
3A	BI04	VREFB3N0	IO			DIFFIO_RX_B14p	DIFFIO_RX_B14p	AE22	Y21	DQ20n18B	DQ20B	DQ20B	DQ20B			DQ20n14B	DO7B
3A	BI04	VREFB3N0	IO			DIFFIO_TX_B14p	DIFFIO_TX_B14p	AP26	AB16	DQ18B	DQ18B	DQ18B	DQ18B			DQ14B	DO7B
3A	BI04	VREFB3N0	IO			DIFFIO_RX_B15n	DIFFIO_RX_B15n	AP24	AD23	DQ20n17B	DQ20n19B/DQ20B	DQ20n19B/DQ20B	DQ20B			DQ20n13B	DQ20n7B/DO7B
3A	BI04	VREFB3N0	IO			DIFFIO_TX_B15n	DIFFIO_TX_B15n	AP28	AD24	DQ18B	DQ18B	DQ18B	DQ18B			DQ14B	DO7B
3A	BI04	VREFB3N0	IO			DIFFIO_RX_B15p	DIFFIO_RX_B15p	AN24	AD22	DQ20n17B	DQ20n19B/DQ20B	DQ20n19B/DQ20B	DQ20B			DQ20n13B	DQ20n7B/DO7B
3A	BI04	VREFB3N0	IO			DIFFIO_TX_B15p	DIFFIO_TX_B15p	AN25	AC18	DQ18B	DQ18B	DQ18B	DQ18B			DQ14B	DO7B
3A	BI04	VREFB3N0	IO			DIFFIO_RX_B16n	DIFFIO_RX_B16n	AE19		DQ17B	DQ17B	DQ17B	DQ17B			DQ13B	DO7B
3A	BI04	VREFB3N0	IO			DIFFIO_TX_B16n	DIFFIO_TX_B16n	AJ23	AC23	DQ17B	DQ17B	DQ17B	DQ17B			DQ13B	DO7B
3A	BI04	VREFB3N0	IO			DIFFIO_RX_B16p	DIFFIO_RX_B16p	AD19	Y19	DQ17B	DQ17B	DQ17B	DQ17B			DQ13B	DO7B
3A	BI04	VREFB3N0	IO			DIFFIO_TX_B16p	DIFFIO_TX_B16p	AM23	AC22	DQ17B	DQ17B	DQ17B	DQ17B			DQ13B	DO7B
3A	BI05	VREFB3N0	IO			DIFFIO_RX_B17n	DIFFIO_RX_B17n	AL25	AD24	DQ16B	DQ16B	DQ16B	DQ16B			DQ12B	DO3B
3A	BI05	VREFB3N0	IO			DIFFIO_TX_B17n	DIFFIO_TX_B17n	AM22	AE22	DQ16B	DQ16B	DQ16B	DQ16B			DQ12B	DO3B
3A	BI05	VREFB3N0	IO			DIFFIO_RX_B17p	DIFFIO_RX_B17p	AK28	AC24	DQ16B	DQ16B	DQ16B	DQ16B			DQ12B	DO3B
3A	BI05	VREFB3N0	IO			DIFFIO_TX_B17p	DIFFIO_TX_B17p	AL22	AE21	DQ16B	DQ16B	DQ16B	DQ16B			DQ12B	DO3B
3A	BI05	VREFB3N0	IO			DIFFIO_RX_B18n	DIFFIO_RX_B18n	AJ21	Y23	DQ20n16B	DQ20B	DQ20B	DQ20B			DQ20n12B	DO3B
3A	BI05	VREFB3N0	IO			DIFFIO_TX_B18n	DIFFIO_TX_B18n	AL21	AF20	DQ16B	DQ16B	DQ16B	DQ16B			DQ12B	DO3B
3A	BI05	VREFB3N0	IO			DIFFIO_RX_B18p	DIFFIO_RX_B18p	AM20	Y22	DQ20n16B	DQ20B	DQ20B	DQ20B			DQ20n12B	DO3B
3A	BI05	VREFB3N0	IO			DIFFIO_TX_B18p	DIFFIO_TX_B18p	AK21	AE20	DQ16B	DQ16B	DQ16B	DQ16B			DQ12B	DO3B
3A	BI05	VREFB3N0	IO			DIFFIO_RX_B19n	DIFFIO_RX_B19n	AP22	AF18	DQ20n15B	DQ20n19B/DQ20B	DQ20n19B/DQ20B	DQ20B			DQ20n11B	DQ20n6B/DO6B
3A	BI05	VREFB3N0	IO			DIFFIO_TX_B19n	DIFFIO_TX_B19n	AP23	AF19	DQ16B	DQ16B	DQ16B	DQ16B			DQ12B	DO3B
3A	BI05	VREFB3N0	IO			DIFFIO_RX_B19p	DIFFIO_RX_B19p	AP21	AE18	DQ20n15B	DQ20n19B/DQ20B	DQ20n19B/DQ20B	DQ20B			DQ20n11B	DQ20n6B/DO6B
3A	BI05	VREFB3N0	IO			DIFFIO_TX_B19p	DIFFIO_TX_B19p	AN22	AE19	DQ16B	DQ16B	DQ16B	DQ16B			DQ12B	DO3B
3A	BI05	VREFB3N0	IO			DIFFIO_RX_B20n	DIFFIO_RX_B20n	AG19	AE16	DQ15B	DQ15B	DQ15B	DQ15B			DQ11B	DO6B
3A	BI05	VREFB3N0	IO			DIFFIO_TX_B20n	DIFFIO_TX_B20n	AL20	AF17	DQ15B	DQ15B	DQ15B	DQ15B			DQ11B	DO6B
3A	BI05	VREFB3N0	IO			DIFFIO_RX_B21n	DIFFIO_RX_B21n	AF18	Y16	DQ15B	DQ15B	DQ15B	DQ15B			DQ11B	DO6B
3A	BI05	VREFB3N0	IO			DIFFIO_TX_B21n	DIFFIO_TX_B21n	AN18	AE17	DQ15B	DQ15B	DQ15B	DQ15B			DQ11B	DO6B
3A	BI06	VREFB3N0	IO			DIFFIO_RX_B21p	DIFFIO_RX_B21p	AN21	AD15	DQ14B	DQ14B	DQ14B	DQ14B			DQ10B	DO5B
3A	BI06	VREFB3N0	IO			DIFFIO_TX_B21p	DIFFIO_TX_B21p	AP20	AF16	DQ14B	DQ14B	DQ14B	DQ14B			DQ10B	DO5B
3A	BI06	VREFB3N0	IO			DIFFIO_RX_B22n	DIFFIO_RX_B22n	AK21	AE15	DQ14B	DQ14B	DQ14B	DQ14B			DQ10B	DO5B
3A	BI06	VREFB3N0	IO			DIFFIO_TX_B22n	DIFFIO_TX_B22n	AF19	AE16	DQ14B	DQ14B	DQ14B	DQ14B			DQ10B	DO5B
3A	BI06	VREFB3N0	IO			DIFFIO_RX_B22p	DIFFIO_RX_B22p	AM19	AG19	DQ20n14B	DQ20B	DQ20B	DQ20B			DQ20n10B	DO5B
3A	BI06	VREFB3N0	IO			DIFFIO_TX_B22p	DIFFIO_TX_B22p	AN19	AH19	DQ14B	DQ14B	DQ14B	DQ14B			DQ10B	DO5B
3A	BI06	VREFB3N0	IO			DIFFIO_RX_B23n	DIFFIO_RX_B23n	AM18	AH17	DQ20n13B	DQ20n19B/DO7B	DQ20n19B/DO7B	DQ20B			DQ20n9B	DQ20n6B/DO6B
3A	BI06	VREFB3N0	IO			DIFFIO_TX_B23n	DIFFIO_TX_B23n	AP18	AH18	DQ13B	DQ13B	DQ13B	DQ13B			DQ9B	DO3B
3A	BI06	VREFB3N0	IO			DIFFIO_RX_B23p	DIFFIO_RX_B23p	AL18	AH16	DQ20n13B	DQ20n19B/DO7B	DQ20n19B/DO7B	DQ20B			DQ20n9B	DQ20n6B/DO6B
3A	BI06	VREFB3N0	IO			DIFFIO_TX_B23p	DIFFIO_TX_B23p	AM17	AH15	DQ13B	DQ13B	DQ13B	DQ13B			DQ9B	DO3B
3A	BI06	VREFB3N0	IO			DIFFIO_RX_B24n	DIFFIO_RX_B24n	AH18	AH15	DQ13B	DQ13B	DQ13B	DQ13B			DQ9B	DO3B
3A	BI06	VREFB3N0	IO			DIFFIO_TX_B24n	DIFFIO_TX_B24n	AG18	AE15	DQ13B	DQ13B	DQ13B	DQ13B			DQ9B	DO3B
3A	BI06	VREFB3N0	IO			DIFFIO_RX_B24p	DIFFIO_RX_B24p	AK18	AE14	DQ20n12B	DQ20n19B/DO7B	DQ20n19B/DO7B	DQ20B			DQ20n9B	DQ20n6B/DO6B
3A	BI06	VREFB3N0	IO			DIFFIO_TX_B24p	DIFFIO_TX_B24p	AG19	AE16	DQ13B	DQ13B	DQ13B	DQ13B			DQ9B	DO3B
3A	BI06	VREFB3N0	IO			DIFFIO_RX_B25n	DIFFIO_RX_B25n	AK19	AF15	DQ20n11B	DQ20n19B/DO7B	DQ20n19B/DO7B	DQ20B			DQ20n9B	DQ20n6B/DO6B
3A	BI06	VREFB3N0	IO			DIFFIO_TX_B25n	DIFFIO_TX_B25n	AG18	AE15	DQ13B	DQ13B	DQ13B	DQ13B			DQ9B	DO3B
3A	BI06	VREFB3N0	IO			DIFFIO_RX_B25p	DIFFIO_RX_B25p	AK17	AE14	DQ20n11B	DQ20n19B/DO7B	DQ20n19B/DO7B	DQ20B			DQ20n9B	DQ20n6B/DO6B
3A	BI06	VREFB3N0	IO			DIFFIO_TX_B25p	DIFFIO_TX_B25p	AH17	AH13	DQ12B	DQ12B	DQ12B	DQ12B			DQ8B	DO2B
3A	BI07	VREFB3N0	IO			DIFFIO_RX_B26n	DIFFIO_RX_B26n	AN16	AG12	DQ20n10B	DQ20n19B/DO7B	DQ20n19B/DO7B	DQ20B			DQ20n9B	DO1B
3A	BI07	VREFB3N0	IO														



Bank number	I/O Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with no OCT Rd (Note 2)	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)
4A	BIO8	VREFB4N0	IO			DFFIO_RX_B32b	DFFOUT_B32b	AE17	AE13								
4A	BIO8	VREFB4N0	IO			DFFIO_RX_B30a	DFFIN_B30a	AH16	AC13	DQSn10B	DQ2B	DQ3B	DQ1B	DQSn4B	DQ3B	DQ2B	DQ1B
4A	BIO8	VREFB4N0	IO			DFFIO_RX_B30b	DFFOUT_B30b	AN12	AF12	DQ10B	DQ2B	DQ3B	DQ1B	DQSn4B	DQ3B	DQ2B	DQ1B
4A	BIO8	VREFB4N0	IO			DFFIO_TX_B33b	DFFIN_B33b	AS18	AB13	DQSn10B	DQ2B	DQ3B	DQ1B	DQSn4B	DQ3B	DQ2B	DQ1B
4A	BIO8	VREFB4N0	IO			DFFIO_TX_B33c	DFFOUT_B33c	AM12	AE12								
4A	BIO8	VREFB4N0	IO			DFFIO_TX_B31a	DFFIN_B31a	AL15	AF10	DQSn9B	DQSn2B/DQ2B	DQ3B	DQSn1B/DQ1B	DQSn5B	DQSn3B/DQ3B	DQ2B	DQSn1B/DQ1B
4A	BIO8	VREFB4N0	IO			DFFIO_RX_B31b	DFFOUT_B31b	AP10	AF11	DQSn9B	DQ2B	DQ3B	DQ1B	DQSn5B	DQ3B	DQ2B	DQ1B
4A	BIO8	VREFB4N0	IO			DFFIO_TX_B33d	DFFIN_B33d	AM15	AE10	DQSn9B	DQ2B	DQ3B	DQ1B	DQSn5B	DQ3B	DQ2B	DQ1B
4A	BIO8	VREFB4N0	IO			DFFIO_RX_B31c	DFFOUT_B31c	AN10	AE11								
4A	BIO8	VREFB4N0	IO			DFFIO_TX_B32a	DFFIN_B32a	AH15	W13	DQSn8	DQ2B	DQ3B	DQ1B	DQSn5B	DQ3B	DQ2B	DQ1B
4A	BIO8	VREFB4N0	IO			DFFIO_RX_B32b	DFFOUT_B32b	AP9	AF8	DQSn8	DQ2B	DQ3B	DQ1B	DQSn5B	DQ3B	DQ2B	DQ1B
4A	BIO8	VREFB4N0	IO			DFFIO_TX_B32c	DFFIN_B32c	AE15	W12								
4A	BIO8	VREFB4N0	IO			DFFIO_RX_B32d	DFFOUT_B32d	AP9	AE9	DQSn8	DQ2B	DQ3B	DQ1B	DQSn5B	DQ3B	DQ2B	DQ1B
4A	BIO8	VREFB4N0	IO			DFFIO_TX_B33e	DFFIN_B33e	AF7	AF8	DQSn8	DQ2B	DQ3B	DQ1B	DQSn5B	DQ3B	DQ2B	DQ1B
4A	BIO9	VREFB4N0	IO			DFFIO_RX_B33a	DFFOUT_B33a	AL14	AF7	DQSn8	DQ4B	DQ2B	DQ1B	DQ4B	DQ2B	DQ1B	DQ1B
4A	BIO9	VREFB4N0	IO			DFFIO_TX_B33c	DFFIN_B33c	AN7	AE8	DQSn8	DQ4B	DQ2B	DQ1B	DQ4B	DQ2B	DQ1B	DQ1B
4A	BIO9	VREFB4N0	IO			DFFIO_RX_B34a	DFFOUT_B34a	AF16	Y12	DQSn8B	DQ4B	DQ2B	DQ1B	DQ4B	DQ2B	DQ1B	DQ1B
4A	BIO9	VREFB4N0	IO			DFFIO_TX_B34b	DFFOUT_B34b	AP6	AF6	DQSn8	DQ4B	DQ2B	DQ1B	DQ4B	DQ2B	DQ1B	DQ1B
4A	BIO9	VREFB4N0	IO			DFFIO_TX_B34c	DFFIN_B34c	AE16	W11	DQSn8B	DQ4B	DQ2B	DQ1B	DQ4B	DQ2B	DQ1B	DQ1B
4A	BIO9	VREFB4N0	IO			DFFIO_RX_B34d	DFFOUT_B34d	AN8	AE6								
4A	BIO9	VREFB4N0	IO			DFFIO_TX_B35a	DFFIN_B35a	AL12	AD12	DQSn7B	DQSn4B/DQ4B	DQSn2B/DQ2B	DQ1B	DQSn3B	DQSn2B/DQ2B	DQSn1B/DQ1B	DQ1B
4A	BIO9	VREFB4N0	IO			DFFIO_RX_B35b	DFFOUT_B35b	AP5	AF5	DQSn7B	DQ4B	DQ2B	DQ1B	DQSn3B	DQ2B	DQ1B	DQ1B
4A	BIO9	VREFB4N0	IO			DFFIO_TX_B35c	DFFIN_B35c	AK13	AC12	DQSn7B	DQSn4B/CQ4B	DQSn2B/CQ2B	DQ1B	DQSn3B	DQSn2B/CQ2B	DQSn1B/CQ1B	DQ1B
4A	BIO9	VREFB4N0	IO			DFFIO_RX_B35d	DFFOUT_B35d	AP4	AE5								
4A	BIO9	VREFB4N0	IO			DFFIO_TX_B36a	DFFIN_B36a	AC15	AC11	DQSn7B	DQ4B	DQ2B	DQ1B	DQ4B	DQ2B	DQ1B	DQ1B
4A	BIO9	VREFB4N0	IO			DFFIO_RX_B36b	DFFOUT_B36b	AL11	AG4	DQSn7B	DQ4B	DQ2B	DQ1B	DQ4B	DQ2B	DQ1B	DQ1B
4A	BIO9	VREFB4N0	IO			DFFIO_TX_B36c	DFFIN_B36c	AC14	AB11								
4A	BIO10	VREFB4N0	IO			DFFIO_RX_B37a	DFFOUT_B37a	AP17	AG3	DQSn7B	DQ4B	DQ2B	DQ1B	DQ4B	DQ2B	DQ1B	DQ1B
4A	BIO10	VREFB4N0	IO			DFFIO_TX_B37b	DFFIN_B37b	AP3	AH3	DQSn7B	DQ4B	DQ2B	DQ1B	DQ4B	DQ2B	DQ1B	DQ1B
4A	BIO10	VREFB4N0	IO			DFFIO_RX_B37c	DFFOUT_B37c	AN9	AF4	DQSn7B	DQ3B	DQ2B	DQ1B	DQ3B	DQ2B	DQ1B	DQ1B
4A	BIO10	VREFB4N0	IO			DFFIO_TX_B37d	DFFIN_B37d	AF2	AF2	DQSn7B	DQ3B	DQ2B	DQ1B	DQ3B	DQ2B	DQ1B	DQ1B
4A	BIO10	VREFB4N0	IO			DFFIO_RX_B38a	DFFOUT_B38a	AM8	AE4								
4A	BIO10	VREFB4N0	IO			DFFIO_TX_B38b	DFFIN_B38b	AF15	Y11	DQSn6B	DQ3B	DQ2B	DQ1B	DQSn2B	DQ1B	DQ1B	DQ1B
4A	BIO10	VREFB4N0	IO			DFFIO_RX_B38c	DFFOUT_B38c	AM10	AF3	DQSn6B	DQ3B	DQ2B	DQ1B	DQSn2B	DQ1B	DQ1B	DQ1B
4A	BIO10	VREFB4N0	IO			DFFIO_TX_B38d	DFFIN_B38d	AE15	W10	DQSn6B	DQ3B	DQ2B	DQ1B	DQSn2B	DQ1B	DQ1B	DQ1B
4A	BIO10	VREFB4N0	IO			DFFIO_RX_B39a	DFFOUT_B39a	AL10	AF2	DQSn6B	DQSn3B/DQ3B	DQ2B	DQ1B	DQSn1B	DQSn1B/DQ1B	DQ1B	DQ1B
4A	BIO10	VREFB4N0	IO			DFFIO_TX_B39b	DFFIN_B39b	AM4	AG1	DQSn6B	DQ3B	DQ2B	DQ1B	DQSn1B	DQ1B	DQ1B	DQ1B
4A	BIO10	VREFB4N0	IO			DFFIO_RX_B39c	DFFOUT_B39c	AM7	AC6	DQSn6B	DQSn3B/CQ3B	DQ2B	DQ1B	DQSn1B	DQ1B	DQ1B	DQ1B
4A	BIO10	VREFB4N0	IO			DFFIO_TX_B39d	DFFIN_B39d	AN3	AF1								
4A	BIO10	VREFB4N0	IO			DFFIO_RX_B40a	DFFOUT_B40a	AL16	AA10	DQSn6B	DQ3B	DQ2B	DQ1B	DQ3B	DQ2B	DQ1B	DQ1B
4A	BIO10	VREFB4N0	IO			DFFIO_TX_B40b	DFFIN_B40b	AJ12	AD9	DQSn6B	DQ3B	DQ2B	DQ1B	DQ3B	DQ2B	DQ1B	DQ1B
4A	BIO10	VREFB4N0	IO			DFFIO_RX_B40c	DFFOUT_B40c	AJ15	Y10								
4A	BIO10	VREFB4N0	IO			DFFIO_TX_B40d	DFFIN_B40d	AE8	AE8	DQSn6B	DQ3B	DQ2B	DQ1B	DQ3B	DQ2B	DQ1B	DQ1B
4A	BIO10	VREFB4N0	IO	PLL3_CLKOUT1n				AJ13	AC10								
4A	BIO10	VREFB4N0	IO	PLL3_CLKOUT1p		DFFIO_RX_B41a	DFFOUT_B41a	AH13	AD7								
4A	BIO10	VREFB4N0	IO	PLL3_CLKOUT1n				AM14	AB10								
4A	BIO10	VREFB4N0	IO	PLL3_CLKOUT1p		DFFIO_RX_B41p	DFFOUT_B41p	AG13	AC7								
4A	BIO10	VREFB4N0	IO	PLL3_CLKOUT1n				AF14	AB9								
4A	BIO10	VREFB4N0	IO	PLL3_CLKOUT1p				AM12	AG8								
4A	BIO10	VREFB4N0	IO	PLL3_CLKOUT1p				AE14	AA9								
4A	BIO10	VREFB4N0	IO	PLL3_CLKOUT1p				AG12	AB8								
4B	BIO11	VREFB4N0	IO			DFFIO_TX_B41a	DFFIN_B41a	AK10		DQ4B	DQ2B	DQ1B					
4B	BIO11	VREFB4N0	IO			DFFIO_RX_B42a	DFFOUT_B42a	AL9		DQ4B	DQ2B	DQ1B					
4B	BIO11	VREFB4N0	IO			DFFIO_TX_B41p	DFFIN_B41p	AJ10		DQ4B	DQ2B	DQ1B					
4B	BIO11	VREFB4N0	IO			DFFIO_RX_B42b	DFFOUT_B42b	AK9									
4B	BIO11	VREFB4N0	IO			DFFIO_TX_B42c	DFFIN_B42c	AF13		DQSn4B	DQ2B	DQ1B					
4B	BIO11	VREFB4N0	IO			DFFIO_RX_B43a	DFFOUT_B43a	AL8		DQ4B	DQ2B	DQ1B					
4B	BIO11	VREFB4N0	IO			DFFIO_TX_B42d	DFFIN_B42d	AE13		DQSn4B	DQ2B	DQ1B					
4B	BIO11	VREFB4N0	IO			DFFIO_RX_B43b	DFFOUT_B43b	AL7			DQSn2B/CQ2B	DQ1B/CQ1B					
4B	BIO11	VREFB4N0	IO			DFFIO_TX_B43c	DFFIN_B43c	AL6		DQSn3B	DQSn2B/DQ2B	DQSn1B/DQ1B					
4B	BIO11	VREFB4N0	IO			DFFIO_RX_B44a	DFFOUT_B44a	AM8		DQ3B	DQ2B	DQ1B					
4B	BIO11	VREFB4N0	IO			DFFIO_TX_B44b	DFFIN_B44b	AM6		DQSn3B	DQSn2B/CQ2B	DQSn1B/CQ1B					
4B	BIO11	VREFB4N0	IO			DFFIO_RX_B44c	DFFOUT_B44c	AM5									
4B	BIO11	VREFB4N0	IO			DFFIO_TX_B44d	DFFIN_B44d	AF12		DQ3B	DQ2B	DQ1B					
4B	BIO11	VREFB4N0	IO			DFFIO_RX_B45a	DFFOUT_B45a	AE12		DQ3B	DQ2B	DQ1B					
4B	BIO11	VREFB4N0	IO			DFFIO_TX_B45b	DFFIN_B45b	AF7		DQ3B	DQ2B	DQ1B					
4B	BIO12	VREFB4N0	IO			DFFIO_RX_B45c	DFFOUT_B45c	AM4		DQ2B	DQ1B	DQ1B					
4B	BIO12	VREFB4N0	IO			DFFIO_TX_B46a	DFFIN_B46a	AJ9		DQ2B	DQ1B	DQ1B					
4B	BIO12	VREFB4N0	IO			DFFIO_RX_B45d	DFFOUT_B45d	AL5		DQ2B	DQ1B	DQ1B					
4B	BIO12	VREFB4N0	IO			DFFIO_TX_B46b	DFFIN_B46b	AH9									
4B	BIO12	VREFB4N0	IO			DFFIO_RX_B46c	DFFOUT_B46c	AE11		DQSn2B	DQ1B	DQ1B					
4B	BIO12	VREFB4N0	IO			DFFIO_TX_B47a	DFFIN_B47a	AH10		DQ2B	DQ1B	DQ1B					
4B	BIO12	VREFB4N0	IO			DFFIO_RX_B46d	DFFOUT_B46d	AD12		AB10	DQSn2B	DQ1B/CQn1B	DQ1B				
4B	BIO12	VREFB4N0	IO			DFFIO_TX_B47b	DFFIN_B47b	AG9									
4B	BIO12	VREFB4N0	IO			DFFIO_RX_B47c	DFFOUT_B47c	AM2		DQSn1B	DQSn1B/DQ1B	DQ1B					
4B	BIO12	VREFB4N0	IO			DFFIO_TX_B47d	DFFIN_B47d	AK3		DQ2B	DQ1B	DQ1B					
4B	BIO12	VREFB4N0	IO			DFFIO_RX_B48a	DFFOUT_B48a	AN1		DQSn1B	DQSn1B/CQ1B	DQ1B					
4B	BIO12	VREFB4N0	IO			DFFIO_TX_B48b	DFFIN_B48b	AF11									
4B	BIO12	VREFB4N0	IO			DFFIO_RX_B48c	DFFOUT_B48c	AM1		DQ1B	DQ1B	DQ1B					
5B	RI01	VREFB5N0	IO			DFFIO_TX_R1a	DFFIN_R1a	AE6			DQ2R	DQ1R	DQ0R				
5B	RI01	VREFB5N0	IO			DFFIO_RX_R1b	DFFOUT_R1b	AF7		DQ2R	DQ1R	DQ0R					
5B	RI01	VREFB5N0	IO			DFFIO_TX_R1c	DFFIN_R1c	AF7		DQ22R	DQ12R	DQ0R					
5B	RI01	VREFB5N0	IO			DFFIO_RX_R1d	DFFOUT_R1d	AF8									
5B	RI01	VREFB5N0	IO			DFFIO_TX_R2a	DFFIN_R2a	AD9		DQSn24R	DQ12R	DQ0R					
5B	RI01	VREFB5N0	IO			DFFIO_RX_R2b	DFFOUT_R2b	AK3		DQ22R	DQ12R	DQ0R					
5B	RI01	VREFB5N0	IO			DFFIO_TX_R2c	DFFIN_R2c	AD10		DQSn24R	DQ12R/CQn12R	DQ0R					
5B	RI01	VREFB5N0	IO			DFFIO_RX_R2d	DFFOUT_R2d	AK4									
5B	RI01	VREFB5N0	IO			DFFIO_TX_R3a	DFFIN_R3a	AH5		DQSn23R	DQSn12R/DQ12R	DQ0R					
5B	RI01	VREFB5N0	IO			DFFIO_RX_R3b	DFFOUT_R3b	AK6		DQ22R	DQ12R	DQ0R					
5B	RI01	VREFB5N0	IO			DFFIO_TX_R3c	DFFIN_R3c	AH6		DQSn23R	DQSn12R/CQ12R	DQ0R					
5B	RI01	VREFB5N0	IO			DFFIO_RX_R3d	DFFOUT_R3d	AG7									
5B	RI01	VREFB5N0	IO			DFFIO_TX_R4a	DFFIN_R4a	AE7			DQ12R	DQ0R					
5B	RI01	VREFB5N0	IO														



Bank number	IO Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT RA	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT RA (Note 2)	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)
5B	RI02	VREFB5N0	IO			DIFFIO_RX_R6n	DIFFOUT_R6n	AF0		DQ22R	DQ21R	DQ2R					
5B	RI02	VREFB5N0	IO			DIFFIO_RX_R6p	DIFFOUT_R6p	AC11		DQ22R	DQ21R	DQ2R					
5B	RI02	VREFB5N0	IO			DIFFIO_RX_R6p	DIFFOUT_R6p	AH3		DQ22R	DQ21R	DQ2R					
5B	RI02	VREFB5N0	IO			DIFFIO_TX_R7n	DIFFOUT_R7n	AF5		DQ22R	DQ21R	DQ2R					
5B	RI02	VREFB5N0	IO			DIFFIO_RX_R7n	DIFFOUT_R7n	AH4		DQ21R	DQ21R	DQ2R					
5B	RI02	VREFB5N0	IO			DIFFIO_TX_R7p	DIFFOUT_R7p	AF6		DQ22R	DQ21R	DQ2R					
5B	RI02	VREFB5N0	IO			DIFFIO_RX_R7p	DIFFOUT_R7p	AC4		DQ21R	DQ21R	DQ2R					
5B	RI02	VREFB5N0	IO			DIFFIO_TX_R8n	DIFFOUT_R8n	AF8		DQ21R	DQ21R	DQ2R					
5B	RI02	VREFB5N0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	AC8		DQ21R	DQ21R	DQ2R					
5B	RI02	VREFB5N0	IO			DIFFIO_TX_R8p	DIFFOUT_R8p	AF9		DQ21R	DQ21R	DQ2R					
5B	RI02	VREFB5N0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	AC9		DQ21R	DQ21R	DQ2R					
5B	RI02	VREFB5N0	IO			DIFFIO_TX_R9n	DIFFOUT_R9n	AF9		DQ21R	DQ21R	DQ2R					
5A	RI03	VREFB5N0	IO			DIFFIO_TX_R9n	DIFFOUT_R9n	AD6	AA6	DQ20R	DQ10R	DQ2R	DQ2R	DQ14R	DO7R	DQ3R	DO1R
5A	RI03	VREFB5N0	IO			DIFFIO_RX_R9n	DIFFOUT_R9n	AC5	AD4	DQ20R	DQ10R	DQ2R	DQ2R	DQ14R	DO7R	DQ3R	DO1R
5A	RI03	VREFB5N0	IO			DIFFIO_TX_R9p	DIFFOUT_R9p	AD7	AB7	DQ20R	DQ10R	DQ2R	DQ2R	DQ14R	DO7R	DQ3R	DO1R
5A	RI03	VREFB5N0	IO			DIFFIO_RX_R9p	DIFFOUT_R9p	AC7	AC5								
5A	RI03	VREFB5N0	IO			DIFFIO_TX_R10n	DIFFOUT_R10n	AB9	WB	DQ20R	DQ10R	DQ2R	DQ2R	DQ14R	DO7R	DQ3R	DO1R
5A	RI03	VREFB5N0	IO			DIFFIO_RX_R10n	DIFFOUT_R10n	AB7	AB5	DQ20R	DQ10R	DQ2R	DQ2R	DQ14R	DO7R	DQ3R	DO1R
5A	RI03	VREFB5N0	IO			DIFFIO_TX_R10p	DIFFOUT_R10p	AB10	Y9	DQ20R	DQ10R/CQn10R	DQ2R	DQ2R	DQ14R	DO7R/CQn7R	DQ3R	DO1R
5A	RI03	VREFB5N0	IO			DIFFIO_RX_R10p	DIFFOUT_R10p	AB8	AB6								
5A	RI03	VREFB5N0	IO			DIFFIO_TX_R11n	DIFFOUT_R11n	AH1	AC4	DQ21R	DQ21R	DQ2R	DQ2R	DQ13R	DO7R	DQ3R	DO1R
5A	RI03	VREFB5N0	IO			DIFFIO_RX_R11n	DIFFOUT_R11n	AF4	Y5	DQ19R	DQ21R	DQ2R	DQ2R	DQ13R	DO7R	DQ3R	DO1R
5A	RI03	VREFB5N0	IO			DIFFIO_TX_R11p	DIFFOUT_R11p	AH2	AB4	DQ21R	DQ21R	DQ2R	DQ2R	DQ13R	DO7R/CQ7R	DQ3R	DO1R
5A	RI03	VREFB5N0	IO			DIFFIO_RX_R11p	DIFFOUT_R11p	AE4	Y6								
5A	RI03	VREFB5N0	IO			DIFFIO_TX_R12n	DIFFOUT_R12n	Y6	WB	DQ19R	DQ19R	DQ2R	DQ2R	DQ13R	DO7R	DQ3R	DO1R
5A	RI03	VREFB5N0	IO			DIFFIO_RX_R12n	DIFFOUT_R12n	AG1	AE3	DQ19R	DQ19R	DQ2R	DQ2R	DQ13R	DO7R	DQ3R	DO1R
5A	RI03	VREFB5N0	IO			DIFFIO_TX_R12p	DIFFOUT_R12p	AA7	Y7								
5A	RI03	VREFB5N0	IO			DIFFIO_RX_R12p	DIFFOUT_R12p	AF1	AD3	DQ19R	DQ19R	DQ2R	DQ2R	DQ13R	DO7R	DQ3R	DO1R
5A	RI04	VREFB5N0	IO			DIFFIO_TX_R13n	DIFFOUT_R13n	AF2	AC2	DQ18R	DQ2R	DQ2R	DQ2R	DQ12R	DO6R	DQ3R	DO1R
5A	RI04	VREFB5N0	IO			DIFFIO_RX_R13n	DIFFOUT_R13n	AF3	AC3	DQ18R	DQ2R	DQ2R	DQ2R	DQ12R	DO6R	DQ3R	DO1R
5A	RI04	VREFB5N0	IO			DIFFIO_TX_R13p	DIFFOUT_R13p	AF3	AC3	DQ18R	DQ2R	DQ2R	DQ2R	DQ12R	DO6R	DQ3R	DO1R
5A	RI04	VREFB5N0	IO			DIFFIO_RX_R13p	DIFFOUT_R13p	AE2	AA4								
5A	RI04	VREFB5N0	IO			DIFFIO_TX_R14n	DIFFOUT_R14n	AA5	WB	DQ21R	DQ2R	DQ2R	DQ2R	DQ12R	DO6R	DQ3R	DO1R
5A	RI04	VREFB5N0	IO			DIFFIO_RX_R14n	DIFFOUT_R14n	AA5	WB	DQ21R	DQ2R	DQ2R	DQ2R	DQ12R	DO6R	DQ3R	DO1R
5A	RI04	VREFB5N0	IO			DIFFIO_TX_R14p	DIFFOUT_R14p	AA10	UB	DQ21R	DQ2R/CQnR	DQ2R	DQ2R	DQ12R	DO6R/CQnR	DQ3R/CQn3R	DO1R
5A	RI04	VREFB5N0	IO			DIFFIO_RX_R14p	DIFFOUT_R14p	AB6	WB								
5A	RI04	VREFB5N0	IO			DIFFIO_TX_R15n	DIFFOUT_R15n	AE3	AB2	DQ21R	DQ2R	DQ2R	DQ2R	DQ11R	DO6R	DQ3R	DO1R
5A	RI04	VREFB5N0	IO			DIFFIO_RX_R15n	DIFFOUT_R15n	AC4	Y3	DQ17R	DQ2R	DQ2R	DQ2R	DQ11R	DO6R	DQ3R	DO1R
5A	RI04	VREFB5N0	IO			DIFFIO_TX_R15p	DIFFOUT_R15p	AD4	AB3	DQ21R	DQ2R/CQnR	DQ2R	DQ2R	DQ11R	DO6R/CQnR	DQ3R/CQn3R	DO1R
5A	RI04	VREFB5N0	IO			DIFFIO_RX_R15p	DIFFOUT_R15p	AC5	Y4								
5A	RI04	VREFB5N0	IO			DIFFIO_TX_R16n	DIFFOUT_R16n	Y7	T6	DQ17R	DQ2R	DQ2R	DQ2R	DQ11R	DO6R	DQ3R	DO1R
5A	RI04	VREFB5N0	IO			DIFFIO_RX_R16n	DIFFOUT_R16n	AD1	AE1	DQ17R	DQ2R	DQ2R	DQ2R	DQ11R	DO6R	DQ3R	DO1R
5A	RI04	VREFB5N0	IO			DIFFIO_TX_R16p	DIFFOUT_R16p	Y8	T7								
5A	RI04	VREFB5N0	IO			DIFFIO_RX_R16p	DIFFOUT_R16p	AC1	AD1	DQ17R	DQ2R	DQ2R	DQ2R	DQ11R	DO6R	DQ3R	DO1R
5A	RI05	VREFB5N0	IO			DIFFIO_TX_R17n	DIFFOUT_R17n	AC2	AC1	DQ16R	DQ2R	DQ2R	DQ2R	DQ10R	DO6R	DQ3R	DO1R
5A	RI05	VREFB5N0	IO			DIFFIO_RX_R17n	DIFFOUT_R17n	AB3	AB1	DQ16R	DQ2R	DQ2R	DQ2R	DQ10R	DO6R	DQ3R	DO1R
5A	RI05	VREFB5N0	IO			DIFFIO_TX_R17p	DIFFOUT_R17p	AC3	AB1	DQ16R	DQ2R	DQ2R	DQ2R	DQ10R	DO6R	DQ3R	DO1R
5A	RI05	VREFB5N0	IO			DIFFIO_RX_R17p	DIFFOUT_R17p	AB4	Y1								
5A	RI05	VREFB5N0	IO			DIFFIO_TX_R18n	DIFFOUT_R18n	Y10	AA	DQ21R	DQ2R	DQ2R	DQ2R	DQ10R	DO6R	DQ3R	DO1R
5A	RI05	VREFB5N0	IO			DIFFIO_RX_R18n	DIFFOUT_R18n	AB1	Y3	DQ18R	DQ2R	DQ2R	DQ2R	DQ10R	DO6R	DQ3R	DO1R
5A	RI05	VREFB5N0	IO			DIFFIO_TX_R18p	DIFFOUT_R18p	Y11	PS	DQ21R	DQ2R	DQ2R	DQ2R	DQ10R	DO6R/CQnR	DQ3R	DO1R
5A	RI05	VREFB5N0	IO			DIFFIO_RX_R18p	DIFFOUT_R18p	AA2	Y4								
5A	RI05	VREFB5N0	IO			DIFFIO_TX_R19n	DIFFOUT_R19n	AA4	W1	DQ21R	DQ2R	DQ2R	DQ2R	DQ10R	DO6R	DQ3R	DO1R
5A	RI05	VREFB5N0	IO			DIFFIO_RX_R19n	DIFFOUT_R19n	AA1	W2	DQ15R	DQ2R	DQ2R	DQ2R	DQ10R	DO6R	DQ3R	DO1R
5A	RI05	VREFB5N0	IO			DIFFIO_TX_R19p	DIFFOUT_R19p	Y5	W1	DQ21R	DQ2R	DQ2R	DQ2R	DQ10R	DO6R	DQ3R	DO1R
5A	RI05	VREFB5N0	IO			DIFFIO_RX_R19p	DIFFOUT_R19p	Y1	W3								
5A	RI05	VREFB5N0	IO			DIFFIO_TX_R20n	DIFFOUT_R20n	Y9	RB	DQ15R	DQ2R	DQ2R	DQ2R	DQ10R	DO6R	DQ3R	DO1R
5A	RI05	VREFB5N0	IO			DIFFIO_RX_R20n	DIFFOUT_R20n	Y3	UB	DQ15R	DQ2R	DQ2R	DQ2R	DQ10R	DO6R	DQ3R	DO1R
5A	RI05	VREFB5N0	IO			DIFFIO_TX_R20p	DIFFOUT_R20p	Y10	W6								
5A	RI05	VREFB5N0	IO			DIFFIO_RX_R20p	DIFFOUT_R20p	Y4	US	DQ15R	DQ2R	DQ2R	DQ2R	DQ10R	DO6R	DQ3R	DO1R
5A	RI06	VREFB5N0	IO			DIFFIO_TX_R21n	DIFFOUT_R21n	W6	U3	DQ14R	DQ2R	DQ2R	DQ2R	DQ10R	DO6R	DQ3R	DO1R
5A	RI06	VREFB5N0	IO			DIFFIO_RX_R21n	DIFFOUT_R21n	W1	T3	DQ14R	DQ2R	DQ2R	DQ2R	DQ10R	DO6R	DQ3R	DO1R
5A	RI06	VREFB5N0	IO			DIFFIO_TX_R21p	DIFFOUT_R21p	W7	T4	DQ14R	DQ2R	DQ2R	DQ2R	DQ10R	DO6R	DQ3R	DO1R
5A	RI06	VREFB5N0	IO			DIFFIO_RX_R21p	DIFFOUT_R21p	Y2	R3								
5A	RI06	VREFB5N0	IO			DIFFIO_TX_R22n	DIFFOUT_R22n	Y10	N6	DQ21R	DQ2R	DQ2R	DQ2R	DQ10R	DO6R	DQ3R	DO1R
5A	RI06	VREFB5N0	IO			DIFFIO_RX_R22n	DIFFOUT_R22n	W3	U1	DQ14R	DQ2R	DQ2R	DQ2R	DQ10R	DO6R	DQ3R	DO1R
5A	RI06	VREFB5N0	IO			DIFFIO_TX_R22p	DIFFOUT_R22p	Y11	M6	DQ21R	DQ2R	DQ2R	DQ2R	DQ10R	DO6R	DQ3R	DO1R
5A	RI06	VREFB5N0	IO			DIFFIO_RX_R22p	DIFFOUT_R22p	W4	T1								
5A	RI06	VREFB5N0	IO			DIFFIO_TX_R23n	DIFFOUT_R23n	Y3	R1	DQ21R	DQ2R	DQ2R	DQ2R	DQ10R	DO6R	DQ3R	DO1R
5A	RI06	VREFB5N0	IO			DIFFIO_RX_R23n	DIFFOUT_R23n	Y1	R4	DQ13R	DQ2R	DQ2R	DQ2R	DQ10R	DO6R	DQ3R	DO1R
5A	RI06	VREFB5N0	IO			DIFFIO_TX_R23p	DIFFOUT_R23p	Y7	P3	DQ13R	DQ2R	DQ2R	DQ2R	DQ10R	DO6R	DQ3R	DO1R
5A	RI06	VREFB5N0	IO			DIFFIO_RX_R23p	DIFFOUT_R23p	Y2	R5								
5A	RI06	VREFB5N0	IO			DIFFIO_TX_R24n	DIFFOUT_R24n	Y12	M5	DQ13R	DQ2R	DQ2R	DQ2R	DQ10R	DO6R	DQ3R	DO1R
5A	RI06	VREFB5N0	IO			DIFFIO_RX_R24n	DIFFOUT_R24n	Y7	P3	DQ13R	DQ2R	DQ2R	DQ2R	DQ10R	DO6R	DQ3R	DO1R
5A	RI06	VREFB5N0	IO			DIFFIO_TX_R24p	DIFFOUT_R24p	Y12	L6								
5A	RI06	VREFB5N0	IO			DIFFIO_RX_R24p	DIFFOUT_R24p	Y7	P4	DQ13R	DQ2R	DQ2R	DQ2R	DQ10R	DO6R	DQ3R	DO1R
5A	VREFB5N0	CLK8	DIFFCLK_2n														
5A	VREFB5N0	CLK10	DIFFCLK_2p														
5A	VREFB5N0	CLK9	DIFFCLK_3n														
5A	VREFB5N0	CLK11	DIFFCLK_3p														
6A	RI07	VREFB5N0	IO			DIFFIO_TX_R25n	DIFFOUT_R25n	Y7	L1	DQ12R	DQ2R	DQ2R	DQ2R	DQ10R	DO6R	DQ3R	DO1R
6A	RI07	VREFB5N0	IO			DIFFIO_RX_R25n	DIFFOUT_R25n	U1	M2	DQ12R	DQ2R	DQ2R	DQ2R	DQ10R	DO6R	DQ3R	DO1R
6A	RI07	VREFB5N0	IO			DIFFIO_TX_R25p	DIFFOUT_R25p	R7	K1	DQ12R	DQ2R	DQ2R	DQ2R	DQ10R	DO6R	DQ3R	DO1R
6A	RI07	VREFB5N0	IO			DIFFIO_RX_R25p	DIFFOUT_R25p	U2	L3								
6A	RI07	VREFB5N0	IO			DIFFIO_TX_R26n	DIFFOUT_R26n	U10	R6	DQ21R	DQ2R	DQ2R	DQ2R	DQ10R	DO6R	DQ3R	DO1R
6A	RI07	VREFB5N0	IO			DIFFIO_RX_R26n	DIFFOUT_R26n	T1	M3	DQ12R	DQ2R	DQ2R	DQ2R	DQ10R	DO6R	DQ3R	DO1R
6A	RI07	VREFB5N0	IO			DIFFIO_TX_R26p	DIFFOUT_R26p	U7	L2	DQ21R	DQ2R	DQ2R	DQ2R	DQ10R	DO6R	DQ3R	DO1R
6A	RI07	VREFB5N0	IO			DIFFIO_RX_R26p	DIFFOUT_R26p	R1	M4								
6A	RI07	VREFB5N0	IO			DIFFIO_TX_R27n	DIFFOUT_R27n	Y1	J2	DQ21R	DQ2R	DQ2R	DQ2R	DQ10R			



Bank number	IO Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with no OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)	
6A	RI08	VREFBAND	IO			DIFFIO_RX_R31b	DIFFIO_RX31b	F0	H4									
6A	RI08	VREFBAND	IO			DIFFIO_TX_R32a	DIFFIN_R32a	R9	K5	DQ3R	DQ3R	DQ3R	DQ1R	DQ3R	DQ2R	DQ1R		
6A	RI08	VREFBAND	IO			DIFFIO_RX_R32b	DIFFOUT_R32b	J1	K4	DQ3R	DQ3R	DQ3R	DQ1R	DQ3R	DQ2R	DQ1R		
6A	RI08	VREFBAND	IO			DIFFIO_TX_R32c	DIFFIN_R32c	L10	K9									
6A	RI08	VREFBAND	IO			DIFFIO_RX_R32d	DIFFOUT_R32d	K2	K5	DQ3R	DQ3R	DQ3R	DQ1R	DQ3R	DQ2R	DQ1R		
6A	RI08	VREFBAND	IO			DIFFIO_TX_R33a	DIFFIN_R33a	H1		DQ3R	DQ3R	DQ3R	DQ1R					
6A	RI08	VREFBAND	IO			DIFFIO_RX_R33b	DIFFOUT_R33b	F1		DQ3R	DQ3R	DQ3R	DQ1R					
6A	RI08	VREFBAND	IO			DIFFIO_TX_R33c	DIFFIN_R33c	G1		DQ3R	DQ3R	DQ3R	DQ1R					
6A	RI08	VREFBAND	IO			DIFFIO_RX_R33d	DIFFOUT_R33d	E1										
6A	RI08	VREFBAND	IO			DIFFIO_TX_R34a	DIFFIN_R34a	F7		DQ3R	DQ3R	DQ3R	DQ1R					
6A	RI08	VREFBAND	IO			DIFFIO_RX_R34b	DIFFOUT_R34b	D1		DQ3R	DQ3R	DQ3R	DQ1R					
6A	RI08	VREFBAND	IO			DIFFIO_TX_R34c	DIFFIN_R34c	R8		DQ3R	DQ3R	DQ3R	DQ1R					
6A	RI08	VREFBAND	IO			DIFFIO_RX_R34d	DIFFOUT_R34d	D2										
6A	RI08	VREFBAND	IO			DIFFIO_TX_R35a	DIFFIN_R35a	N3		DQ3R	DQ3R	DQ3R	DQ1R					
6A	RI08	VREFBAND	IO			DIFFIO_RX_R35b	DIFFOUT_R35b	N4		DQ3R	DQ3R	DQ3R	DQ1R					
6A	RI08	VREFBAND	IO			DIFFIO_TX_R35c	DIFFIN_R35c	M3		DQ3R	DQ3R	DQ3R	DQ1R					
6A	RI08	VREFBAND	IO			DIFFIO_RX_R35d	DIFFOUT_R35d	M5										
6A	RI08	VREFBAND	IO			DIFFIO_TX_R36a	DIFFIN_R36a	P9		DQ7R	DQ4R	DQ2R	DQ1R					
6A	RI08	VREFBAND	IO			DIFFIO_RX_R36b	DIFFOUT_R36b	C1		DQ7R	DQ4R	DQ2R	DQ1R					
6A	RI08	VREFBAND	IO			DIFFIO_TX_R36c	DIFFIN_R36c	P10										
6A	RI08	VREFBAND	IO			DIFFIO_RX_R36d	DIFFOUT_R36d	C2		DQ7R	DQ4R	DQ2R	DQ1R					
6A	RI010	VREFBAND	IO		DATA7	DIFFIO_TX_R37a	DIFFIN_R37a	K2	B1	DQ6R	DQ3R	DQ2R	DQ1R	DQ2R	DQ1R			
6A	RI010	VREFBAND	IO		DATA6	DIFFIO_RX_R37b	DIFFOUT_R37b	M4	C2	DQ6R	DQ3R	DQ2R	DQ1R	DQ2R	DQ1R			
6A	RI010	VREFBAND	IO		DATA5	DIFFIO_TX_R37c	DIFFIN_R37c	K3	A2	DQ6R	DQ3R	DQ2R	DQ1R	DQ2R	DQ1R			
6A	RI010	VREFBAND	IO		DATA4	DIFFIO_RX_R37d	DIFFOUT_R37d	L4	C3									
6A	RI010	VREFBAND	IO		DATA3	DIFFIO_TX_R38a	DIFFIN_R38a	P8	H6	DQ5R	DQ3R	DQ3R	DQ1R	DQ3R	DQ1R			
6A	RI010	VREFBAND	IO		DATA2	DIFFIO_RX_R38b	DIFFOUT_R38b	G2	G3	DQ6R	DQ3R	DQ2R	DQ1R	DQ3R	DQ1R			
6A	RI010	VREFBAND	IO		DATA1	DIFFIO_TX_R38c	DIFFIN_R38c	M6	H7	DQ5R	DQ3R	DQ2R	DQ1R	DQ3R	DQ1R			
6A	RI010	VREFBAND	IO		CLKUSR	DIFFIO_RX_R38d	DIFFOUT_R38d	H4	F4									
6A	RI010	VREFBAND	IO			DIFFIO_TX_R39a	DIFFIN_R39a	L4	E3	DQ5R	DQ3R	DQ2R	DQ1R	DQ3R	DQ1R			
6A	RI010	VREFBAND	IO			DIFFIO_RX_R39b	DIFFOUT_R39b	J3	F3	DQ5R	DQ3R	DQ2R	DQ1R	DQ3R	DQ1R			
6A	RI010	VREFBAND	IO		DEV_OE	DIFFIO_TX_R39c	DIFFIN_R39c	J5	D3	DQ5R	DQ3R	DQ2R	DQ1R	DQ3R	DQ1R			
6A	RI010	VREFBAND	IO			DIFFIO_RX_R40a	DIFFOUT_R40a	R3	F4									
6A	RI010	VREFBAND	IO			DIFFIO_TX_R40b	DIFFIN_R40b	M9	G5	DQ5R	DQ3R	DQ2R	DQ1R	DQ3R	DQ1R			
6A	RI010	VREFBAND	IO		DEV_CLRn	DIFFIO_RX_R40c	DIFFOUT_R40c	K4	E4	DQ5R	DQ3R	DQ2R	DQ1R	DQ3R	DQ1R			
6A	RI010	VREFBAND	IO			DIFFIO_TX_R40d	DIFFIN_R40d	M10										
6B	RI011	VREFBAND	IO			DIFFIO_RX_R40e	DIFFOUT_R40e	K5	F5	DQ5R	DQ3R	DQ2R	DQ1R	DQ3R	DQ1R			
6B	RI011	VREFBAND	IO			DIFFIO_TX_R41a	DIFFIN_R41a	M5		DQ4R	DQ2R	DQ1R						
6B	RI011	VREFBAND	IO			DIFFIO_RX_R41b	DIFFOUT_R41b	G3		DQ4R	DQ2R	DQ1R						
6B	RI011	VREFBAND	IO			DIFFIO_TX_R41c	DIFFIN_R41c	M6		DQ4R	DQ2R	DQ1R						
6B	RI011	VREFBAND	IO			DIFFIO_RX_R41d	DIFFOUT_R41d	H4										
6B	RI011	VREFBAND	IO			DIFFIO_TX_R42a	DIFFIN_R42a	N7		DQ3R	DQ2R	DQ1R						
6B	RI011	VREFBAND	IO			DIFFIO_RX_R42b	DIFFOUT_R42b	F3		DQ4R	DQ2R	DQ1R						
6B	RI011	VREFBAND	IO			DIFFIO_TX_R42c	DIFFIN_R42c	M8		DQ4R	DQ2R	DQ1R						
6B	RI011	VREFBAND	IO			DIFFIO_RX_R42d	DIFFOUT_R42d	F4		DQ3R	DQ2R	DQ1R						
6B	RI011	VREFBAND	IO			DIFFIO_TX_R43a	DIFFIN_R43a	S3		DQ3R	DQ2R	DQ1R						
6B	RI011	VREFBAND	IO			DIFFIO_RX_R43b	DIFFOUT_R43b	E3		DQ3R	DQ2R	DQ1R						
6B	RI011	VREFBAND	IO			DIFFIO_TX_R43c	DIFFIN_R43c	D4		DQ3R	DQ2R	DQ1R						
6B	RI011	VREFBAND	IO			DIFFIO_RX_R43d	DIFFOUT_R43d	E4		DQ3R	DQ2R	DQ1R						
6B	RI011	VREFBAND	IO			DIFFIO_TX_R44a	DIFFIN_R44a	M9		DQ3R	DQ2R	DQ1R						
6B	RI011	VREFBAND	IO			DIFFIO_RX_R44b	DIFFOUT_R44b	K6		DQ3R	DQ2R	DQ1R						
6B	RI011	VREFBAND	IO			DIFFIO_TX_R44c	DIFFIN_R44c	M10										
6B	RI011	VREFBAND	IO			DIFFIO_RX_R44d	DIFFOUT_R44d	K7		DQ3R	DQ2R	DQ1R						
6B	RI012	VREFBAND	IO			DIFFIO_TX_R45a	DIFFIN_R45a	K6		DQ3R	DQ2R	DQ1R						
6B	RI012	VREFBAND	IO			DIFFIO_RX_R45b	DIFFOUT_R45b	J7		DQ2R	DQ1R	DQ1R						
6B	RI012	VREFBAND	IO			DIFFIO_TX_R45c	DIFFIN_R45c	G4		DQ2R	DQ1R	DQ1R						
6B	RI012	VREFBAND	IO			DIFFIO_RX_R45d	DIFFOUT_R45d	G5										
6B	RI012	VREFBAND	IO			DIFFIO_TX_R46a	DIFFIN_R46a	M7		DQ3R	DQ1R	DQ1R						
6B	RI012	VREFBAND	IO			DIFFIO_RX_R46b	DIFFOUT_R46b	C5		DQ2R	DQ1R	DQ1R						
6B	RI012	VREFBAND	IO			DIFFIO_TX_R46c	DIFFIN_R46c	M8		DQ3R	DQ1R	DQ1R						
6B	RI012	VREFBAND	IO			DIFFIO_RX_R46d	DIFFOUT_R46d	S5		DQ3R	DQ1R	DQ1R						
6B	RI012	VREFBAND	IO			DIFFIO_TX_R47a	DIFFIN_R47a	F5		DQ3R	DQ1R	DQ1R						
6B	RI012	VREFBAND	IO			DIFFIO_RX_R47b	DIFFOUT_R47b	C6		DQ1R	DQ1R	DQ1R						
6B	RI012	VREFBAND	IO			DIFFIO_TX_R47c	DIFFIN_R47c	G6		DQ3R	DQ1R	DQ1R						
6B	RI012	VREFBAND	IO			DIFFIO_RX_R47d	DIFFOUT_R47d	D6										
6B	RI012	VREFBAND	IO			DIFFIO_TX_R48a	DIFFIN_R48a	L7		DQ1R	DQ1R	DQ1R						
6B	RI012	VREFBAND	IO			DIFFIO_RX_R48b	DIFFOUT_R48b	H7		DQ1R	DQ1R	DQ1R						
6B	RI012	VREFBAND	IO			DIFFIO_TX_R48c	DIFFIN_R48c	M8										
6B	RI012	VREFBAND	IO			DIFFIO_RX_R48d	DIFFOUT_R48d	J8		DQ1R	DQ1R	DQ1R						
7B	TI012	VREFB7ND	IO			DIFFIO_TX_T1p	DIFFIN_T1p	L11										
7B	TI012	VREFB7ND	IO			DIFFIO_RX_T1n	DIFFOUT_T1n	E6		DQ24T	DQ12T	DQ6T						
7B	TI012	VREFB7ND	IO			DIFFIO_TX_T2p	DIFFIN_T2p	K11		DQ24T	DQ12T	DQ6T						
7B	TI012	VREFB7ND	IO			DIFFIO_RX_T2n	DIFFOUT_T2n	G7										
7B	TI012	VREFB7ND	IO			DIFFIO_TX_T2p	DIFFIN_T2p	H9		DQ324T	DQ312T	DQ6T						
7B	TI012	VREFB7ND	IO			DIFFIO_RX_T2n	DIFFOUT_T2n	F7		DQ324T	DQ312T	DQ6T						
7B	TI012	VREFB7ND	IO			DIFFIO_TX_T2p	DIFFIN_T2p	G9		DQ324T	DQ312T	DQ6T						
7B	TI012	VREFB7ND	IO			DIFFIO_RX_T3n	DIFFOUT_T3n	E7										
7B	TI012	VREFB7ND	IO			DIFFIO_TX_T3p	DIFFIN_T3p	L10		DQ32T	DQ12T	DQ6T						
7B	TI012	VREFB7ND	IO			DIFFIO_RX_T3n	DIFFOUT_T3n	O7		DQ32T	DQ12T	DQ6T						
7B	TI012	VREFB7ND	IO			DIFFIO_TX_T3p	DIFFIN_T3p	L9		DQ32T	DQ12T	DQ6T						
7B	TI012	VREFB7ND	IO			DIFFIO_RX_T4n	DIFFOUT_T4n	P9		DQ32T	DQ12T	DQ6T						
7B	TI012	VREFB7ND	IO			DIFFIO_TX_T4p	DIFFIN_T4p	F9		DQ32T	DQ12T	DQ6T						
7B	TI012	VREFB7ND	IO			DIFFIO_RX_T4n	DIFFOUT_T4n	G10		DQ32T	DQ12T	DQ6T						
7B	TI011	VREFB7ND	IO			DIFFIO_TX_T4p	DIFFIN_T4p	F8		DQ32T	DQ12T	DQ6T						
7B	TI011	VREFB7ND	IO			DIFFIO_RX_T5n	DIFFOUT_T5n	G8		DQ32T	DQ12T	DQ6T						
7B	TI011	VREFB7ND	IO			DIFFIO_TX_T5p	DIFFIN_T5p	K12										
7B	TI011	VREFB7ND	IO			DIFFIO_RX_T5n	DIFFOUT_T5n	C7		DQ32T	DQ11T	DQ6T						
7B	TI011	VREFB7ND	IO			DIFFIO_TX_T6n	DIFFIN_T6n	J11		DQ32T	DQ11T	DQ6T						
7B	TI011	VREFB7ND	IO			DIFFIO_RX_T6n	DIFFOUT_T6n	H12		DQ32T	DQ311T	DQ36T						
7B	TI011	VREFB7ND	IO			DIFFIO_TX_T7p	DIFFIN_T7p	E10										
7B	TI011	VREFB7ND	IO			DIFFIO_RX_T7n	DIFFOUT_T7n	M13		DQ32T	DQ311T	DQ36T						
7B	TI011	VREFB7ND	IO			DIFFIO_TX_T7n	DIFFIN_T7n	O9		DQ31T	DQ11T	DQ6T						
7B	TI011	VREFB7ND	IO			DIFFIO_RX_T8n	DIFFOUT_T8n	L3		DQ32T	DQ11T	DQ6T						
7B	TI011	VREFB7ND	IO			DIFFIO_TX_T8p	DIFFIN_T8p	J13		DQ31T	DQ11T	DQ6T						
7B	TI011	VREFB7ND	IO			DIFFIO_RX_T8n	DIFFOUT_T8n	C10		DQ31T	DQ11T	DQ6T						
7A	VREFB7AND	IO	RUP1			DIFFIO_TX_T8n	DIFFIN_T8n	H13		DQ31T	DQ11T	DQ6T						
7A	VREFB7AND	IO	PLL2_CLKOUT1p					G12	F7									
7A	VREFB7AND	IO	RDN1					K14	K10									
7A	VREFB7AND	IO	PLL2_CLKOUT1n					G11	J7									
7A	VREFB7AND	IO					</											



Bank number	I/O Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rx	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rx (Note 2)	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)
7A	TI09	VREFB7ANO	IO			DFFIO_RX_179p	DFFIO_TX_179p	F10	F10								
7A	TI09	VREFB7ANO	IO			DFFIO_RX_180p	DFFIO_TX_180p	F13	F8	DQ20T	DQ10T	DQ5T	DQ2T	DQ14T	DO7T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_190p	DFFIO_TX_190p	G15	G10	DQ20T	DQ10T	DQ5T	DQ2T	DQ14T	DO7T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_110p	DFFIO_TX_110p	B1	F10								
7A	TI09	VREFB7ANO	IO			DFFIO_RX_110p	DFFIO_TX_110p	F12	E6	DQ320T	DQ210T/CQ10T	DQ5T	DQ2T	DQ514T	DQ37T/CQ7T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_110p	DFFIO_TX_110p	A2	E10	DQ20T	DQ10T	DQ5T	DQ2T	DQ14T	DO7T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_110p	DFFIO_TX_110p	E12	D5	DQ3n20T	DQ3n10T/DQ10T	DQ6T	DQ2T	DQ3n14T	DQ3n7T/DQ7T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_111p	DFFIO_TX_111p	G13	D4								
7A	TI09	VREFB7ANO	IO			DFFIO_RX_111p	DFFIO_TX_111p	K15	K11	DQ319T	DQ10T/CQ10T	DQ5T	DQ2T	DQ313T	DO7T/CQ7T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_111p	DFFIO_TX_111p	B4	C4	DO18T	DQ10T	DQ5T	DQ2T	DQ13T	DO7T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_111p	DFFIO_TX_111p	J17	J10	DQ3n19T	DQ10T	DQ5T	DQ2T	DQ3n13T			
7A	TI09	VREFB7ANO	IO			DFFIO_RX_112p	DFFIO_TX_112p	E13	B3								
7A	TI09	VREFB7ANO	IO			DFFIO_RX_112p	DFFIO_TX_112p	D12	A5	DO18T	DQ10T	DQ5T	DQ2T	DQ13T	DO7T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_112p	DFFIO_TX_112p	D13	A3	DQ18T	DQ10T	DQ5T	DQ2T	DQ13T	DO7T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_112p	DFFIO_TX_112p	D11	A4	DO18T	DQ10T	DQ5T	DQ2T	DQ13T	DO7T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_113p	DFFIO_TX_113p	B3	E7	DO18T	DQ9T	DQ5T	DQ2T	DQ12T	DO6T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_113p	DFFIO_TX_113p	K16	C11								
7A	TI09	VREFB7ANO	IO			DFFIO_RX_113p	DFFIO_TX_113p	A3	D7	DO18T	DQ9T	DQ5T	DQ2T	DQ12T	DO6T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_113p	DFFIO_TX_113p	J16	F11	DO18T	DQ9T	DQ5T	DQ2T	DQ12T	DO6T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_114p	DFFIO_TX_114p	A5	B9								
7A	TI09	VREFB7ANO	IO			DFFIO_RX_114p	DFFIO_TX_114p	G14	E9	DQ318T	DQ39T/CQ9T	DQ5T	DQ2T	DQ312T	DO36T/CQ6T	DQ33T/CQ33T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_114p	DFFIO_TX_114p	A4	C5	DO18T	DQ9T	DQ5T	DQ2T	DQ12T	DO6T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_114p	DFFIO_TX_114p	F15	B9	DQ3n18T	DQ3n9T/DQ9T	DQ3n5T/DQ5T	DQ2T	DQ3n12T	DQ3n6T/DQ6T	DQ3n3T/DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_115p	DFFIO_TX_115p	C9	C7								
7A	TI09	VREFB7ANO	IO			DFFIO_RX_115p	DFFIO_TX_115p	L16	J12	DQ317T	DQ37T/CQ9T	DQ5T/CQ5T	DQ2T	DQ311T	DO36T/CQ6T	DQ33T/CQ33T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_115p	DFFIO_TX_115p	B8	C8	DO17T	DQ8T	DQ4T	DQ2T	DQ11T	DO6T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_115p	DFFIO_TX_115p	K17	J11	DQ3n17T	DQ8T	DQ4T	DQ2T	DQ3n11T			
7A	TI09	VREFB7ANO	IO			DFFIO_RX_116p	DFFIO_TX_116p	B8	D8								
7A	TI09	VREFB7ANO	IO			DFFIO_RX_116p	DFFIO_TX_116p	A6	C8	DO17T	DQ8T	DQ4T	DQ2T	DQ11T	DO6T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_116p	DFFIO_TX_116p	A6	C8	DO17T	DQ8T	DQ4T	DQ2T	DQ11T	DO6T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_116p	DFFIO_TX_116p	A7	C10	DO17T	DQ8T	DQ4T	DQ2T	DQ11T	DO6T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_117p	DFFIO_TX_117p	G14	E12	DQ16T	DQ8T	DQ4T	DQ2T	DQ10T	DO6T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_117p	DFFIO_TX_117p	J17	J12								
7A	TI09	VREFB7ANO	IO			DFFIO_RX_117p	DFFIO_TX_117p	C15	D12	DO16T	DQ8T	DQ4T	DQ2T	DQ10T	DO6T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_117p	DFFIO_TX_117p	H18	F12	DO16T	DQ8T	DQ4T	DQ2T	DQ10T	DO6T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_118p	DFFIO_TX_118p	A9	A9								
7A	TI09	VREFB7ANO	IO			DFFIO_RX_118p	DFFIO_TX_118p	E15	D11	DQ316T	DQ38T/CQ8T	DQ4T	DQ2T	DQ310T	DO36T/CQ6T	DQ33T/CQ33T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_118p	DFFIO_TX_118p	A8	B8	DO16T	DQ8T	DQ4T	DQ2T	DQ10T	DO6T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_118p	DFFIO_TX_118p	D15	C11	DQ3n16T	DQ38T/DQ8T	DQ4T	DQ2T	DQ3n10T	DQ3n6T/DQ6T	DQ3n3T/DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_119p	DFFIO_TX_119p	C13	G13								
7A	TI09	VREFB7ANO	IO			DFFIO_RX_119p	DFFIO_TX_119p	H18	K13	DQ315T	DQ37T/CQ8T	DQ4T	DQ2T	DQ39T	DO37T/CQ7T	DQ32T	DO1T/CQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_119p	DFFIO_TX_119p	C12	G12	DQ15T	DQ4T	DQ2T	DQ2T	DQ10T	DO6T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_119p	DFFIO_TX_119p	G18	K12	DQ3n15T	DQ37T	DQ4T	DQ2T	DQ3n9T	DO6T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_120p	DFFIO_TX_120p	F16	E13								
7A	TI09	VREFB7ANO	IO			DFFIO_RX_120p	DFFIO_TX_120p	D13	D13	DQ15T	DQ4T	DQ2T	DQ2T	DQ10T	DO6T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_120p	DFFIO_TX_120p	E16	D13	DQ15T	DQ8T	DQ4T	DQ2T	DQ10T	DO6T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_120p	DFFIO_TX_120p	C16	D12	DO15T	DQ8T	DQ4T	DQ2T	DQ10T	DO6T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_121p	DFFIO_TX_121p	A6	B13	DO14T	DQ7T	DQ4T	DQ2T	DQ9T	DO6T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_121p	DFFIO_TX_121p	G17	K14								
7A	TI09	VREFB7ANO	IO			DFFIO_RX_121p	DFFIO_TX_121p	B12	A6	DO14T	DQ7T	DQ4T	DQ2T	DQ9T	DO6T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_121p	DFFIO_TX_121p	G16	J14	DO14T	DQ7T	DQ4T	DQ2T	DQ9T	DO6T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_122p	DFFIO_TX_122p	A12	A10								
7A	TI09	VREFB7ANO	IO			DFFIO_RX_122p	DFFIO_TX_122p	B10	A8	DQ314T	DQ37T/CQ7T	DQ34T/CQ4T	DQ2T	DQ38T	DO34T/CQ4T	DQ32T/CQ2T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_122p	DFFIO_TX_122p	A11	A8	DO14T	DQ7T	DQ4T	DQ2T	DQ9T	DO6T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_122p	DFFIO_TX_122p	A10	A7	DQ3n14T	DQ37T/DQ7T	DQ3n4T/DQ4T	DQ2T	DQ3n8T	DQ3n4T/DQ4T	DQ3n2T/DQ2T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_123p	DFFIO_TX_123p	A14	B12								
7A	TI09	VREFB7ANO	IO			DFFIO_RX_123p	DFFIO_TX_123p	M17	G14	DQ313T	DQ7T/CQ9T	DQ4T/CQ4T	DQ2T	DQ37T	DO4T/CQ4T	DQ32T/CQ2T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_123p	DFFIO_TX_123p	A13	A11	DO13T	DQ7T	DQ4T	DQ2T	DQ9T	DO6T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_123p	DFFIO_TX_123p	M16	F14	DQ3n13T	DQ7T	DQ4T	DQ2T	DQ9T	DO6T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_124p	DFFIO_TX_124p	B15	A13								
7A	TI09	VREFB7ANO	IO			DFFIO_RX_124p	DFFIO_TX_124p	B16	A15	DO13T	DQ7T	DQ4T	DQ2T	DQ9T	DO6T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_124p	DFFIO_TX_124p	A15	A12	DO13T	DQ7T	DQ4T	DQ2T	DQ9T	DO6T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_124p	DFFIO_TX_124p	A16	A14	DO13T	DQ7T	DQ4T	DQ2T	DQ9T	DO6T	DQ3T	DQ1T
7A	TI09	VREFB7ANO	IO			DFFIO_RX_124n	DFFIO_TX_124n	F18	D15								
7A	TI09	VREFB7ANO	IO			DFFIO_RX_124n	DFFIO_TX_124n	K18	D14								
7A	TI09	VREFB7ANO	IO			DFFIO_RX_124n	DFFIO_TX_124n	F17	C15								
7A	TI09	VREFB7ANO	IO			DFFIO_RX_124n	DFFIO_TX_124n	L18	C14								
8A	TI06	VREFB8ANO	IO			DFFIO_RX_125p	DFFIO_TX_125p	D18	C16	DO12T				DQ3T			DQ1T
8A	TI06	VREFB8ANO	IO			DFFIO_RX_125p	DFFIO_TX_125p	M19	F16								
8A	TI06	VREFB8ANO	IO			DFFIO_RX_125p	DFFIO_TX_125p	D17	B15	DO12T				DQ3T			DQ1T
8A	TI06	VREFB8ANO	IO			DFFIO_RX_125p	DFFIO_TX_125p	M18	F15	DO12T				DQ3T			DQ1T
8A	TI06	VREFB8ANO	IO			DFFIO_RX_126p	DFFIO_TX_126p	C18	A18								
8A	TI06	VREFB8ANO	IO			DFFIO_RX_126p	DFFIO_TX_126p	B18	A17	DQ312T	DQ36T/CQ6T	DQ33T/CQ3T	DQ1T	DQ36T	DO33T/CQ3T	DQ31T/CQ1T	DQ1T
8A	TI06	VREFB8ANO	IO			DFFIO_RX_126p	DFFIO_TX_126p	B18	A17	DO12T	DQ3T	DQ1T	DQ1T	DQ3T			
8A	TI06	VREFB8ANO	IO			DFFIO_RX_126p	DFFIO_TX_126p	A17	A16	DQ3n12T	DQ36T/DQ6T	DQ3n3T/DQ3T	DQ1T	DQ36T	DQ3n3T/DQ3T	DQ3n1T/DQ1T	DQ1T
8A	TI06	VREFB8ANO	IO			DFFIO_RX_127p	DFFIO_TX_127p	B19	E15								
8A	TI06	VREFB8ANO	IO			DFFIO_RX_127p	DFFIO_TX_127p	G19	H15	DQ311T	DQ6T/CQ6T	DQ3T/CQ3T	DQ1T	DQ35T	DO33T/CQ3T	DQ31T/CQ1T	DQ1T
8A	TI06	VREFB8ANO	IO			DFFIO_RX_127p	DFFIO_TX_127p	A19	B16	DO11T	DQ6T	DQ3T	DQ1T	DQ3T			
8A	TI06	VREFB8ANO	IO			DFFIO_RX_127p	DFFIO_TX_127p	F19	D15	DQ3n11T	DQ6T	DQ3T	DQ1T	DQ3n5T			
8A	TI06	VREFB8ANO	IO			DFFIO_RX_128p	DFFIO_TX_128p	D19	A20								
8A	TI06	VREFB8ANO	IO			DFFIO_RX_128p	DFFIO_TX_128p	A21	C19	DO11T	DQ6T	DQ3T	DQ1T	DQ3T			
8A	TI06	VREFB8ANO	IO			DFFIO_RX_128p	DFFIO_TX_128p	C19	A19	DO11T	DQ6T	DQ3T	DQ1T	DQ3T			
8A	TI06	VREFB8ANO	IO			DFFIO_RX_128p	DFFIO_TX_128p	A20	D19	DO11T	DQ6T	DQ3T	DQ1T	DQ3T			
8A	TI06	VREFB8ANO	IO			DFFIO_RX_129p	DFFIO_TX_129p	C21	D17	DO10T	DQ5T	DQ3T	DQ1T	DQ4T			
8A	TI06	VREFB8ANO	IO			DFFIO_RX_129p	DFFIO_TX_129p	K20	L15								
8A	TI06	VREFB8ANO	IO			DFFIO											



Bank number	IO Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with no OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)	
8A	TIO4	VREFBBAND	IO			DIFFIO_TX_T36n	DIFFIN_T36n*	E07	E04	DQSnB	DQSn4T/DQ4T	DQSn2T/DQ2T	DQ1T	DQSn2T	DQSn1T/DQ1T			
8A	TIO4	VREFBBAND	IO			DIFFIO_RX_T36p	DIFFOUT_T36p	G03	F21									
8A	TIO4	VREFBBAND	IO			DIFFIO_TX_T36p	DIFFIN_T36p*	G23	K18	DQ3Y1	DQ4T/CO4T	DQ2T/CO2T	DQ1T	DQ3S1T	DQ1T/CO1T			
8A	TIO4	VREFBBAND	IO			DIFFIO_RX_T36n	DIFFOUT_T36n	G24	E21	DQ4T	DQ4T	DQ2T	DQ1T	DQ3S1T	DQ1T			
8A	TIO4	VREFBBAND	IO			DIFFIO_TX_T36n	DIFFIN_T36n*	F23	J17	DQ3nY1T	DQ4T	DQ2T	DQ1T	DQ3Sn1T	DQ1T			
8A	TIO4	VREFBBAND	IO		CRC_ERROR	DIFFIO_RX_T36p	DIFFOUT_T36p	F24	E19									
8A	TIO4	VREFBBAND	IO			DIFFIO_TX_T36p	DIFFIN_T36p*	G04	G19	DQ4T	DQ4T	DQ2T	DQ1T	DQ4S1T	DQ1T			
8A	TIO4	VREFBBAND	IO			DIFFIO_RX_T36n	DIFFOUT_T36n	G04	E18	DQ4T	DQ4T	DQ2T	DQ1T	DQ4S1T	DQ1T			
8A	TIO4	VREFBBAND	IO			DIFFIO_TX_T36n	DIFFIN_T36n*	G25	G18	DQ4T	DQ4T	DQ2T	DQ1T	DQ4S1T	DQ1T			
8A	TIO3	VREFBBAND	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	F21		DQ6T	DQ3T	DQ2T	DQ1T					
8A	TIO3	VREFBBAND	IO			DIFFIO_TX_T37n	DIFFIN_T37n*	N00										
8A	TIO3	VREFBBAND	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	E21		DQ6T	DQ3T	DQ2T	DQ1T					
8A	TIO3	VREFBBAND	IO			DIFFIO_TX_T37n	DIFFIN_T37n*	M00		DQ6T	DQ3T	DQ2T	DQ1T					
8A	TIO3	VREFBBAND	IO			DIFFIO_RX_T38p	DIFFOUT_T38p	G07										
8A	TIO3	VREFBBAND	IO			DIFFIO_TX_T38p	DIFFIN_T38p*	G25		DQ6T	DQ3T/CO3T	DQ2T	DQ1T					
8A	TIO3	VREFBBAND	IO			DIFFIO_RX_T38n	DIFFOUT_T38n	C27		DQ6T	DQ3T	DQ2T	DQ1T					
8A	TIO3	VREFBBAND	IO			DIFFIO_TX_T38n	DIFFIN_T38n*	C26		DQ6nE1	DQ3n3T/CO3T	DQ2T	DQ1T					
8A	TIO3	VREFBBAND	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	E22										
8A	TIO3	VREFBBAND	IO			DIFFIO_TX_T39p	DIFFIN_T39p*	M1		DQ3S1T	DQ3T/CO3T	DQ2T	DQ1T					
8A	TIO3	VREFBBAND	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	G22		DQ3T	DQ3T	DQ2T	DQ1T					
8A	TIO3	VREFBBAND	IO			DIFFIO_TX_T39n	DIFFIN_T39n*	G22		DQ3nE1T	DQ3T	DQ2T	DQ1T					
8A	TIO3	VREFBBAND	IO			DIFFIO_RX_T40p	DIFFOUT_T40p	G29										
8A	TIO3	VREFBBAND	IO			DIFFIO_TX_T40p	DIFFIN_T40p*	C30		DQ5T	DQ3T	DQ2T	DQ1T					
8A	TIO3	VREFBBAND	IO			DIFFIO_RX_T40n	DIFFOUT_T40n	G28		DQ5T	DQ3T	DQ2T	DQ1T					
8A	TIO3	VREFBBAND	IO			DIFFIO_TX_T40n	DIFFIN_T40n*	C29		DQ5T	DQ3T	DQ2T	DQ1T					
8A	VREFBBAND	IO		RUP2				E25	L21									
8A	VREFBBAND	IO		PLL1_CLKOUT1p				M21	K19									
8A	VREFBBAND	IO		RDN2				G26	K21									
8A	VREFBBAND	IO		PLL1_CLKOUT1m				L21	J18									
8A	VREFBBAND	IO		PLL1_CLKOUT2p				F26	F20									
8A	VREFBBAND	IO		PLL1_CLKOUT3p				K21	J19									
8A	VREFBBAND	IO		PLL1_CLKOUT2m				F25	F19									
8A	VREFBBAND	IO		PLL1_CLKOUT3m				J21	F19									
8B	TIO2	VREFBBAND	IO			DIFFIO_RX_T41p	DIFFOUT_T41p	G25		DQ4T	DQ2T	DQ1T						
8B	TIO2	VREFBBAND	IO			DIFFIO_TX_T41p	DIFFIN_T41p*	K23										
8B	TIO2	VREFBBAND	IO			DIFFIO_RX_T41n	DIFFOUT_T41n	G24		DQ4T	DQ2T	DQ1T						
8B	TIO2	VREFBBAND	IO			DIFFIO_TX_T41n	DIFFIN_T41n*	J22		DQ4T	DQ2T	DQ1T						
8B	TIO2	VREFBBAND	IO			DIFFIO_RX_T42p	DIFFOUT_T42p	J27										
8B	TIO2	VREFBBAND	IO			DIFFIO_TX_T42p	DIFFIN_T42p*	M27		DQ34T	DQ32T/CO2T	DQ31T/CO1T						
8B	TIO2	VREFBBAND	IO			DIFFIO_RX_T42n	DIFFOUT_T42n	J28		DQ4T	DQ2T	DQ1T						
8B	TIO2	VREFBBAND	IO			DIFFIO_TX_T42n	DIFFIN_T42n*	G26		DQ3n4T	DQ3n2T/DQ32T	DQ3n1T/DQ31T						
8B	TIO2	VREFBBAND	IO			DIFFIO_RX_T43p	DIFFOUT_T43p	G28										
8B	TIO2	VREFBBAND	IO			DIFFIO_TX_T43p	DIFFIN_T43p*	L22		DQ33T	DQ2T/CO2T	DQ1T/CO1T						
8B	TIO2	VREFBBAND	IO			DIFFIO_RX_T43n	DIFFOUT_T43n	G27		DQ3T	DQ2T	DQ1T						
8B	TIO2	VREFBBAND	IO			DIFFIO_TX_T43n	DIFFIN_T43n*	E22		DQ3n3T	DQ3T	DQ1T						
8B	TIO2	VREFBBAND	IO			DIFFIO_RX_T44p	DIFFOUT_T44p	L28										
8B	TIO2	VREFBBAND	IO			DIFFIO_TX_T44p	DIFFIN_T44p*	F27		DQ3T	DQ2T	DQ1T						
8B	TIO2	VREFBBAND	IO			DIFFIO_RX_T44n	DIFFOUT_T44n	K28		DQ3T	DQ3T	DQ1T						
8B	TIO2	VREFBBAND	IO			DIFFIO_TX_T44n	DIFFIN_T44n*	E27		DQ3T	DQ2T	DQ1T						
8B	TIO1	VREFBBAND	IO			DIFFIO_RX_T45p	DIFFOUT_T45p	J27		DQ2T	DQ1T	DQ1T						
8B	TIO1	VREFBBAND	IO			DIFFIO_TX_T45p	DIFFIN_T45p*	K24										
8B	TIO1	VREFBBAND	IO			DIFFIO_RX_T45n	DIFFOUT_T45n	F28		DQ2T	DQ1T	DQ1T						
8B	TIO1	VREFBBAND	IO			DIFFIO_TX_T45n	DIFFIN_T45n*	J24		DQ2T	DQ1T	DQ1T						
8B	TIO1	VREFBBAND	IO			DIFFIO_RX_T46p	DIFFOUT_T46p	G30										
8B	TIO1	VREFBBAND	IO			DIFFIO_TX_T46p	DIFFIN_T46p*	F30		DQ2T	DQ1T	DQ1T						
8B	TIO1	VREFBBAND	IO			DIFFIO_RX_T46n	DIFFOUT_T46n	F30		DQ3n2T	DQ3n1T/CO1T	DQ1T						
8B	TIO1	VREFBBAND	IO			DIFFIO_TX_T46n	DIFFIN_T46n*	F28										
8B	TIO1	VREFBBAND	IO			DIFFIO_RX_T47p	DIFFOUT_T47p	J25		DQ31T	DQ1T/CO1T	DQ1T						
8B	TIO1	VREFBBAND	IO			DIFFIO_TX_T47p	DIFFIN_T47p*	E28		DQ1T	DQ1T	DQ1T						
8B	TIO1	VREFBBAND	IO			DIFFIO_RX_T47n	DIFFOUT_T47n	M04		DQ3n1T	DQ1T	DQ1T						
8B	TIO1	VREFBBAND	IO			DIFFIO_TX_T47n	DIFFIN_T47n*	G29		DQ1T	DQ1T	DQ1T						
8B	TIO1	VREFBBAND	IO			DIFFIO_RX_T48p	DIFFOUT_T48p	E30		DQ1T	DQ1T	DQ1T						
8B	TIO1	VREFBBAND	IO			DIFFIO_TX_T48p	DIFFIN_T48p*	F29		DQ1T	DQ1T	DQ1T						
8B	TIO1	VREFBBAND	IO			DIFFIO_RX_T48n	DIFFOUT_T48n	G30										
8C			TDO		TDO			M27	L23									
8C			ASD0		ASD0			K27	E22									
8C			ACS0		ACS0			M26	H22									
8C			DAT0A		DAT0A			M26	K22									
8C			TR0		TR0			M25	H24									
8C			TMS		TMS			M25	J23									
8C			TCK		TCK			L24	L24									
8C			DCLK		DCLK			L25	K24									
			GND					U17	P14									
			GND					AD27	AB21									
			GND					M28	G23									
			GND					N27	K23									
			GND					Y34	Y28									
			GND					Y33	Y27									
			GND					Y30	W26									
			GND					Y29	W25									
			GND					Y27	V29									
			GND					Y26	V27									
			GND					W32	U26									
			GND					W31	U25									
			GND					W28	T28									
			GND					W26	T27									
			GND					V34	T24									
			GND					V33	T22									
			GND					V30	R26									
			GND					V29	R25									
			GND					V27	R23									
			GND					V25	R21									
			GND					U32	P28									
			GND					U31	P27									
			GND					U28	P24									
			GND					U26	P22									
			GND					T34	N28									
			GND					T33	N25									
			GND					T30	N23									
			GND					T29	N21									
			GND					T27	M28									
			GND					T25	M27									
			GND					R30	M24									
			GND					R31	L26									
			GND					R28	L25									



Bank number	IO Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)
			GND					R25	R25								
			GND					P34	A27								
			GND					P33	J26								
			GND					P30	J25								
			GND					P29	T28								
			GND					P28	H27								
			GND					P26	G26								
			GND					M32	G25								
			GND					M31	F28								
			GND					M34	F27								
			GND					M33	E26								
			GND					M30	E25								
			GND					M29	G28								
			GND					L32	D27								
			GND					L31	D24								
			GND					K34	D22								
			GND					K33	C26								
			GND					K30	C25								
			GND					K29	C24								
			GND					K32	C22								
			GND					J31	B28								
			GND					H34	B27								
			GND					H33	B25								
			GND					G32	B23								
			GND					G31	B22								
			GND					F34	B21								
			GND					F33	AH28								
			GND					E32	AH24								
			GND					E31	AH20								
			GND					D34	AH20								
			GND					D33	AG28								
			GND					C34	AG26								
			GND					C31	AG24								
			GND					B34	AG22								
			GND					B33	AG21								
			GND					B30	AG20								
			GND					B29	AF28								
			GND					B28	AF27								
			GND					AP33	AF28								
			GND					AP32	AF25								
			GND					AP30	AF23								
			GND					AN32	AE26								
			GND					AN31	AE25								
			GND					AN30	AE23								
			GND					AM34	AH28								
			GND					AM33	AD27								
			GND					AL32	AC26								
			GND					AL31	AC25								
			GND					AK34	AB28								
			GND					AK33	AB27								
			GND					AK32	AK28								
			GND					AL31	AA25								
			GND					AH34	A27								
			GND					AH33	A26								
			GND					AG32	A23								
			GND					AG31	A21								
			GND					AF34	V7								
			GND					AF33	W9								
			GND					AF30	W22								
			GND					AF29	W19								
			GND					AE32	W17								
			GND					AE31	W15								
			GND					AD34	V8								
			GND					AD33	V5								
			GND					AD30	V20								
			GND					AD29	V2								
			GND					AC32	V18								
			GND					AC31	V16								
			GND					AB34	V14								
			GND					AB33	V12								
			GND					AB30	V10								
			GND					AB29	U9								
			GND					AA32	U17								
			GND					AA32	U13								
			GND					AA31	T8								
			GND					AA28	T20								
			GND					AA26	T18								
			GND					A33	T14								
			GND					A32	T10								
			GND					A31	R19								
			GND					A30	R13								
			GND					A28	P18								
			GND					V23	P12								
			GND					V21	N9								
			GND					V19	N5								
			GND					V17	N18								
			GND					V15	N15								
			GND					V13	N11								
			GND					W8	W16								
			GND					W5	M12								
			GND					W22	L8								
			GND					W20	L20								
			GND					W2	L17								
			GND					W18	L11								
			GND					W16	H8								
			GND					W14	H17								
			GND					W11	G9								
			GND					V23	E20								
			GND					V21	E11								
			GND					V19	B2								
			GND					V15	AG8								
			GND					V13	AG14								
			GND					U22	AD20								
			GND					U20	AD17								
			GND					U18	AA20								
			GND					U16	AA11								



Bank number	IO Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)
			GND					AK4									
			GND					AK8									
			GND					AK20									
			GND					AK23									
			GND					AG2									
			GND					AG14									
			GND					AF9									
			GND					AD8									
			GND					AD26									
			GND					AD20									
			GND					AD17									
			GND					AB23									
			GND					AB19									
			GND					AB15									
			GND					AA5									
			GND					AA20									
			GND					AA14									
			GND					AA8									
			GND					AA22									
			GND					AA16									
			GND					AA18									
			VCC					V16	P15								
			VCC					V24	W20								
			VCC					V22	W18								
			VCC					V20	W16								
			VCC					V18	W14								
			VCC					V16	W9								
			VCC					V14	W21								
			VCC					W23	V19								
			VCC					W21	V17								
			VCC					W19	V15								
			VCC					W17	V13								
			VCC					W15	V11								
			VCC					W13	U20								
			VCC					V24	U18								
			VCC					V22	U16								
			VCC					V20	U14								
			VCC					V18	U12								
			VCC					V14	U10								
			VCC					U21	T9								
			VCC					U19	T19								
			VCC					U15	T17								
			VCC					U13	T15								
			VCC					U24	T13								
			VCC					T22	T11								
			VCC					T20	R18								
			VCC					T18	R16								
			VCC					T16	R14								
			VCC					T14	R12								
			VCC					R23	R10								
			VCC					R21	P9								
			VCC					R19	P19								
			VCC					R17	P17								
			VCC					R15	P13								
			VCC					R13	P11								
			VCC					P24	N20								
			VCC					P22	N18								
			VCC					P20	N16								
			VCC					P18	N14								
			VCC					P16	N12								
			VCC					P14	N10								
			VCC					P12	M8								
			VCC					N23	W20								
			VCC					N21	M19								
			VCC					N17	M17								
			VCC					N15	M15								
			VCC					N13	M13								
			VCC					AK23	M11								
			VCC					AK24	L18								
			VCC					AB22	L16								
			VCC					AB20	L13								
			VCC					AB18	L12								
			VCC					AB16	L10								
			VCC					AB14	K17								
			VCC					AB12									
			VCC					AA23									
			VCC					AA21									
			VCC					AA19									
			VCC					AA17									
			VCC					AA15									
			VCC					AA13									
			DN1					K26	H23								
			DN1					V17	R15								
			DN1					CA	P8								
			VCCBAT					L27	J24								
			VCCA_PLL_1					H25	G20								
			VCCA_PLL_2					J10	H8								
			VCCA_PLL_3					AF10	V8								
			VCCA_PLL_4					AG25	AB20								
			VCCA_PLL_5					T9	P8								
			VCCA_PLL_6					W9	R7								
			VCCD_PLL_1					J26	H21								
			VCCD_PLL_2					K9	G8								
			VCCD_PLL_3					AF9	AV7								
			VCCD_PLL_4					AF26	AA21								
			VCCD_PLL_5					UB	P7								
			VCCD_PLL_6					V8	R8								
			VCCIO3A					AM20	AG16								
			VCCIO3A					AK24	AD19								
			VCCIO3A					AK20	AD16								
			VCCIO3A					AF22									
			VCCIO3B					AF21									
			VCCIO3C					AD25	AC20								
			VCCIO4A					AM14	AG7								



Bank number	IO Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)
			VCCIOA4					AG17	AG10								
			VCCIOA4					AG17	AD13								
			VCCIOA4					AL14	AD10								
			VCCIO4B					AH11									
			VCCIO4B					AJ8									
			VCCIO5A					AG3	I2								
			VCCIO5A					AD3	U2								
			VCCIO5A					AA6	R2								
			VCCIO5A					AA3	AE2								
			VCCIO5B					AA5									
			VCCIO5B					AH8									
			VCCIO5A					I16	K2								
			VCCIO5A					I3	G2								
			VCCIO6A					P3	D2								
			VCCIO6A					L3									
			VCCIO6B					L6									
			VCCIO6B					H6									
			VCCIO7A					F14	B7								
			VCCIO7A					F11	B4								
			VCCIO7A					G14	B13								
			VCCIO7A					G11	B10								
			VCCIO7B					G8									
			VCCIO7B					G8									
			VCCIO8A					F22	F18								
			VCCIO8A					F20	F16								
			VCCIO8A					C23	C20								
			VCCIO8A					C20	B18								
			VCCIO8B					G17									
			VCCIO8B					G23									
			VCCIO8B					H22									
			VCCIO8C					K26	G23								
			VCCPD3A					AC20	AB18								
			VCCPD3A					AC19	AA18								
			VCCPD3B					AC21									
			VCCPD3C					AC24	Y21								
			VCCPD4A					AD16	AA13								
			VCCPD4A					AC16	AA12								
			VCCPD4B					AC13									
			VCCPD5A					Y12	U8								
			VCCPD5A					AA12	U7								
			VCCPD5B					AC12									
			VCCPD6A					T12	M8								
			VCCPD6A					R12	M7								
			VCCPD6B					M11									
			VCCPD7A					M15	J13								
			VCCPD7A					M14	H13								
			VCCPD7B					L12									
			VCCPD8A					M19	H16								
			VCCPD8A					L19	G16								
			VCCPD8B					M22									
			VCCPD8C					M24	G21								
3A	VREFB3A0		VREFB3A0	VREFB3A0				AE20	Y17								
3B	VREFB3B0		VREFB3B0	VREFB3B0				AE22									
4A	VREFB4A0		VREFB4A0	VREFB4A0				AD15	AB12								
4B	VREFB4B0		VREFB4B0	VREFB4B0				AD13									
5A	VREFB5A0		VREFB5A0	VREFB5A0				AB11	W7								
5B	VREFB5B0		VREFB5B0	VREFB5B0				AD11									
6A	VREFB6A0		VREFB6A0	VREFB6A0				M11	L9								
6B	VREFB6B0		VREFB6B0	VREFB6B0				M12									
7A	VREFB7A0		VREFB7A0	VREFB7A0				L15	H12								
7B	VREFB7B0		VREFB7B0	VREFB7B0				K13	H18								
8A	VREFB8A0		VREFB8A0	VREFB8A0				K19	H18								
8B	VREFB8B0		VREFB8B0	VREFB8B0				M23									
			NC					AL30	AF21								
			NC					AM30	AF22								
			VCCL_GXB					V28	P23								
			VCCL_GXB					V26	P21								
			VCCL_GXB					V27	N24								
			VCCL_GXB					U25	N22								
			VCCL_GXB					T28	M23								
			VCCL_GXB					T26	T23								
			VCCL_GXB					R27	T21								
			VCCL_GXB					R25	R24								
			VCCL_GXB					V28									
			VCCL_GXB					V26									
			VCCL_GXB					V27									
			VCC0B					U23	Y15								
			VCC0B					J12	N7								
			VCC0B					L18	J15								
			VCC0B					AD16	P20								
			RREF0					AP31	AA21								
			RREF1					A29	A22								
			VCCA					U24	R20								
			VCCA					R24	M21								
			VCCA					AA24	U21								
			VCCA					W24									
			VCC0H_GXB					P27	U23								
			VCC0H_GXB					N28	U22								
			VCC0H_GXB					AB25	M22								
			VCC0H_GXB					AA27	L22								

- Notes:
(1) An IO module is a group of 16 IO pins.
(2) When not used as DIFFIN or DIFFIO, TX, all pins marked with * (DIFFIN_#pin) can be configured as emulated LVDS output channels (DIFFOUT). Only DIFFIN pins of the same index group (e.g DIFFIN_B1p and DIFFIN_B1n) can be used to form an emulated LVDS output channel.
(3) When not used as clocks, the CQn and DQSn pins can be used as DQ pins.



Pin Name	Pin Type (1st and 2nd Function)	Pin Description
Clock and PLL Pins		
CLK[4:15]	Clock, Input	Single ended clock input pin.
DIFFCLK[0:5]p	Clock, Input	Clock input pin for differential clock input. OCT Rd is not supported.
DIFFCLK[0:5]n	Clock, Input	Negative clock input for differential clock input. OCT Rd is not supported.
PLL_[1:4]_CLKOUT1p	I/O, Clock	PLL[1:4]_CLKOUT1 (except PLL1 and PLL3 in EP2AGX125 and EP2AGX260) supports 2 clock I/O pins, configured either as one single ended I/O or one differential I/O pair. PLL1 and PLL3 in EP2AGX125 and EP2AGX260 support 6 clock I/O pins, configured either as 3 single ended I/Os or 3 differential I/O pairs.
PLL_[1:4]_CLKOUT1n	I/O, Clock	
PLL_[1,3]_CLKOUT[2:3]p (Note 4)	I/O, Clock	PLL1 and PLL3 in EP2AGX125 and EP2AGX260 support 6 clock I/O pins, configured either as 3 single ended I/Os or 3 differential I/O pairs.
PLL_[1,3]_CLKOUT[2:3]n (Note 4)	I/O, Clock	
Dedicated Configuration/JTAG Pins		
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (nCSCO, ASDO, DATA[7:0], CLKUSR, INIT_DONE, DEV_OE, DEV_CLRn) are on or off before and during configuration. A logic high (1.5V, 1.8V, 2.5V, 3.0V or 3.3V) turns off the weak pull-up, while a logic low turns them on.
MSEL[0:3]	Input	Configuration input pins that set the FPGA device configuration scheme.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user-mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration done pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin.
nCEO	I/O, Output (open-drain)	Output that drives low when device configuration is complete. This pin can be used as a regular I/O if not used for device configuration.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as a user I/O pin.
TCK	Input	Dedicated JTAG test clock input pin.
TMS	Input	Dedicated JTAG test mode select input pin.
TDI	Input	Dedicated JTAG test data input pin.
TDO	Output	Dedicated JTAG test data output pin.
Optional/Dual-Purpose Configuration Pins		
nCSCO	Output	Dedicated output control signal from the FPGA to the serial configuration device in AS mode that enables the configuration device.
ASDO	Output	Control signal from the FPGA to the serial configuration device in AS mode used to read out configuration data.
DCLK	I/O (PS, FPP) Output (AS)	Dedicated configuration clock pin. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into the FPGA. In AS mode, DCLK is an output from the FPGA that provides timing for the configuration interface.
CRC_ERROR	I/O, Output (open-drain)	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled. This pin can be used as regular I/O if not used for CRC error detection.
DEV_CLRn	I/O, Input	Optional pin that allows designers to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed.
DEV_OE	I/O, Input	Optional pin that allows designers to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
DATA0	Input	DATA[0] is a dedicated pin that is used for both the passive and active configuration modes.
DATA[1:7]	I/O, Input	Dual-purpose configuration input data pins. The DATA[0:7] pins can be used for byte-wide configuration. DATA[1:7] pins can also be used as user I/O pins after configuration, but not DATA0.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin.
Differential I/O Pins		
DIFFIO_RX_[T,B,R][##]p, DIFFIO_RX_[T,B,R][##]n	I/O, RX channel	These are true LVDS receiver channels with OCT Rd support. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX_[T,B,R][##]p, DIFFIO_TX_[T,B,R][##]n	I/O, TX channel	These are true LVDS transmitter channels. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used as true LVDS transmitter channels, these pins can be configured as true LVDS receiver channels without OCT Rd support (DIFFIN_[T,B,R][##][p,n]). If not used for differential signaling, these pins are available as user I/O pins.
DIFFIN_[T,B,R][##]p, DIFFIN_[T,B,R][##]n	I/O, RX channel	These are true LVDS receiver channels without OCT Rd support. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used as true LVDS receiver channels without OCT Rd support, these pins can be configured as true LVDS transmitter channels (DIFFIO_TX_[T,B,R][##][p,n]). If not used for differential signaling, these pins are available as user I/O pins.
DIFFOUT_[##]p, DIFFOUT_[##]n	I/O, TX channel	These are emulated LVDS output channels. On I/O banks, there are true LVDS input buffers but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, (DIFFIO_RX_[T,B,R][##][p,n], DIFFIN_[T,B,R][##][p,n]) can be configured as emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
External Memory Interface Pins		
DQS[##][T,B,R]	I/O, DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.
DQSn[##][T,B,R] (Note 5)	I/O, DQS	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.
DQ[##][T,B,R]	I/O, DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
CQ[##][T,B,R]	DQS	Optional data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.
CQn[##][T,B,R] (Note 5)	DQS	Optional complementary data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.
Reference Pins		
RUP[0:2]	I/O, Input	Reference pins for I/O banks. The RUP pins share the same VCCIO with the I/O bank where they are located. The external precision resistor RUP must be connected to the designated RUP pin within the bank. If not required, this pin is a regular I/O pin.
RDN[0:2]	I/O, Input	Reference pins for I/O banks. The RDN pins share the same GND with the I/O bank where they are located. The external precision resistor RDN must be connected to the designated RDN pin within the bank. If not required, this pin is a regular I/O pin.
DNU	Do Not Use	Do Not Use (DNU).
NC	No Connect	Do not drive signals into these pins.



Pin Name	Pin Type (1st and 2nd Function)	Pin Description
Supply Pins		
VCC	Power	VCC supplies power to the core and periphery.
VCCD_PLL[1:6]	Power	Digital power for PLL[1:6]. All of these pins must be connected even if the PLL is not used
VCCCB	Power	Configuration RAM bits power supply.
VCCA_PLL[1:6]	Power	Analog power for PLL [1:6]. All of these pins must be connected even if the PLL is not used
VCCIO[3:8][A,B]	Power	These are I/O supply voltage pins for banks 3 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all LVDS, LVCMOS(1.2V, 1.5V, 1.8V, 2.5V, 3.0V, 3.3V), HSTL(12,15,18), SSTL(15,18,2), 3.0V PCI/PCI-X I/O as well as LVTTTL (1.8V, 2.5V, 3.0V, 3.3V) I/O standards. VCCIO also supplies power to the input buffers used for LVCMOS(1.2V, 1.5V, 1.8V, 2.5V, 3.0V, 3.3V), 3.0V PCI/PCI-X and LVTTTL (1.8V, 2.5V, 3.0V, 3.3V) I/O standards.
VCCIO[3,8]C	Power	These are configuration and JTAG supply voltage pins for banks 3C and 8C. Each bank can support a different voltage level. For AS/PP/FPP configuration schemes, VCCIO8C supports 1.8V, 2.5V, 3.0V or 3.3V. JTAG can support 1.5V, 1.8V, 2.5V, 3.0V or 3.3V.
VCCPD[3:8][A,B], VCCPD[3,8]C	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers and the input buffers for HSTL/SSTL input buffers. This can be connected to 3.3V, 3.0V or 2.5V. For 3.3V I/O standard connect VCCPD to 3.3V, for 3.0V I/O standard connect VCCPD to 3.0V and for 2.5V/1.8V/1.2V I/O standards connect VCCPD to 2.5V
VCCBAT	Power	Battery back-up power supply for design security volatile key register.
GND	Ground	Device ground pins.
VREF[3:8][A,B]N0	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. These pins cannot be used as regular I/Os.
Transceiver Pins		
VCCL_GXB	Power	Supplies power to the transceiver PMA TX, PMA RX and clocking.
VCCH_GXB	Power	Supplies power to the transceiver PMA output (TX) buffer.
VCCA	Power	Supplies power to the transceiver PMA regulator.
GXB_RX[0:15]p (Note 6)	Input	High speed positive differential receiver channels.
GXB_RX[0:15]n (Note 6)	Input	High speed negative differential receiver channels.
GXB_TX[0:15]p (Note 6)	Output	High speed positive differential transmitter channels.
GXB_TX[0:15]n (Note 6)	Output	High speed negative differential transmitter channels.
REFCLK[0:7]p	Input	High speed differential reference clock positive.
REFCLK[0:7]n	Input	High speed differential reference clock complement.
RREF[0:1]	Input	Reference resistor for transceiver.

Notes:

1. Refer to the Arria II GX Device Datasheet and Pin Connection Guidelines for the recommended operating conditions.
2. This pin definition is prepared based on the EP2AGX260.
3. Some of the pull-up /pull down resistors mentioned in the table above may not be required, depending on the exact device configuration scheme.
The ability to NC or short them may be valuable during the debug phase, should you be required to use a different configuration scheme.
Refer to the Configuring Arria II GX Devices chapter in the Arria II GX Device Handbook for more information.
4. PLL[1,3]_CLKOUT[2..3][p,n] are only available in PLL1 and PLL3 in EP2AGX125 and EP2AGX260.
5. When not used as clocks, the CQn and DQSn pins can be used as DQ pin.
6. Transceiver signals GXB_RX[15..0] and GXB_TX[15..0] are device specific.

PLL_1	8C	8B	8A	7A	7B	PLL_2	
		VREFB8BN0	VREFB8AN0	VREFB7AN0	VREFB7BN0		
Transceiver Block (QL3)						6B	VREFB6BN0
Transceiver Block (QL2)						6A	VREFB6AN0
Transceiver Block (QL1)						PLL_5	
Transceiver Block (QL0)						PLL_6	
PLL_4	3C	3B	3A	4A	4B	PLL_3	
		VREFB3BN0	VREFB3AN0	VREFB4CN0	VREFB4BN0		
						5A	VREFB5AN0
						5B	VREFB5BN0

This is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only.



Pin Information for the Arria[®] II GX EP2AGX260 Device
Version 1.1

Version Number	Date	Changes Made
1.0	2/27/2009	Initial release.
1.1	5/29/2009	Added DNU in Pin List and Pin Definitions.