



Bank number	IO Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F1152	F780	F572	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note 3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)	DQS for X4 for F572	DQS for X8/X9 for F572 (Note 3)	DQS for X16/X18 for F572 (Note 3)		
Q12			XVB TX11a					K32	C23														
Q12			XVB TX11b					K31	C23														
Q12			XVB RX11a					L34	A24														
Q12			XVB RX11b					L33	B24														
Q12			XVB TX10a					M32	A26														
Q12			XVB TX10b					M31	B26														
Q12			XVB RX10a					N34	C28														
Q12			XVB RX10b					N33	C27														
Q12			REFCLK9p					N30	D28														
Q12			REFCLK9n					O28	D28														
Q12			REFCLK20p					O30	E28														
Q12			REFCLK20n					O28	E27														
Q12			XVB TX3a					P26	F26														
Q12			XVB TX3b					P27	F26														
Q12			XVB RX3a					S34	G28														
Q12			XVB RX3b					S33	G27														
Q12			XVB TX5a					T24	H26														
Q12			XVB TX5b					T31	H26														
Q12			XVB RX5a					U34	J28														
Q12			XVB RX5b					U33	J27														
Q12			XVB TX7a					V32	K28	B22													
Q12			XVB TX7b					V31	K25	B21													
Q12			XVB RX7a					W34	L28	C24													
Q12			XVB RX7b					W33	L27	C23													
Q12			XVB TX9a					Y32	M26	D22													
Q12			XVB TX9b					Y31	M25	D21													
Q12			XVB RX9a					AA34	N28	E24													
Q12			XVB RX9b					AA33	N27	E23													
Q12			REFCLK9p					AP30	Q28	F22													
Q12			REFCLK9n					AP29	Q25	F21													
Q12			REFCLK16p					AA30	R28	G24													
Q12			REFCLK16n					AA29	R27	G23													
Q12			XVB TX5a					AB32	I26	H22													
Q12			XVB TX5b					AB31	I25	H21													
Q12			XVB RX5a					AC34	L28	J24													
Q12			XVB RX5b					AC33	L27	J23													
Q12			XVB TX4a					AD32	M26	K22													
Q12			XVB TX4b					AD31	M25	K21													
Q12			XVB RX4a					AE34	N28	L24													
Q12			XVB RX4b					AE33	N27	L23													
Q12			XVB TX3a					AF32	Y26	M22													
Q12			XVB TX3b					AF31	Y25	M21													
Q12			XVB RX3a					AG34	AA28	N24													
Q12			XVB RX3b					AG33	AA27	N23													
Q12			XVB TX2a					AH32	AB26	P22													
Q12			XVB TX2b					AH31	AB25	P21													
Q12			XVB RX2a					AJ34	AC28	R24													
Q12			XVB RX2b					AJ33	AC27	R23													
Q12			REFCLK9p					AK30	AD26	T22													
Q12			REFCLK9n					AK29	AD25	T21													
Q12			REFCLK20p					AE30	AE28	U24													
Q12			REFCLK20n					AE29	AE27	U23													
Q12			XVB TX1a					AK32	AH27	V22													
Q12			XVB TX1b					AK31	AH26	V21													
Q12			XVB RX1a					AL34	AE25	W24													
Q12			XVB RX1b					AL33	AE24	W23													
Q12			XVB TX0a					AM32	AE24	V22													
Q12			XVB TX0b					AM31	AE24	V21													
Q12			XVB RX0a					AN34	AF28	AA24													
Q12			XVB RX0b					AN33	AF27	AA23													
SC			HC0NF0G		HC0NF0G			AC26	AA24	V20													
SC			ZONE_DONE		ZONE_DONE			AE25	AA23	W20													
SC			MSEL3		MSEL3			AB26	AB24	T20													
SC			MSEL2		MSEL2			AD34	V24	W20													
SC			MSEL1		MSEL1			AC25	Y23	I19													
SC			MSEL0		MSEL0			AC27	W24	I19													
SC			HSTATUS		HSTATUS			AD28	AC23	U18													
SC			NO_PULLUP		NO_PULLUP			AC29	AB22	U19													
SC								AE25	AA22	U18													
SC								AH25	U24	Y16													
SA			VREFBAND		PLL4_CLKOUT1a			AE27	AB19	AB20													
SA			VREFBAND		RWD			AH24	V24	Y16													
SA			VREFBAND		RLUPD			AL26	AC19	AA20													
SA	BD1	VREFBAND	IO			DIFFIO_TX_B1a	DIFFIN_B1a	AM28	AB24	AB20	DO2B									DO2B			
SA	BD1	VREFBAND	IO			DIFFIO_RX_B1a	DIFFOUT_B1a	AM28	AB24	AB20	DO2B										DO2B		
SA	BD1	VREFBAND	IO			DIFFIO_TX_B1p	DIFFIN_B1p	AL29	AB21	AB20	DO2B										DO2B		
SA	BD1	VREFBAND	IO			DIFFIO_RX_B1p	DIFFOUT_B1p	AL29	AB21	AB20	DO2B										DO2B		
SA	BD1	VREFBAND	IO			DIFFIO_TX_B0a	DIFFIN_B0a	AL26	AB18	DO2B11B	DO2B												
SA	BD1	VREFBAND	IO			DIFFIO_RX_B0a	DIFFOUT_B0a	AL26	AB18	DO2B11B	DO2B												
SA	BD1	VREFBAND	IO			DIFFIO_TX_B0p	DIFFIN_B0p	AL24	AB18	DO2B11B	DO2B												
SA	BD1	VREFBAND	IO			DIFFIO_RX_B0p	DIFFOUT_B0p	AL24	AB18	DO2B11B	DO2B												
SA	BD1	VREFBAND	IO			DIFFIO_TX_B0a	DIFFIN_B0a	AM27	AB16	DO2B11B	DO2B												
SA	BD1	VREFBAND	IO			DIFFIO_RX_B0a	DIFFOUT_B0a	AM26	AB16	DO2B11B	DO2B												
SA	BD1	VREFBAND	IO			DIFFIO_TX_B0p	DIFFIN_B0p	AM27	AB16	DO2B11B	DO2B												
SA	BD1	VREFBAND	IO			DIFFIO_RX_B0p	DIFFOUT_B0p	AM26	AB16	DO2B11B	DO2B												
SA	BD1	VREFBAND	IO			DIFFIO_TX_B0a	DIFFIN_B0a	AM27	AB16	DO2B11B	DO2B												
SA	BD1	VREFBAND	IO			DIFFIO_RX_B0a	DIFFOUT_B0a	AM26	AB16	DO2B11B	DO2B												
SA	BD1	VREFBAND	IO			DIFFIO_TX_B0p	DIFFIN_B0p	AM27	AB16	DO2B11B	DO2B												
SA	BD1	VREFBAND	IO			DIFFIO_RX_B0p	DIFFOUT_B0p	AM26	AB16	DO2B11B	DO2B												
SA	BD2	VREFBAND	IO			DIFFIO_TX_B0a	DIFFIN_B0a	AM24	AD21	AC21	DO2B									DO4B	DO2B		
SA	BD2	VREFBAND	IO			DIFFIO_RX_B0a	DIFFOUT_B0a	AM23	AC17	AD21	DO2B									DO4B	DO2B		
SA	BD2	VREFBAND	IO			DIFFIO_TX_B0p	DIFFIN_B0p	AL24	AC21	AB21	DO2B									DO4B	DO2B		
SA	BD2	VREFBAND	IO			DIFFIO_RX_B0p	DIFFOUT_B0p	AL23	AB17	AD20	DO2B									DO4B	DO2B		
SA	BD2	VREFBAND	IO		NET_DONE	DIFFIO_TX_B0a	DIFFIN_B0a	AM27	AB16	DO2B11B	DO2B									DO5B4B	DO2B		
SA	BD2	VREFBAND	IO			DIFFIO_RX_B0a	DIFFOUT_B0a	AM27	AB16	DO2B11B	DO2B									DO5B4B	DO2B		
SA	BD2	VREFBAND	IO			DIFFIO_TX_B0p	DIFFIN_B0p	AP27	AC16	AB19	DO2B									DO4B	DO2B		
SA	BD2	VREFBAND	IO			DIFFIO_RX_B0p	DIFFOUT_B0p	AP27	AC16	AB19	DO2B		</										







Bank number	IO Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F152	F780	F572	DQS for X4 for F152	DQS for X8/X9 for F152 (Note 3)	DQS for X16/X18 for F152 (Note 3)	DQS for X32/X36 for F152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)	DQS for X4 for F572	DQS for X8/X9 for F572 (Note 3)	DQS for X16/X18 for F572 (Note 3)	
BA	T104	VREFBAND	CLK15	DIFFCLK_5n				F18	D18	D11												
BA	T104	VREFBAND	CLK14	DIFFCLK_4n				F17	D17	D10												
BA	T104	VREFBAND	CLK13	DIFFCLK_3n				F16	D16	D9												
BA	T104	VREFBAND	CLK12	DIFFCLK_2n				F15	D15	D8												
BA	T104	VREFBAND	CLK11	DIFFCLK_1n				F14	D14	D7												
BA	T104	VREFBAND	CLK10	DIFFCLK_0n				F13	D13	D6												
BA	T104	VREFBAND	CLK9	DIFFCLK_0n				F12	D12	D5												
BA	T104	VREFBAND	CLK8	DIFFCLK_0n				F11	D11	D4												
BA	T104	VREFBAND	CLK7	DIFFCLK_0n				F10	D10	D3												
BA	T104	VREFBAND	CLK6	DIFFCLK_0n				F9	D9	D2												
BA	T104	VREFBAND	CLK5	DIFFCLK_0n				F8	D8	D1												
BA	T104	VREFBAND	CLK4	DIFFCLK_0n				F7	D7	D0												
BA	T104	VREFBAND	CLK3	DIFFCLK_0n				F6	D6	D0												
BA	T104	VREFBAND	CLK2	DIFFCLK_0n				F5	D5	D0												
BA	T104	VREFBAND	CLK1	DIFFCLK_0n				F4	D4	D0												
BA	T104	VREFBAND	CLK0	DIFFCLK_0n				F3	D3	D0												
BA	T104	VREFBAND	CLK0	DIFFCLK_0n				F2	D2	D0												
BA	T104	VREFBAND	CLK0	DIFFCLK_0n				F1	D1	D0												







Bank number (Note 1)	IO Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F1152	F780	F572	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note 3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780 (Note 3)	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)	DQS for X4 for F572	DQS for X8/X9 for F572 (Note 3)	DQS for X16/X18 for F572 (Note 3)	
			GND				E20															
			GND				E17															
			GND				E14															
			GND				E11															
			GND				E8															
			GND				E5															
			GND				E26															
			GND				E23															
			GND				E20															
			GND				E17															
			GND				E14															
			GND				E11															
			GND				E8															
			GND				E5															
			GND				E26															
			GND				E23															
			GND				E20															
			GND				E17															
			GND				E14															
			GND				E11															
			GND				E8															
			GND				E5															
			GND				E26															
			GND				E23															
			GND				E20															
			GND				E17															
			GND				E14															
			GND				E11															
			GND				E8															
			GND				E5															
			GND				E26															
			GND				E23															
			GND				E20															
			GND				E17															
			GND				E14															
			GND				E11															
			GND				E8															
			GND				E5															
			GND				E26															
			GND				E23															
			GND				E20															
			GND				E17															
			GND				E14															
			GND				E11															
			GND				E8															
			GND				E5															
			GND				E26															
			GND				E23															
			GND				E20															
			GND				E17															
			GND				E14															
			GND				E11															
			GND				E8															
			GND				E5															
			GND				E26															
			GND				E23															
			GND				E20															
			GND				E17															
			GND				E14															
			GND				E11															
			GND				E8															
			GND				E5															
			GND				E26															
			GND				E23															
			GND				E20															
			GND				E17															
			GND				E14															
			GND				E11															
			GND				E8															
			GND				E5															
			GND				E26															
			GND				E23															
			GND				E20															
			GND				E17															
			GND				E14															
			GND				E11															
			GND				E8															
			GND				E5															
			GND				E26															
			GND				E23															
			GND				E20															
			GND				E17															
			GND				E14															
			GND				E11															
			GND				E8															
			GND				E5															
			GND				E26															
			GND				E23															
			GND				E20															
			GND				E17															
			GND				E14															
			GND				E11															
			GND				E8															
			GND				E5															
			GND				E26															
			GND				E23															
			GND				E20															
			GND				E17															
			GND				E14															
			GND				E11															
			GND				E8															
			GND				E5															
			GND				E26															
			GND				E23															
			GND				E20															
			GND				E17															
			GND				E14															
			GND				E11															
			GND				E8															
			GND				E5															
			GND				E26															
			GND				E23															
			GND				E20															
			GND				E17															
			GND				E14															
			GND				E11															
			GND				E8															



Bank number	IO Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F1152	F780	F572	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note 3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)	DQS for X4 for F572	DQS for X8/X9 for F572 (Note 3)	DQS for X16/X18 for F572 (Note 3)		
			VCC					AB16	L10														
			VCC					AB17	K17														
			VCC					AB12															
			VCC					AA21															
			VCC					AA19															
			VCC					AA17															
			VCC					AA15															
			VCC					AA13															
			DN0					C25	H23	G18													
			DN0					V17	R15	N12													
			DN0					G4	F5	D5													
			VCCBAT					L27	J24	F19													
			VCCA_PLL_1					HC5	C20	F17													
			VCCA_PLL_2					J10	HE	EE													
			VCCA_PLL_3					AF10	YE	VE													
			VCCA_PLL_4					AG20	HE20	W17													
			VCCA_PLL_5					T9	FB	LE													
			VCCA_PLL_6					HS9	RT	PE													
			VCCD_PLL_1					GE	H21	E18													
			VCCD_PLL_2					K9	GB	FS													
			VCCD_PLL_3					AE9	AA7	VE													
			VCCD_PLL_4					AK20	AA21	Y18													
			VCCD_PLL_5					LE	PT	ME													
			VCCD_PLL_6					V8	RE	NS													
			VCCIO3A					AM20	AG18	AC18													
			VCCIO3A					AK24	AD19	AA17													
			VCCIO3A					AJ20	AD16														
			VCCIO3A					AM20															
			VCCIO3C					AD25	AC20	V19													
			VCCIO4A					AM14	AG7	Y10													
			VCCIO4A					AM11	AG13	AC7													
			VCCIO4A					AL17	AG10	AC10													
			VCCIO4A					AL19	AG10														
			VCCIO4A					AL14	AD10														
			VCCIO4B					AM11															
			VCCIO4B					AG3	V2	V2													
			VCCIO4B					AD3	L2	R2													
			VCCIO4B					AE4	AE4	AA2													
			VCCIO4B					AA3	AE2														
			VCCIO4B					T6	K2	M2													
			VCCIO4B					T3	Q2	J2													
			VCCIO4B					P3	D2	F2													
			VCCIO4B					L3															
			VCCIO7A					F14	B7	C8													
			VCCIO7A					F13	B4	C5													
			VCCIO7A					C14	B13														
			VCCIO7A					G11	B10														
			VCCIO7B					GE															
			VCCIO8A					F22	F18	D16													
			VCCIO8A					F20	E16	C17													
			VCCIO8A					G23	C20	C14													
			VCCIO8A					C20	B18														
			VCCIO8A					H17															
			VCCIO8C					C26	G23	E19													
			VCCIO8A					AC20	AB18	U16													
			VCCIO8A					AC19	AA18														
			VCCP3B					AE24	V21	V17													
			VCCP4A					AE18	AA15	U10													
			VCCP4A					AE18	AA12														
			VCCP4B					AC13															
			VCCP5A					F12	JB	TR													
			VCCP5A					AA12	L7	T7													
			VCCP5A					F12	MB	K7													
			VCCP5A					R12	M7	K6													
			VCCP7A					MI5	J13	H10													
			VCCP7A					MI4	HI3														
			VCCP7B					L12															
			VCCP8A					MI9	HI8	HI3													
			VCCP8A					L19	GI6														
			VCCP8C					M24	IG1	H18													
3A		VREFBAND	VREFBAND	VREFBAND				AE20	Y17	T16													
4A		VREFBAND	VREFBAND	VREFBAND				AD16	AB12	V10													
4B		VREFBAND	VREFBAND	VREFBAND				AD15															
5A		VREFBAND	VREFBAND	VREFBAND				AB11	W7	U7													
6A		VREFBAND	VREFBAND	VREFBAND				N11	LB	J7													
7A		VREFBAND	VREFBAND	VREFBAND				L15	HI2	HI2													
7B		VREFBAND	VREFBAND	VREFBAND				K13															
8A		VREFBAND	VREFBAND	VREFBAND				F19	HI0	GI5													
			NC					AL30	AF21	AC22													
			NC					AM30	AF22	AC22													
			NC					AK20															
			NC					H22															
			NC					AK24															
			NC					J23															
			NC					E27															
			NC					AK20															
			NC					K28															
			NC					AK23															
			NC					F27															
			NC					AL26															
			NC					L28															
			NC					AL30															
			NC					AK21															
			NC					AK27															
			NC					G27															
			NC					AK20															
			NC					GB															
			NC					L25															
			NC					AK28															
			NC					G28															
			NC					HE23															
			NC					G26															
			NC					AL26															
			NC					GB															
			NC					AK26															
			NC					AK27															
			NC					AK27															
			NC					L27															
			NC					AK28			</												



Bank number (Note 1)	IO Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F1152	F780	F572	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note 3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780 (Note 3)	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)	DQS for X4 for F572 (Note 3)	DQS for X8/X9 for F572 (Note 3)	DQS for X16/X18 for F572 (Note 3)	
			NC				ANT															
			NC				A0															
			NC				A010															
			NC				A01															
			NC				A02															
			NC				A04															
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Bank number	IO Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F1152	F780	F572	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note 3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)	DQS for X4 for F572	DQS for X8/X9 for F572 (Note 3)	DQS for X16/X18 for F572 (Note 3)	
			NC				AL2															
			NC				AL3															
			NC				AL4															
			NC				AL7															
			NC				AG7															
			NC				AH6															
			NC				AG8															
			NC				AK5															
			NC				AK4															
			NC				AD10															
			NC				AK3															
			NC				AK9															
			NC				AK8															
			NC				AK7															
			NC				AK6															
			NC				AK11															
			NC				AK2															
			NC				AK1															
			NC				AK12															
			NC				AK21															
			NC				AK9															
			NC				AK0															
			NC				AK3															
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**Pin Information for the Arria® II GX EP2AGX95 Device**  
**Version 1.1**  
**Notes (1), (2), (3)**

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
<b>Clock and PLL Pins</b>		
CLK[4:15]	Clock, Input	Single ended clock input pin.
DIFFCLK[0:5]p	Clock, Input	Clock input pin for differential clock input. OCT Rd is not supported.
DIFFCLK[0:5]n	Clock, Input	Negative clock input for differential clock input. OCT Rd is not supported
PLL_[1:4]_CLKOUT1p	I/O, Clock	PLL[1:4]_CLKOUT1 (except PLL1 and PLL3 in EP2AGX125 and EP2AGX260) supports 2 clock I/O pins, configured either as one single ended I/O or one differential I/O pair. PLL1 and PLL3 in EP2AGX125 and EP2AGX260 support 6 clock I/O pins, configured either as 3 single ended I/Os or 3 differential I/O pairs.
PLL_[1:4]_CLKOUT1n	I/O, Clock	
PLL_[1,3]_CLKOUT[2:3]p (Note 4)	I/O, Clock	PLL1 and PLL3 in EP2AGX125 and EP2AGX260 support 6 clock I/O pins, configured either as 3 single ended I/Os or 3 differential I/O pairs.
PLL_[1,3]_CLKOUT[2:3]n (Note 4)	I/O, Clock	
<b>Dedicated Configuration/JTAG Pins</b>		
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (nCSO, ASDO, DATA[7:0], CLKUSR, INIT_DONE, DEV_OE, DEV_CLRn) are on or off before and during configuration. A logic high (1.5V, 1.8V, 2.5V, 3.0V or 3.3V) turns off the weak pull-up, while a logic low turns them on.
MSEL[0:3]	Input	Configuration input pins that set the FPGA device configuration scheme.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user-mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration done pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin.
nCEO	I/O, Output (open-drain)	Output that drives low when device configuration is complete. This pin can be used as a regular I/O if not used for device configuration.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as a user I/O pin.
TCK	Input	Dedicated JTAG test clock input pin.
TMS	Input	Dedicated JTAG test mode select input pin.
TDI	Input	Dedicated JTAG test data input pin.
TDO	Output	Dedicated JTAG test data output pin.
<b>Optional/Dual-Purpose Configuration Pins</b>		
nCSO	Output	Dedicated output control signal from the FPGA to the serial configuration device in AS mode that enables the configuration device.
ASDO	Output	Control signal from the FPGA to the serial configuration device in AS mode used to read out configuration data.
DCLK	I/O (PS, FPP) Output (AS)	Dedicated configuration clock pin. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into the FPGA. In AS mode, DCLK is an output from the FPGA that provides timing for the configuration interface.
CRC_ERROR	I/O, Output (open-drain)	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled. This pin can be used as regular I/O if not used for CRC error detection.
DEV_CLRn	I/O, Input	Optional pin that allows designers to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed.
DEV_OE	I/O, Input	Optional pin that allows designers to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
DATA0	Input	DATA[0] is a dedicated pin that is used for both the passive and active configuration modes
DATA[1:7]	I/O, Input	Dual-purpose configuration input data pins. The DATA[0:7] pins can be used for byte-wide configuration. DATA[1:7] pins can also be used as user I/O pins after configuration, but not DATA0.



**Pin Information for the Arria® II GX EP2AGX95 Device**  
**Version 1.1**  
**Notes (1), (2), (3)**

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin.
<b>Differential I/O Pins</b>		
DIFFIO_RX_[T,B,R][##]p, DIFFIO_RX_[T,B,R][##]n	I/O, RX channel	These are true LVDS receiver channels with OCT Rd support. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX_[T,B,R][##]p, DIFFIO_TX_[T,B,R][##]n	I/O, TX channel	These are true LVDS transmitter channels. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used as true LVDS transmitter channels, these pins can be configured as true LVDS receiver channels without OCT Rd support (DIFFIN_[T,B,R][##][p,n]). If not used for differential signaling, these pins are available as user I/O pins.
DIFFIN_[T,B,R][##]p, DIFFIN_[T,B,R][##]n	I/O, RX channel	These are true LVDS receiver channels without OCT Rd support. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used as true LVDS receiver channels without OCT Rd support, these pins can be configured as true LVDS transmitter channels (DIFFIO_TX_[T,B,R][##][p,n]). If not used for differential signaling, these pins are available as user I/O pins.
DIFFOUT_[##]p, DIFFOUT_[##]n	I/O, TX channel	These are emulated LVDS output channels. On I/O banks, there are true LVDS input buffers but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, (DIFFIO_RX_[T,B,R][##][p,n] , DIFFIN_[T,B,R][##][p,n]) can be configured as emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
<b>External Memory Interface Pins</b>		
DQS[##][T,B,R]	I/O, DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.
DQSn[##][T,B,R] (Note 5)	I/O, DQSn	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.
DQ[##][T,B,R]	I/O, DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
CQ[##][T,B,R]	DQS	Optional data strobe signal for use in QDR II SRAM. These are the pins for echo clocks.
CQn[##][T,B,R] (Note 5)	DQS	Optional complementary data strobe signal for use in QDR II SRAM. These are the pins for echo clocks.
<b>Reference Pins</b>		
RUP[0:2]	I/O, Input	Reference pins for I/O banks. The RUP pins share the same VCCIO with the I/O bank where they are located. The external precision resistor RUP must be connected to the designated RUP pin within the bank. If not required, this pin is a regular I/O pin.
RDN[0:2]	I/O, Input	Reference pins for I/O banks. The RDN pins share the same GND with the I/O bank where they are located. The external precision resistor RDN must be connected to the designated RDN pin within the bank. If not required, this pin is a regular I/O pin.
DNU	Do Not Use	Do Not Use (DNU).
NC	No Connect	Do not drive signals into these pins.
<b>Supply Pins</b>		
VCC	Power	VCC supplies power to the core and periphery.
VCCD_PLL_[1:6]	Power	Digital power for PLL [1:6]. All of these pins must be connected even if the PLL is not used
VCCCB	Power	Configuration RAM bits power supply.
VCCA_PLL_[1:6]	Power	Analog power for PLL [1:6]. All of these pins must be connected even if the PLL is not used
VCCIO[3:8][A,B]	Power	These are I/O supply voltage pins for banks 3 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all LVDS, LVCMOS(1.2V, 1.5V, 1.8V, 2.5V, 3.0V,3.3V), HSTL(12,15,18),SSTL(15,18,2),3.0V PCI/PCI-X I/O as well as LVTTTL (1.8V, 2.5V, 3.0V, 3.3V) I/O standards. VCCIO also supplies power to the input buffers used for LVCMOS(1.2V, 1.5V, 1.8V, 2.5V, 3.0V, 3.3V), 3.0V PCI/PCI-X and LVTTTL (1.8V, 2.5V, 3.0V, 3.3V) I/O standards.
VCCIO[3:8]C	Power	These are configuration and JTAG supply voltage pins for banks 3C and 8C. Each bank can support a different voltage level. For AS/PP/FPP configuration schemes, VCCIO8C supports 1.8V, 2.5V, 3.0V or 3.3V. JTAG can support 1.5V, 1.8V, 2.5V, 3.0V or 3.3V.



**Pin Information for the Arria® II GX EP2AGX95 Device**  
**Version 1.1**  
**Notes (1), (2), (3)**

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
VCCPD[3:8][A,B], VCCPD[3,8]C	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers and the input buffers for HSTL/SSTL input buffers. This can be connected to 3.3V, 3.0V or 2.5V. For 3.3V I/O standard connect VCCPD to 3.3V, for 3.0V I/O standard connect VCCPD to 3.0V and for 2.5V/1.8V/1.2V I/O standards connect VCCPD to 2.5V
VCCBAT	Power	Battery back-up power supply for design security volatile key register.
GND	Ground	Device ground pins.
VREF[3:8][A,B]N0	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. These pins cannot be used as regular I/Os.
<b>Transceiver Pins</b>		
VCCL_GXB	Power	Supplies power to the transceiver PMA TX, PMA RX and clocking.
VCCH_GXB	Power	Supplies power to the transceiver PMA output (TX) buffer.
VCCA	Power	Supplies power to the transceiver PMA regulator.
GXB_RX[0:15]p (Note 6)	Input	High speed positive differential receiver channels.
GXB_RX[0:15]n (Note 6)	Input	High speed negative differential receiver channels.
GXB_TX[0:15]p (Note 6)	Output	High speed positive differential transmitter channels.
GXB_TX[0:15]n (Note 6)	Output	High speed negative differential transmitter channels.
REFCLK[0:7]p	Input	High speed differential reference clock positive.
REFCLK[0:7]n	Input	High speed differential reference clock complement.
RREF[0:1]	Input	Reference resistor for transceiver.

**Notes:**

1. Refer to the Arria II GX Device Datasheet and Pin Connection Guidelines for the recommended operating conditions.
2. This pin definition is prepared based on the EP2AGX260.
3. Some of the pull-up /pull down resistors mentioned in the table above may not be required, depending on the exact device configuration scheme.  
 The ability to NC or short them may be valuable during the debug phase, should you be required to use a different configuration scheme.  
 Refer to the Configuring Arria II GX Devices chapter in the Arria II GX Device Handbook for more information.
4. PLL[1,3]\_CLKOUT[2..3][p,n] are only available in PLL1 and PLL3 in EP2AGX125 and EP2AGX260.
5. When not used as clocks, the CQn and DQS<sub>n</sub> pins can be used as DQ pin.
6. Transceiver signals GXB\_RX[15..0] and GXB\_TX[15..0] are device specific.

PLL_1	8C	8A	7A	7B	PLL_2	
		VREFB8AN0	VREFB7AN0	VREFB7BN0		
Transceiver Block (QL2)					6A	VREFB6AN0
Transceiver Block (QL1)					5A	VREFB5AN0
Transceiver Block (QL0)						
PLL_4	3C	3A	4A	4B	PLL_3	
		VREFB3AN0	VREFB4CN0	VREFB4BN0		

This is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only.



**Pin Information for the Arria<sup>®</sup> II GX EP2AGX95 Device**  
**Version 1.1**

<b>Version Number</b>	<b>Date</b>	<b>Changes Made</b>
1.0	2/27/2009	Initial release.
1.1	5/29/2009	Added DNU in Pin List and Pin Definitions.