

Features

- Provided with the Quartus™ II software
- Probes internal nodes while the design is running at system speeds
- Requires no design modification
- Optimized for APEX™ II and APEX 20K devices (including APEX 20K, APEX 20KE, and APEX 20KC devices)
- Provides non-intrusive probing of ball-grid array (BGA) pins
- Logic analyzer controls available within the Quartus II design software include:
 - Signal selection
 - Trigger setup
 - Memory configuration
 - Waveform display

General Description

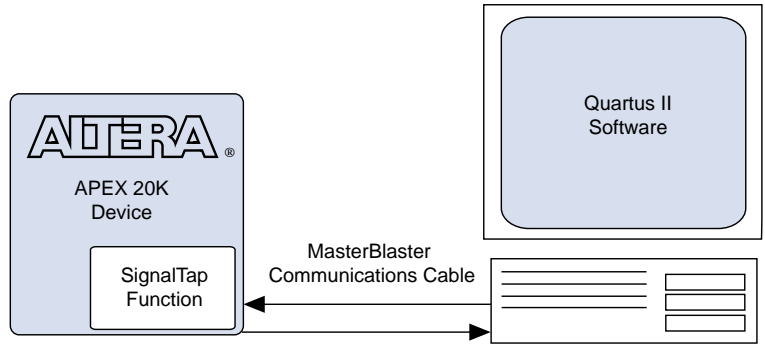
The SignalTap® logic analyzer megafunction captures signals from any internal node or I/O pin of an APEX II or APEX 20K device in real-time at system speed. SignalTap analysis also works with all existing EDA synthesis tool design flows. SignalTap analysis also eliminates the need for external probes and design file changes to capture signals from an internal node. The logic analyzer controls and signal capture display are all accessible from the Quartus II design software. The MasterBlaster™ or ByteBlasterMV™ communications cables support data transfer between the APEX II or APEX 20K device and the Quartus II software for waveform display of signals captured by SignalTap logic analysis.

Functional Description

The SignalTap megafunction is a parameterized embedded logic analyzer that provides access to signals inside an APEX II or APEX 20K device. The embedded logic analyzer function can be parameterized to capture from 1 to 128 signals from internal nodes or I/O pins. Signal capture occurs in-system and at system speed. From within the Quartus II software, the user selects which signals will be captured, when signal capture starts, and how many samples of data are captured. The user can also select if captured data will be stored in APEX II or APEX 20K embedded system block (ESB) RAM, or if data will be sent to I/O pins for capture by external analysis equipment. Data stored in ESB RAM is transferred to a host computer by using the MasterBlaster or ByteBlasterMV communication cable and is displayed in the SignalTap waveform viewer. See [Figure 1](#) for more information.

The Quartus II software can automatically instantiate the SignalTap logic analyzer without making changes to user design files.

Figure 1. SignalTap Logic Analyzer



Triggering Conditions

Trigger patterns can be defined to tell the SignalTap logic analyzer when to start capturing data. Any input signal channel can be set to a variety of trigger conditions. Data capture begins when all of the trigger conditions in the active trigger pattern are satisfied. Table 1 lists possible trigger conditions for each channel.

Trigger Condition	Description
Don't Care	Default trigger condition. The channel is not used to determine the trigger event.
Low	The analyzer triggers when the channel is low.
High	The analyzer triggers when the channel is high.
Falling	The analyzer triggers when the channel is falling.
Rising	The analyzer triggers when the channel is rising.
Rising or Falling Edge	The analyzer triggers when the channel is rising or falling.

A Trigger Position setting allows the user to specify the amount of data captured by the SignalTap logic analyzer that should be acquired before the trigger and the amount that should be acquired after the trigger. Acquired data is placed in a circular buffer, as shown in Figure 2, with the newest sample replacing the oldest. When triggered, the SignalTap logic analyzer continues sampling the input signals to capture post-trigger data. Set the ratio of pre-trigger to post-trigger data saved in the sample buffer using the settings shown in Table 2.

Figure 2. Circular Signal Capture Buffer

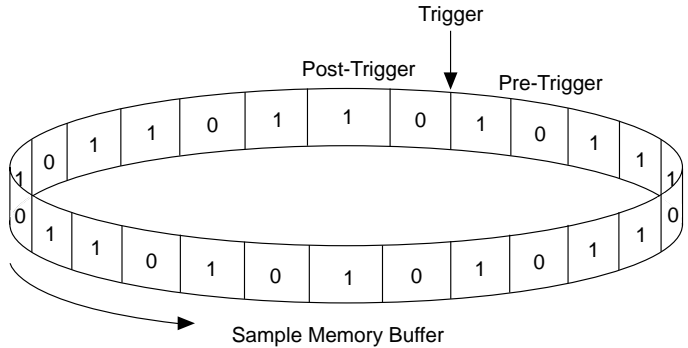


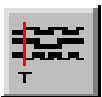



Table 2. Trigger Position Settings (Part 1 of 2)

Setting	Description
Pre 	Save signal activity that occurred before the trigger (88% pre-trigger, 12% post-trigger)
Center 	Save half pre-trigger and half post-trigger data
Post 	Save signal activity that occurred after the trigger (12% pre-trigger, 88% post-trigger)

Setting	Description
Continuous 	Save signal activity indefinitely (until stopped manually)

Trigger I/O

An unused I/O pin can be used as an external output to indicate that a trigger event has occurred. The polarity of the output pulse may be specified as high or low. An unused I/O pin can also be used to trigger the embedded logic analyzer by setting the trigger to recognize a high, low, rising edge, falling edge, either edge, or don't care condition.

Device Resource Usage

The number of logic elements (LEs) used by the logic analyzer is a function of the number of channels used. [Table 3](#) shows an estimate of the number of LEs consumed by the logic analyzer.

Channels Used	LEs
1	136
2	144
4	160
8	192
16	256
32	384
64	640
128	1,152

The embedded logic analyzer can use internal memory (i.e., ESBs) for acquisition data storage. The size and number of these blocks are device-dependent and must be considered when configuring the logic analyzer. The number of RAM bits consumed depends on the number of channels used and the number of samples taken. Table 4 shows the number of ESBs used to store the values for different configurations.

Channels	Buffer Samples				
	128	256	512	1,024	2,048
1	1	1	1	1	1
2	1	1	1	1	2
4	1	1	1	2	4
8	1	1	2	4	8
16	1	2	4	8	16
32	2	4	8	16	32
64	4	8	16	32	64
128	8	16	32	64	128

Logic Analyzer Configurations

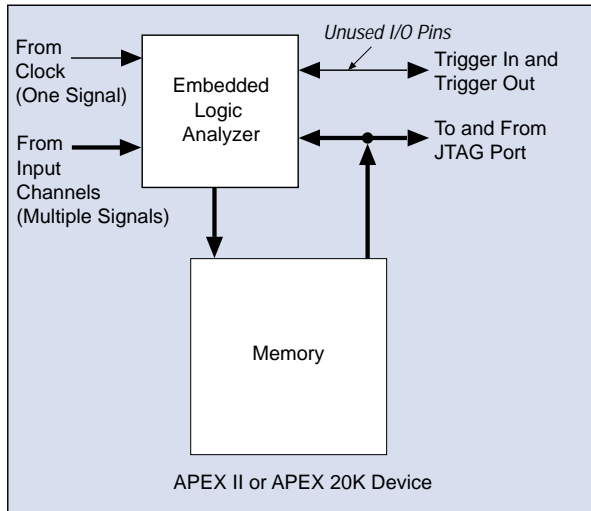
The SignalTap embedded logic analyzer provides several data configurations that can be used in any combination. The configurations are:

- Embedded logic analyzer
- Debugging port
- Trigger output

Embedded Logic Analyzer

In the embedded logic analyzer configuration, I/O pins and internal nodes can be connected to input channels for data capture. The analyzer clock signal comes from an internal global clock. The acquisition data is placed in RAM and then streamed off-chip via the IEEE Std. 1149.1 Joint Test Action Group (JTAG) interface. See Figure 3 for more information. The optional trigger-in and trigger-out signals can be routed to spare I/O pins to synchronize the embedded logic analyzer to external test equipment or to circuitry and vice-versa.

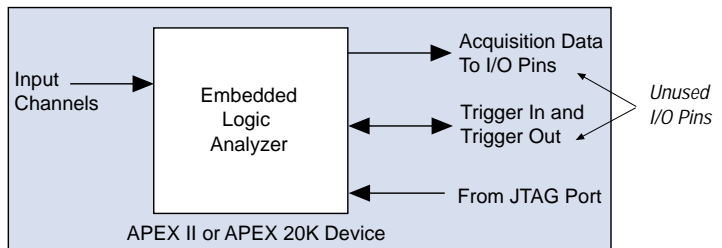
Figure 3. Embedded Logic Analyzer Architecture



Debugging Port

When device RAM is limited, you can route internal signals to unused I/O pins for capture by an external analyzer or oscilloscope. The debugging port conserves ESBs at the expense of I/O pins and is useful for data-intensive applications in which the amount of saved data exceeds the available sample buffer. See [Figure 4](#).

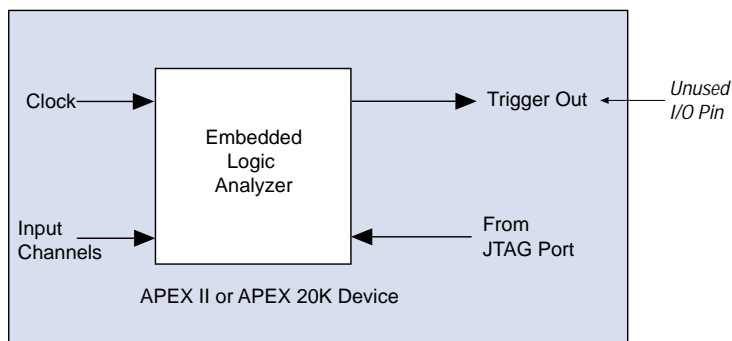
Figure 4. Device Debugging Port



Trigger Output

The trigger-out signal can be used to generate a pulse on a spare I/O pin when the embedded logic analyzer trigger pattern is recognized. The trigger-out pulse can be set to active high or active low, and remains active until the input signals no longer match the trigger pattern. Trigger out requires no ESBs and only one I/O pin. See [Figure 5](#).

Figure 5. Using the Logic Analyzer as an Event Analyzer



Download Cable Support

All setup, control, and display functions for the SignalTap analyzer are integrated into the Quartus II development software. The MasterBlaster or ByteBlasterMV communications cable uploads required data from internal nodes to the Quartus II software, where they are displayed in the Waveform Editor window.

The MasterBlaster communications cable downloads information at high speeds to APEX II or APEX 20K devices. The USB host interface supports download bitstream rates up to 12 megabits per second (Mbps) to the target device. An RS-232 port is also provided and runs at speeds up to 115k baud. A JTAG interface connects to the target device for design download and acquisition buffer retrieval. The MasterBlaster cable supports I/O voltages for the entire range of Altera® devices. The ByteBlasterMV cable only supports 3.3-V and 5.0-V voltages.



See the [MasterBlaster Serial/USB Communications Cable Data Sheet](#) for more information.

Conclusion

With the SignalTap embedded analyzer megafunction, internal device signals can be monitored in a variety of ways without affecting device performance. Triggering, system resource management, and configuration can be controlled using the Quartus II software in conjunction with the MasterBlaster or ByteBlasterMV communications cable. Data may be routed externally to unused I/O pins or to a JTAG port. Analyzed data is useful for debugging designs and optimizing system performance.



101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
<http://www.altera.com>
Applications Hotline:
(800) 800-EPLD
Customer Marketing:
(408) 544-7104
Literature Services:
lit_req@altera.com

Altera, APEX, APEX II, APEX 20K, APEX 20KE, APEX 20KC, ByteBlasterMV, MasterBlaster, Quartus, Quartus II, and SignalTap, and are trademarks and/or service marks of Altera Corporation in the United States and other countries. Altera acknowledges the trademarks of other organizations for their respective products or services mentioned in this document. Altera products are protected under numerous U.S. and foreign patents and pending applications, maskwork rights, and copyrights. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera Corporation. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.



I.S. EN ISO 9001

Copyright © 2001 Altera Corporation. All rights reserved.

