



## Introduction

This document addresses known errata and documentation changes for the DSP Development Kit, Stratix® II Edition version 1.0.0.

Errata are design functional defects or errors. Errata may cause the board or the designs included with the kit to deviate from published specifications.

Documentation changes include typos, errors, unclear descriptions, or omissions from current published specifications or product documents. These documentation changes or clarifications will be incorporated in upcoming releases of the kit.

## DSP Development Kit, Stratix II Edition Issues

Altera has identified the following issues that affect the DSP Development Kit, Stratix II Edition:

1. [“JTAG Programming Fails When Using the Quartus II Software Version 4.2 to Program the 2S60 DSP Development Board” on page 1.](#)
2. [“The FFT Co-Processor Reference Design Reports an Error When Compiling With the Quartus II Software Version 4.2 or Later” on page 2.](#)
3. [“The DACs Are AC Coupled, Not DC Coupled as the Board Data Sheet Indicates” on page 3.](#)
4. [“The Stratix II ES Devices Have an M-RAM Problem When Using Byte Enables” on page 4.](#)
5. [“J23 Pin 5 is Connected to P32, Not R32” on page 4.](#)

### **JTAG Programming Fails When Using the Quartus II Software Version 4.2 to Program the 2S60 DSP Development Board**

On the Stratix II DSP board, configuration of the FPGA via JTAG fails when using the Quartus® II software version 4.2 or version 4.2 SP1 if `switch4` is set to the OPEN position on DIP switch SW2.

The Quartus II software version 4.2 (with or without SP1) loads the user design and reports that the device programming was successful. However, the configuration controller in the MAX II device does not recognize that the device programming was successful and reloads the factory design immediately after the user design has been loaded. The result is that programming appears to have failed.

The Quartus II software version 4.1 SP2, which is the version that ships with the kit, programs the FPGA appropriately.

### *Affected Configurations*

This failure is observed on all Stratix II DSP boards when configuring the FPGA via JTAG in the Quartus II software version 4.2 with `switch4` on DIP switch SW2 set to the OPEN position.

### *Design Impact*

The user programming file loads, but it is immediately overwritten by the factory configuration.

### *Workaround*

Set `switch4` to the CLOSED position on DIP switch SW2 before programming the FPGA. This action disables the configuration controller and allows the FPGA to be successfully configured via JTAG using the Quartus II software version 4.2.

Alternatively, you can use the Quartus II software version 4.1 SP2 to program the board via JTAG.

### *Solution Status*

The Quartus II software version 5.0 fixes this problem. Also, the problem is not observed when using the Quartus II software version 4.1 SP2.

## **The FFT Co-Processor Reference Design Reports an Error When Compiling With the Quartus II Software Version 4.2 or Later**

When compiling the FFT co-processor in the Quartus II software version 4.2 (with or without SP1), the compiler reports the following error:

```
Error: Verilog HDL error at atlantic_fifo.v(372):  
variable "fifo_wr_mty" has mixed blocking and  
nonblocking Procedural Assignments -- must be all  
blocking or all nonblocking assignments
```

### *Affected Configurations*

This failure is observed with the Quartus II software version 4.2 or later. The Quartus II software version 4.1 SP2 does not report this error.

### *Design Impact*

The FFT co-processor demonstration cannot be compiled with versions of the Quartus II software after version 4.1 SP2.

### *Workaround*

Replace the **atlantic\_fifo.v** file that is found in the `<install_path>\Examples\HW\ReferenceDesigns\emif_ref_design_FFT\example\source` directory after installation of the kit CD. A replacement file can be downloaded from the following location:

[ftp://ftp.altera.com/outgoing/devkit/DSP\\_DK\\_2S60/DSP-2S60\\_FFT\\_fix\\_Q4p2.zip](ftp://ftp.altera.com/outgoing/devkit/DSP_DK_2S60/DSP-2S60_FFT_fix_Q4p2.zip)

### *Solution Status*

Users must download the replacement **atlantic\_fifo.v** file to use this design in versions of the Quartus II software after version 4.1 SP2.

## **The DACs Are AC Coupled, Not DC Coupled as the Board Data Sheet Indicates**

Figure 5 (page 23) in the *Stratix II DSP Board Data Sheet* shows the on-board circuitry after a D/A converter. The output of a D/A converter chip, DAC904, consists of a current source whose maximum value is 20 mA. This differential output is converted to a single-ended output using an RF transformer. The DSP board uses a 1:1 ratio transformer to interface to a 50 ohm impedance load. Each of the outputs is terminated with a 49.9 ohm resistor to ground. This circuit results in the outputs being AC coupled and inherently isolated due to the transformers magnetic coupling. The output of the transformer is then brought to an SMA connector.

### *Affected Configurations*

Applies to all Stratix II DSP boards.

### *Design Impact*

None. This problem is a documentation error.

### *Workaround*

None.

### *Solution Status*

The next version of the data sheet will correctly document the DAC circuitry.

## **The Stratix II ES Devices Have an M-RAM Problem When Using Byte Enables**

Stratix II EP2S60 ES devices have a silicon problem that prevents the use of byte enables on M-RAM blocks. Refer to the *Stratix II FPGA Family Errata Sheet* for details. Because of this issue, the Quartus II software does not allow you to directly instantiate an M-RAM block with byte enables in designs targeting EP2S60 ES devices.

### *Affected Configurations*

Applies to all Stratix II ES devices.

### *Design Impact*

Byte enables cannot be used on M-RAM blocks in Stratix II EP2S60 ES devices.

### *Workaround*

Stratix II production devices (non-ES) support M-RAM byte enables.

### *Solution Status*

The problem is fixed in Stratix II production devices (non-ES).

## **J23 Pin 5 is Connected to P32, Not R32**

Figure 11 (page 46) in the *Stratix II DSP Board Data Sheet* shows that J23 pin 5 is connected to pin R32 on the Stratix II device. This is incorrect. J23 pin 5 is actually connected to pin P32 on the Stratix II device.

### *Affected Configurations*

Applies to all Stratix II DSP boards.

*Design Impact*

None. This problem is a documentation error.

*Workaround*

Ensure that you assign the pin in your project to P32, not R32.

*Solution Status*

This will be fixed in the next revision of the Board data sheet.

**Contact Information**

For more information, contact Altera’s mySupport website at [www.altera.com/mysupport](http://www.altera.com/mysupport) and click **Create New Service Request**. Choose the **Product Related Request** form.

**Revision History**

Table 1 shows the revision history.

<i>Table 1. Revision History</i>		
Version	Date	Details of Change
1.0	April 2005	First release of the DSP Development Kit, Stratix II Edition errata sheet.



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