



## Introduction

This document addresses known errata and documentation changes for the High Speed Development Kit, Stratix® II Edition version 1.0.0.

Errata are design functional defects or errors. Errata may cause the board or the designs included with the kit to deviate from published specifications.

Documentation changes include typos, errors, unclear descriptions, or omissions from current published specifications or product documents. These documentation changes or clarifications will be incorporated in upcoming releases of the kit.

## High Speed Development Kit, Stratix II Edition Issues

Altera has identified the following issues that affect the High Speed Development Kit, Stratix II Edition:

1. [“JTAG Programming Fails When Using the Quartus II Software Version 4.2 to Program the 2S60 High Speed Development Board” on page 1.](#)
2. [“The Stratix II ES Devices Have an M-RAM Problem When Using Byte Enables” on page 2.](#)

### JTAG Programming Fails When Using the Quartus II Software Version 4.2 to Program the 2S60 High Speed Development Board

On the Stratix II High Speed board, configuration of the FPGA via JTAG fails when using the Quartus® II software version 4.2 or version 4.2 SP1 if switch3 (MSEL1) is set to the OPEN position on DIP switch S2.

The Quartus II software version 4.2 (with or without SP1) loads the user design and reports that the device programming was successful. However, the configuration controller in the MAX II device does not recognize that the device programming was successful and reloads the factory design immediately after the user design has been loaded. The result is that programming appears to have failed.

The Quartus II software version 4.1 SP2, which is the version that ships with the kit, programs the FPGA appropriately.

### *Affected Configurations*

This failure is observed on all Stratix II High Speed boards when configuring the FPGA via JTAG in the Quartus II software version 4.2 with `switch3` on DIP switch S2 set to the OPEN position.

### *Design Impact*

The user programming file loads, but it is immediately overwritten by the factory configuration.

### *Workaround*

Set `switch3` to the CLOSED position on DIP switch S2 before programming the FPGA. This action disables the configuration controller and allows the FPGA to be successfully configured via JTAG using the Quartus II software version 4.2.

Alternatively, you can use the Quartus II software version 4.1 SP2 to program the board via JTAG.

### *Solution Status*

The Quartus II software version 5.0 fixes this problem. Also, the problem is not observed when using the Quartus II software version 4.1 SP2.

## **The Stratix II ES Devices Have an M-RAM Problem When Using Byte Enables**

Stratix II EP2S60 ES devices have a silicon problem that prevents the use of byte enables on M-RAM blocks. Refer to the *Stratix II FPGA Family Errata Sheet* for details. Because of this issue, the Quartus II software does not allow you to directly instantiate an M-RAM block with byte enables in designs targeting EP2S60 ES devices.

### *Affected Configurations*

Applies to all Stratix II ES devices.

### *Design Impact*

Byte enables cannot be used on M-RAM blocks in Stratix II EP2S60 ES devices.

### *Workaround*

Stratix II production devices (non-ES) support M-RAM byte enables.

### Solution Status

The problem is fixed in Stratix II production devices (non-ES).

## Contact Information

For more information, contact Altera's mySupport website at [www.altera.com/mysupport](http://www.altera.com/mysupport) and click **Create New Service Request**. Choose the **Product Related Request** form.

## Revision History

Table 1 shows the revision history.

Version	Date	Details of Change
1.0	April 2005	First release of the High Speed Development Kit, Stratix II Edition errata sheet.



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