

Introduction

This document addresses known errata and documentation changes for version 1.3.0 of the POS-PHY Level 2 and 3 Compiler.

Errata are design functional defects or errors. Errata may cause the POS-PHY Level 2 and 3 Compiler to deviate from published specifications.

Documentation changes include typos, errors, unclear descriptions or omissions from current published specifications or product documents. These documentation changes or clarifications will be incorporated into an upcoming release of the POS-PHY Level 2 and 3 Compiler.

POS-PHY Level 2 & 3 Compiler v1.3.0 Issues

Altera has identified the following issue that affects the POS-PHY Level 2 and 3 Compiler v1.3.0:

1. “SX Signal May Not Be Asserted in SX Always Mode”.

SX Signal May Not Be Asserted in SX Always Mode

A POS-PHY MegaCore® function may not assert the SX signal with the address of the packet. This issue only happens if the transfer pauses two cycles before the end of a burst sequence in SX Always mode.

The SX signal occurs correctly when the address changes.

Affected Configurations

This problem only affects ports of the MegaCore function that are configured as POS-PHY Level 3 PHY sources in SX Always mode and that use a custom setting to resend the address after a fixed burst length.

Design Impact

Data may be lost when interfacing to external devices that are not fully POS-PHY Level 3 compliant. The POS-PHY protocol is never violated.

Workaround

No workaround is available.

Solution Status

This issue will be fixed in the next release of the POS-PHY Level 2 and 3 Compiler.

Contact Information

For more information, contact Altera's mySupport website at www.altera.com/mysupport and click **Create New Service Request**. Choose the **Product Related Request** form.

Revision History

Table 1 shows the revision history.

Version	Date	Details of Change
1.0	November 2004	First release of the POS-PHY Level 2 and 3 Compiler errata sheet for version 1.3.0.



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