

Introduction


This errata sheet provides updated information about the development kit for the ARM®-based family of embedded processor programmable logic devices (PLDs).

The development kit contains the EPXA10 development board. Most of the errata are related to the development board.



EXCALIBUR™



 Identify the revision number of your Excalibur™ development kit before using this errata information, because the kit has been revised. Revised information given in this document affects only revision 2.1 of the Excalibur development kit.

To identify the revision number of the development kit, the revision number of the development board contained in the kit must be identified. Examine the Altera® logo, which is located in the lower-right corner of the board. The revision number of revision 2.1 boards is printed in dark green to the left of the logo below the PCI connector. For this errata sheet, the revision information must be *XA10 Development Board Revision 2.1*. Revision 2.1 boards are populated with an EPXA10F1020C1 device.

The revised information given in this document updates information on the following board features:

- CONF_DONE LED
- U125 and U126 daughter card connectors
- Connected nets
- PCI functionality
- PCI connectors
- Errata of the Excalibur ARM-based embedded processor PLD device
- New versions of Excalibur IP cores

Information for each errata includes an assessment of the severity of the problem, which is indicated by a grade from 'a' to 'e' next to the problem description. A grade 'a' anomaly is likely to affect only a small proportion of customer applications, and then only under specific operational situations. Grade 'a' anomalies generally have a work around with minimal impact on the customer application. A grade 'e' anomaly could present a challenge to most applications.

You are recommended to contact Altera for latest information.

CONF_DONE LED (a)

Observation

The CONF_DONE LED on the development board does not reflect the status of the EPXA10 CONF_DONE signal.

Cause

The CONF_DONE LED is connected to the INIT_DONE pin of the EPXA10 device.

Work Around

To avoid confusion, relabel the LED on the development board manually.

U125 and U126 Daughter Card Connector (a)

Observation

The U125 and U126 daughter card connector pin-out table in earlier versions of the *Excalibur EPXA10 Development Board User Guide* is incorrect.

Cause

The following pin connections are not stated correctly in versions 1.1 and earlier of the *Excalibur EPXA10 Development Board User Guide*. [Table 1](#) lists the correct physical connection between connector U125 on the development board and the EPXA10.

| Table 1. Connections Between the EPXA10 Device and U125 | |
|--|-------------------------------|
| EPXA10 Device Pin | U125 Daughter Card Pin |
| N26 | 69 |
| M26 | 80 |
| P27 | 81 |
| M28 | 83 |

[Table 2](#) lists the correct physical connection between connector U126 on the development board and the EPXA10.

| Table 2. Connections Between the EPXA10 Device and U126 | |
|--|-------------------------------|
| EPXA10 Device Pin | U126 Daughter Card Pin |
| J26 | 170 |

Work Around

Use [Tables 1 and 2](#) for the five development board connections listed, instead of using versions 1.1 and earlier of the *Excalibur EPXA10 Development Board User Guide*. Alternatively, download a new version from <http://www.altera.com/literature/lit-exc.html>.

Connected Nets (e)

Observation

Some pins on the U125 daughter card header do not change their signal level independently.

Cause

[Table 3](#) shows the signal nets which are connected on the development board. The connections between the daughter card header, U125, and the EPXA10 device on the right and on the left are correct. The connections in between the two nets on the right and left are false connections.

| Table 3. Connected Signal Nets | | | | |
|---------------------------------------|----------------------|-------------------------|--------------|----------------------|
| Net A | | False Connection | Net B | |
| U125 | EPXA10 device | | U125 | EPXA10 device |
| 19 | AM25 | ↔ | 23 | AJ25 |
| 21 | AK25 | ↔ | 25 | AG25 |

Work Around

It is not possible to separate the falsely connected nets (A and B) by cutting the appropriate board wires. This is why only one driving signal can be applied to both nets.

Valid net configurations are shown in [Table 4 on page 4](#).

Table 4. Valid Net Configurations

| Net A | | False Connection | Net B | |
|---------------------|-----------------------------|------------------|---------------------|-----------------------------|
| Ext. signal at U125 | Configuration of EPXA10 pin | | Ext. signal at U125 | Configuration of EPXA10 pin |
| input | input | ↔ | input | input |
| <i>output</i> | input | ↔ | input | input |
| input | <i>output</i> | ↔ | input | input |
| input | input | ↔ | <i>output</i> | input |
| input | input | ↔ | input | <i>output</i> |
| input | input | ↔ | NC | input |
| <i>output</i> | input | ↔ | NC | input |
| input | <i>output</i> | ↔ | NC | input |
| input | input | ↔ | NC | <i>output</i> |
| NC | input | ↔ | input | input |
| NC | <i>output</i> | ↔ | input | input |
| NC | input | ↔ | <i>output</i> | input |
| NC | input | ↔ | input | <i>output</i> |
| NC | input | ↔ | NC | input |
| NC | <i>output</i> | ↔ | NC | input |
| NC | input | ↔ | NC | <i>output</i> |

PCI Functionality (c)

Observation

Communication on the PCI ports is corrupted or does not work when only PCI slaves are present.

Cause

PCI pins Req1 and Req2 have no pull-up resistors.

Work Around

To recover PCI communication, do one of the following:

- Use at least one PCI master
- Solder two 10-kΩ resistors between pins 18 and 19 of U23 and U24 (the PCI slots)

PCI Connectors

Observation

The pin labeling of the PCI connectors on the development board is incorrect.

Cause

The A and B row labels are reversed on the development board silkscreen, causing the labels to be incorrect. The actual connection of the PCI connectors is correct for 3.3-V 32-bit or universal PCI cards.

Work Around:

Relabel the PCI connection if necessary; refer to the *EPXA10 Development Board Hardware Reference Manual* for the correct usage of the PCI connectors.

Errata of the Excalibur ARM-Based Device

The Excalibur EPXA10 Development Board contains an Excalibur ARM-based embedded processor PLD device, EPXA10F1020C1. All errata applicable to this device should be taken into account.

New Versions of Excalibur IP Cores

The evaluation versions of the Excalibur IP cores shipped with the development kit are constantly subject to improvement. Please download the latest versions of the documents from the Altera website:

http://www.altera.com/products/ip/altera/m-alt-10_100_ethernet.html

<http://www.altera.com/products/ip/altera/m-alt-a16450.html>



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