



EPF10K100E

Embedded Programmable Logic Device

June 1999, ver. 1.0

Errata Sheet

Preliminary Information

This errata sheet provides updated information for engineering sample (ES) EPF10K100EQC240-2XES and EPF10K100EBC356-2XES devices with the ClockLock™ and ClockBoost™ circuitry, which is indicated by an “X” in the ordering code. These engineering samples are intended for prototyping only.

The programming files generated for ES devices are not compatible with production devices. Designers must recompile EPF10K100EQC240-2XES and EPF10K100EBC356-2XES designs to generate programming files for production devices.

Full compilation and programming support for EPF10K100EQC240-2XES devices will be available in the MAX+PLUS® II version 9.25 update, which can be requested from the Altera® web site (<http://www.altera.com>). The update also supports pin-out generation and simulation using the ClockLock and ClockBoost features for -1 and -2 speed grade EPF10K100E devices in all packages. Full compilation and programming support for EPF10K100EBC356-2XES devices will be available in the MAX+PLUS II software version 9.3.

EPF10K100EQC240-2XES and EPF10K100EBC356-2XES devices can be configured via the configuration device, passive serial, passive parallel synchronous, passive parallel asynchronous, JTAG, and Jam™ modes.



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