

This document addresses known errata and documentation issues for the Altera® CIC MegaCore® function, v7.1. Errata are functional defects or errors, which may cause an CIC MegaCore function to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

CIC MegaCore function, v7.1 Issues

Altera has identified the following issue that affects the CIC MegaCore function, v7.1.

Synthesis Error When Number of Stages is Greater than 10

If the number of stages is more than 10, a signal name used in the MISO architecture can conflict.

Affected Configurations

MISO architectures with 10 stages or more.

Design Impact

An incorrect variation file is generated which cannot be synthesized. The following error message is issued:

```
VHDL error at xxx_cic.vhd(115): name "D_fsR10" cannot be used because it is already used for a previously declared item
```

Workaround

A patch is available from Altera customer support.

Solution Status

This issue will be fixed in v7.2 of the CIC MegaCore function.



For existing up-to-date errata, refer to the [CIC, v7.1 Errata Sheet](#) on the [Errata Sheets](#) page of the Altera literature website.

Contact Information

For more information, contact Altera's mySupport website at www.altera.com/mysupport and click **Create New Service Request**. Choose the **Product Related Request** form.

Revision History

Table 1 shows the revision history for the *CIC MegaCore function, v7.1 Errata Sheet*.

Table 1. CIC MegaCore Function v7.1 Errata Sheet Revision History		
Version	Date	Errata Summary
1.1	July 2007	Added synthesis error errata.
1.0	May 2007	First release of this errata sheet.



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