

This document addresses known errata and documentation issues for the CRC Compiler version 6.1. Errata are functional defects or errors, which may cause the CRC Compiler to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.



For the most up-to-date errata for this release, continue to refer to the errata page on the Altera® website:

[www.altera.com/literature/es/es\\_crc\\_61.pdf](http://www.altera.com/literature/es/es_crc_61.pdf)

## CRC Compiler v6.1 Issues

Table 1 shows the issues that affect the CRC Compiler v6.1.

<i>Table 1. CRC Compiler v6.1 Issues</i>	
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### Counters in Verilog HDL Testbench Not Properly Reset

The Verilog HDL demonstration testbench contains the counters, `errI` and `errC`, which count inserted and detected errors respectively. These counters are not properly initialized when `reset_n` is asserted resulting in incorrect initial counter values. After `reset_n` is deasserted, the absolute counter values remain incorrect but the counters are properly incremented. To determine the correct values during simulation, subtract the initial values of these counters from the current value of the counters.

#### *Affected Configurations*

This issue affects only the Verilog HDL demonstration testbench.

#### *Design Impact*

This issue has no adverse effects on the generated MegaCore function or simulation model.

### *Workaround*

This issue does not require a workaround.

### *Solution Status*

This issue will be fixed in the 7.1 release.

## **Setting the Process low-numbered bit first Control Has No Effect**

The generated CRC MegaCore processes the high numbered input bits first regardless of whether or not you turn on the **Process low-numbered bit first** setting in the **Input Options** on the **Parameter Settings** page in the Quartus® II MegaWizard® interface.

### *Affected Configuration*

This issue affects all CRC generator and CRC checker variations.

### *Design Impact*

The impact of this issue is that the value of the CRC generator `checksum` output or the CRC checker `crcbad` output will be incorrect.

### *Workaround*

To workaround this issue, manually reverse the bit order of the connections to the `data` input of the CRC MegaCore function.

### *Solution Status*

This issue will be corrected in the 7.0 release.

## **Contact Information**

For more information, contact Altera's mySupport website at [www.altera.com/mysupport](http://www.altera.com/mysupport) and click **Create New Service Request**. Choose the **Product Related Request** form.

## Revision History

Table 2 shows the revision history for the *CRC Compiler v6.1 Errata Sheet*.

Version	Date	Errata Summary
1.1	July 2007	Added the erratum, Setting the Process low-numbered bit first Control Has No Effect.
1.0	December 2006	<ul style="list-style-type: none"> <li>Counters in Verilog HDL Testbench Not Properly Reset</li> </ul>



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