

This document addresses known errata and documentation issues for the CRC Compiler version 7.0. Errata are functional defects or errors, which may cause the CRC Compiler to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.



For the most up-to-date errata for this release, continue to refer to the errata page on the Altera® website:

[www.altera.com/literature/es/es\\_crc\\_70.pdf](http://www.altera.com/literature/es/es_crc_70.pdf)

## CRC Compiler v7.0 Issues

Table 1 shows the issues that affect the CRC Compiler v7.0.

<i>Table 1. CRC Compiler v7.0 Issues</i>	
Issue	Page
Counters in the Verilog HDL Testbench Not Properly Reset	1
Testbench Directory Generated When You Create a Simulation Model	2

### Counters in Verilog HDL Testbench Not Properly Reset

The Verilog HDL demonstration testbench contains the counters, `errI` and `errC`, which count inserted and detected errors respectively. These counters are not properly initialized when `reset_n` is asserted resulting in incorrect initial counter values. After `reset_n` is deasserted, the absolute counter values remain incorrect but the counters are properly incremented. To determine the correct values during simulation, subtract the initial values of these counters from the current value of the counters.

#### *Affected Configurations*

This issue affects only the Verilog HDL demonstration testbench.

#### *Design Impact*

This issue has no adverse effects on the generated MegaCore function or simulation model.

### *Workaround*

This issue does not require a workaround.

### *Solution Status*

This issue will be fixed in the 7.1 release.

## **Testbench Directory Generated When You Create a Simulation Model**

When you create a simulation model, the CRC compiler automatically creates a **testbench** directory in the project directory for you. If you follow the **Running the Testbench Example** steps in the *CRC Compiler User Guide* to create the generator and checker files, another **testbench** directory is created as a subdirectory of the initial **testbench** directory resulting in the following directory structure:

```
c:\altera\projects\crc_project\testbench\testbench
```

when the initial directory is

```
c:\altera\projects\crc_project\testbench
```

### *Affected Configuration*

All CRC MegaCore function variations are affected.

### *Design Impact*

There is no design impact for this issue.

### *Workaround*

The **testbench** subdirectory (**testbench\testbench**) of the initial **c:\altera\projects\crc\_project\testbench** directory may be deleted.

### *Solution Status*

Currently, there are no plans to change this behavior.

## **Contact Information**

For more information, contact Altera's mySupport website at [www.altera.com/mysupport](http://www.altera.com/mysupport) and click **Create New Service Request**. Choose the **Product Related Request** form.

## Revision History

Table 2 shows the revision history for the *CRC Compiler v7.0 Errata Sheet*.

Version	Date	Errata Summary
1.1	December	<ul style="list-style-type: none"> <li>Revised description for erratum, <b>Counters in Verilog HDL Testbench Not Properly Reset</b></li> <li><b>Testbench Directory Generated When You Create a Simulation Model</b></li> </ul>
1.0	December 2006	<ul style="list-style-type: none"> <li><b>Counters in Verilog HDL Testbench Not Properly Reset</b></li> </ul>



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