



# DDR & DDR2 SDRAM Controller Compiler

August 2007, Compiler Version 7.1

Errata Sheet

This document addresses known errata and documentation issues for the DDR and DDR2 SDRAM Controller Compiler version 7.1. Errata are functional defects or errors, which may cause the DDR and DDR2 SDRAM Controller Compiler to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

Table 1 shows the issues that affect the DDR and DDR2 SDRAM Controller Compiler v7.1.

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**Table 1. DDR and DDR2 SDRAM Controller Compiler v7.1 Issues**

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For the most up-to-date errata for this release, refer to the errata sheet on the Altera® website:

[www.altera.com/literature/es/es\\_ddr\\_ddr2\\_sdram\\_71.pdf](http://www.altera.com/literature/es/es_ddr_ddr2_sdram_71.pdf)

## DDR & DDR2 SDRAM Controller Compiler v7.1 Issues

This section describes the DDR and DDR2 SDRAM Controller Compiler v7.1 issues.

### SOPC Builder Data and Address Width Errors

The DDR or DDR2 SDRAM slave address space in SOPC Builder does not update when you change the controller data width.

#### *Affected Configurations*

This issue affects DDR and DDR2 SDRAM Controller designs in SOPC Builder.

#### *Design Impact:*

Your design may fail to operate correctly if the address space is incorrect.

#### *Workaround*

Add a new instance of the controller to SOPC Builder when you want to change the data width. The address space is correctly calculated when adding a new instance.

#### *Solution Status*

This issue will be fixed in the next version of the DDR and DDR2 SDRAM Controller Compiler.

## ODT Launches Off System Clock

In designs with a separate address and command clock, the ODT output launches from the system clock not from this address and command clock.

### *Affected Configurations*

This issue affects the following configurations:

- DDR2 SDRAM controller (not DDR SDRAM)
- ODT is turned on
- CAS latency is set to three
- The design uses a separate address and command clock and not the default system clock

### *Design Impact*

It may not be possible to close timing on the address and command outputs, because the ODT pin is launched on a different clock to the rest of the address and command outputs.

### *Workaround*

Use a CAS latency of four, which means one extra cycle of read latency, or use the DDR SDRAM High-Performance controller, which uses the ALTMEMPHY megafunction to transfer all the address and command outputs to the correct clock.

### *Solution Status*

This issue will never be fixed.

## Simulating with the NCSim Software

The DDR or DDR2 SDRAM Controller MegaCore® functions do not fully support the NCSim software.

### *Affected Configurations*

This issue affects all configurations.

### *Design Impact*

The design does not simulate.

### *Workaround*

Set the `-relax` switch for all calls to the VHDL analyzer.

### *Solution Status*

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controller Compiler.

## **Simulating with the VCS Simulator**

The DDR or DDR2 SDRAM Controller MegaCore functions do not fully support the VCS simulator.

### *Affected Configurations*

This issue affects all configurations.

### *Design Impact*

The design does not simulate.

### *Workaround*

The following workarounds exist.

### **VHDL**

Change the following code.

- In file `<variation name>_example_driver.vhd`, change all when statements between lines 333 and 503 from when `std_logic_vector'("<bit_pattern>")` to when `"<bit_pattern>"`.
- In file `testbench\<example name>_tb`, change line 191 from `signal zero_one(gMEM_BANK_BITS -1 downto 0) := (0 => '1', others => '0')` to `signal zero_one(gMEM_BANK_BITS -1 downto 0) := ('1', others=> '0')`.

### **Verilog HDL**

No changes are necessary. Calls to the Verilog analyzer sets the `+v2k` switch to enable Verilog 2000 constructs.

### *Solution Status*

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controller Compiler.

## VHDL Package Declaration Error When Upgrading the MegaCore Function

If you upgrade an existing custom variation of the MegaCore function, the following error may occur:

```
Error (10624): VHDL Package Declaration error at
auk_ddr_tb_functions.vhd(23): package "auk_ddr_tb_functions" already
exists in the work library
```

IP Toolbench adds files to your Quartus® II project when you generate your custom variation. When you upgrade your megaCore function, the same files from the previous and current versions are present in the same Quartus II project, which causes a VHDL error.

### *Affected Configurations*

This issue affects all designs that were created in a previous version of the MegaCore function.

### *Workaround*

From your Quartus II project, remove the Device Design Files that were added by the earlier version of the MegaCore function. These files can be identified by the files' directory names.

### *Design Impact*

You cannot compile your Quartus II project until you remove the duplicate files.

### *Solution Status*

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controller Compiler.

## Quartus II Timing Analyzer Reports Incorrect Capture Cycles

If you load settings into the DDR Timing Wizard from the DDR or DDR2 SDRAM <variation name>\_ddr\_settings.txt file, you occasionally get incorrect values for the **Resynchronize read data in cycle** and **Postamble reset control clock in cycle** parameters.

### *Affected Configurations*

This issue only affects you if you use the DDR Timing Wizard to add timing constraints to DDR or DDR2 SDRAM MegaCore functions, and import the settings from the MegaCore settings file to the DDR Timing Wizard.

### *Design Impact*

The timing margins reported by the Quartus II Timing Analyzer will be wrong by a complete cycle.

### *Workaround*

Edit the **Resynchronize read data in cycle** and **Postamble reset control clock in cycle parameters** and add or remove a cycle to ensure correct timing analysis.

### *Solution Status*

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controller Compiler.

## **Using Regional Clocks**

Versions of the DDR or DDR2 SDRAM MegaCore function before v3.3.1 incorrectly allow the use of regional clocks for the datapath logic.

The static timing analysis performed after the design compiles requires that the all the clocks in the datapath are global, but this requirement is not checked version 3.2.0 or earlier.

### *Affected Configurations*

This issue affect designs that force the clocks going to the datapath logic onto regional clocks.

### *Design Impact*

Timing margins may be incorrect.

### *Workaround*

Do not use regional clocks for the datapath logic.

### *Solution Status*

Timing analysis will report an error for these designs in the Quartus II software v5.1 and later.

## **Some Timing Assignments Are Not Converted To HardCopy II Devices**

The Quartus II HardCopy® II migration tool gives warnings about assignments that are not convertible to HardCopy II devices.

When compiling a design that uses the DDR or DDR2 SDRAM MegaCore function, which targets a HardCopy II device, the Quartus II HardCopy II Netlist Writer gives warning messages because it ignores the `MAX_DATA_ARRIVAL_SKEW` assignments.

### *Affected Configurations*

This issue affects designs that use the DDR or DDR2 SDRAM MegaCore function, which target HardCopy II devices.

### *Workaround*

Ignore these messages because timing analysis for the interface is provided by the DDR Timing Wizard.



Contact Altera Support for more information on DDR and DDR2 SDRAM timing analysis for HardCopy II designs.

### *Solution Status*

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controller Compiler.

## **Error Message When Recompiling a Project**

If you move the directory containing your Quartus II project, or rename your Quartus II project and recompile it without regenerating the DDR or DDR2 SDRAM Controller, you may receive the following error:

```
Error: DDR timing cannot be verified until project has been successfully compiled.
```

This error indicates that some of the settings files contain references to the previous location or project name and the verify timing script is unable to find the current project.

### *Affected Configurations*

This issue affects all configurations.

### *Design Impact*

The timing script does not verify your design.

### *Workaround*

Regenerate your controller in IP Toolbench and recompile the project. The timing analysis script now completes correctly.

### *Solution Status*

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controller Compiler.

## **Remove Redundant Logic Cells Option (Stratix Devices Only)**

Do not turn on **Remove Redundant Logic Cells** in the Quartus II software if you are targeting Stratix devices.

### *Affected Configurations*

This issue affect all designs targeted at Stratix® devices, if you turn on **Remove Redundant Logic Cells** in the Quartus II software.

### *Design Impact*

For Stratix devices, removing redundant logic cells makes the Quartus II software optimize away the important DQS delay matching buffers that the postamble circuitry uses.

### *Workaround*

Ensure you turn off **Remove Redundant Logic Cells** in the Quartus II software if you are targeting Stratix devices.

### *Solution Status*

There are no plans to fix this issue.

## IP Toolbench Fails to Launch When Editing a Variation

In the MegaWizard® Plug-In Manager, when you select **Edit existing custom variation**, to edit an existing variation, IP Toolbench fails to launch.

### *Affected Configurations*

Variations that have **DQ bits per DQS pin** set to 4 and that have **Enable DQS mode** turned off.

### *Design Impact*

IP Toolbench cannot be launched to edit the variation.

### *Workaround*

Create a new variation with the new parameters or edit the top-level design file for your variation to change `value="1"` to `value="0"` in the following line:

```
// Retrieval info: <PRIVATE name = "enable_capture_clk" value="1"  
type="BOOLEAN" enable="1" />
```

When you relaunch IP Toolbench, you must then turn off **Enable DQS mode** and reselect your desired byte group constraints.

### *Solution Status*

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controller Compiler.

## SOPC Builder System Fails—Invalid Clock Frequency

You cannot edit or generate an SOPC Builder system when the clock frequency is specified with more than two decimal places.

### *Affected Configurations*

SOPC Builder designs that contain the DDR or DDR2 SDRAM Controller where the clock frequency is specified with more than two decimal places.

### *Design Impact*

IP Toolbench cannot be launched and the system cannot be generated.

### *Workaround*

Reduce the number of decimal places of the clock frequency in the SOPC Builder **Clock Settings** box to two or less places.

### *Solution Status*

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controller Compiler

## **SOPC Builder System Fails—Invalid Directory Name**

You cannot edit or generate an SOPC Builder system when the project directory contains spaces.

### *Affected Configurations*

SOPC Builder designs that contain the DDR or DDR2 SDRAM Controller where the project directory contains spaces.

### *Design Impact*

You cannot launch IP Toolbench and you cannot generate the SOPC Builder system.

### *Workaround*

Rename the project directory so that it does not have spaces in the name.

### *Solution Status*

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controller Compiler

## **Pin Planner HDL Syntax Error**

There is an HDL syntax error in Pin Planner-generated top-level design files that contain a DDR or DDR2 SDRAM Controller variation.

### *Affected Configurations*

Pin Planner-generated top-level design files that use a design that contains a DDR or DDR2 SDRAM Controller variation.

### *Design Impact*

If you import the DDR or DDR2 SDRAM Controller Pin Planner file into Pin Planner and then generate a top-level design file for your design, it contains an HDL syntax error and does not compile in the Quartus II software. You cannot use this top-level design file for IO Assignment Analysis.

### *Workaround*

Use the IP Toolbench top-level example design and automatically assigned constraints to verify your pin and IO assignments.

### *Solution Status*

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controller Compiler

## **Converting Stratix II Design to Stratix III Device Produces Error**

When you convert a Stratix II DDR or DDR2 SDRAM Controller design to Stratix III device, you see the following error `Cannot translate WYSIWYG DQS I/O.`

### *Affected Configurations*

Stratix II designs that have the **Insert logic to allow the DLL to update during the memory refresh period** turned on.

### *Design Impact*

The design does not compile in the Quartus II software.

### *Workaround*

Stratix III designs do not require the **Insert logic to allow the DLL to update during the memory refresh period** option and you should turn the option off before converting the design from a Stratix II to Stratix III design.

### *Solution Status*

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controller Compiler.

## SOPC Builder Supported Memory Data Bus Widths

SOPC Builder currently only supports data bus widths that are a power of 2. IP Toolbench does not impose these limitations in the SOPC Builder flow, and can therefore generate bus widths incompatible with SOPC builder, which results in the following error message during SOPC Builder system generation.

```
ERROR: slave data width (48) for slave ddr_sdram/s1 unexpected
```

### *Affected Configurations*

This issue affects all configurations that specify data bus widths that are not a power of two when you use the SOPC Builder flow.

### *Design Impact*

You cannot generate the design in SOPC Builder.

### *Workaround*

Ensure you restrict the data bus width parameter in the DDR SDRAM Controller IP Toolbench to a power of 2, for example, 8, 16, 32 or 64.

### *Solution Status*

This issue will be fixed in the next version of the DDR and DDR2 SDRAM Controller Compiler.

## Precompile Timing Estimates With Four or More DQS Delay Matching Buffers (Stratix Devices Only)

For Stratix devices, if you turn on **Manual postamble control** and choose 4 or more for the **Number of DQS delay matching buffers**, the pre-compile timing estimates in the system timing report for the read postamble enable property are incorrect. The correct timing analysis result is shown in the post-compile timing analysis report after compiling the design in the Quartus II software.

### *Affected Configurations*

This issue affects designs on Stratix devices that require four or more DQS delay matching buffers.

### *Design Impact*

This issue does not affect your design.

### *Workaround*

Ignore the pre-compile timing estimates in the system timing report for the read postamble enable property.

### *Solution Status*

This issue will be fixed in the next version of the DDR and DDR2 SDRAM Controller Compiler.

## **Illegal Byte Group Placements (Stratix & Stratix GX devices only)**

The IP Toolbench constraint editor allows you to place byte groups on both top and bottom of a Stratix or Stratix GX device at the same time, which causes an error in the Quartus II software. While you can split a DDR or DDR2 SDRAM interface across both the top and bottom of a Stratix device, some manual editing of the data path is required.

### *Affected Configurations*

This issue affects designs on Stratix and Stratix GX devices that split the interface across the top and bottom.

### *Design Impact*

The design does not compile.

### *Workaround*

For more information, contact Altera.

### *Solution Status*

This issue will never be fixed.

## **DQS I/O Pin Error (Cyclone Devices Only)**

Under some circumstances, the timing analysis may show that the design requires a dedicated resynchronization clock. The IP Toolbench-generated example top-level design does not automatically support a separate resynchronization clock on Cyclone® devices, which causes the following error message:

```
Error: DQS I/O pin <path name>cyclone_ddio_bidir:ddio_bidir[0]|ioatom must  
have a combinational output to the device  
Error: Can't fit design in device
```

### *Affected Configurations*

This issue affects Cyclone designs for which IP Toolbench recommends a separate resynchronization clock.

### *Design Impact*

The design does not compile.

### *Workaround*

Edit the example top-level design to instantiate a second PLL to provide a resynchronization clock with the IP Toolbench-recommended phase offset and connect this clock to the `resynch_clk` input of the controller.

### *Solution Status*

This issue will never be fixed.

## **Design Assistant Warning Messages**

The Quartus II Design Assistant generates warning messages when the design does not follow a Design Assistant rule, and generates information messages to provide information regarding a rule. If you enable the Design Assistant for a design containing a DDR or DDR2 SDRAM Controller, during compilation you will see the following messages for each of the following device families, which you can safely disregard.

### *Cyclone Devices*

#### **Medium**

```
Clock signal source should drive only input clock ports  
Node: altp11:altp11_component|_clk0
```

```
Clock signal source should drive only input clock ports  
Node: altp11:altp11_component|_clk1
```

```
Clock signal source should not drive registers that are triggered by  
different clock edges  
Node: altp11:altp11_component|_clk0
```

```
External reset should be synchronized using two cascaded registers  
Node: reset_n
```

### *Cyclone II Devices*

#### **Medium**

Clock signal source should drive only input clock ports  
Node: altp11:altp11\_component|\_clk0

Clock signal source should not drive registers that are triggered by different clock edges  
Node: altp11:altp11\_component|\_clk0

External reset should be synchronized using two cascaded registers  
Node: reset\_n

### *Stratix Devices*

#### **Medium**

Clock signal source should not drive registers that are triggered by different clock edges  
Node: altp11:altp11\_component|\_clk0

External reset should be synchronized using two cascaded registers reset\_n

Reset signal that is generated in one clock domain and used in other, asynchronous clock domains should be synchronized  
Node: dq\_enable\_reset[0]

### *Stratix II Devices*

#### **High**

Input clock pin should fan out to only one set of clock gating logic  
Node: altp11:altp11\_component|\_clk0

#### **Medium**

Clock signal source should drive only input clock ports  
Node: altp11:altp11\_component|\_clk0

Clock signal source should not drive registers that are triggered by different clock edges  
Node: altp11:altp11\_component|\_clk0

External reset should be synchronized using two cascaded registers  
Node: reset\_n

### *HardCopy II Devices*

#### **High**

Input clock pin should fan out to only one set of clock gating logic  
Node: altp11:altp11\_component|\_clk0

#### **Medium**

Clock signal source should drive only input clock ports  
Node: altp11:altp11\_component|\_clk0

Clock signal source should not drive registers that are triggered by different clock edges  
Node: altp11:altp11\_component|\_clk0

External reset should be synchronized using two cascaded registers  
Node: reset\_n

PLL drives multiple clock network types  
Node: altp11:altp11\_component|pll

### *Affected Configurations*

This issue affects all configurations.

### *Design Impact*

There is no design impact.

### *Workaround*

No workaround is necessary.

### *Solution Status*

This issue may be fixed in the next version of the Quartus II software and the DDR and DDR2 SDRAM Controller Compiler.

## IP Toolbench Generated Files List Is Incomplete

When you click Generate in IP Toolbench, it displays a list of the generated files in your project directory. This list is incomplete. The user guide shows the full list of generated files. [Table 2](#) shows the files that are missing from the IP Toolbench generated files list.

<b>Filename</b>	<b>Description</b>
<code>&lt;variation name&gt;_bb.v</code>	Verilog HDL black-box file for the MegaCore function variation. Use this file when using a third-party EDA tool to synthesize your design.
<code>&lt;variation name&gt;_auk_dds_datapath_pack.vhd</code> or <code>.v</code>	A VHDL package, which contains a component that the IP functional simulation model uses.
<code>&lt;variation name&gt;_dds_sdrsm_vsims.tcl</code>	The ModelSim simulation script.
<code>&lt;variation name&gt;_example_driver.vhd</code> or <code>.v</code>	The example driver.
<code>&lt;variation name&gt;_example_settings.txt</code>	The settings file for your variation, which the add constraints and the verify timing scripts use.
<code>auto_add_dds_constraints.tcl</code>	The add constraints script, which calls the variation-specific add constraints scripts.
<code>auto_verify_dds_timing_constraints.tcl</code>	The auto verify timing script, which calls the variation-specific verify timing scripts.
<code>dds_lib_path.tcl</code>	The Tcl library path file.
<code>dds_pll_fb_stratixii.vhd</code> or <code>.v</code>	Design file for the Stratix II feedback PLL.
<code>dds_pll_&lt;device name&gt;.vhd</code> or <code>.v</code>	Design file for the system PLL.
<code>generic_dds_dimm_model.vhd</code>	VHDL simulation file.
<code>generic_dds_sdrsm.vhd</code>	VHDL simulation file.
<code>generic_dds2_sdrsm.vhd</code>	VHDL simulation file.
<code>remove_constraints_for_&lt;variation name&gt;.tcl</code>	The remove constraints script for the variation.

### *Affected Configurations*

This issue affects all configurations.

### *Design Impact*

There is no design impact.

### *Workaround*

There is no workaround.

### Solution Status

This issue may be fixed in the next version of the DDR and DDR2 SDRAM Controller Compiler.

## Contact Information

For more information, contact Altera's mySupport website at [www.altera.com/mysupport](http://www.altera.com/mysupport) and click **Create New Service Request**. Choose the **Product Related Request** form.

## Revision History

Table 3 shows the revision history for the DDR and DDR2 SDRAM Controller Compiler v7.1.

Version	Date	Errata Summary
1.2	August 2007	Updated the following issues: <ul style="list-style-type: none"><li>● SOPC Builder Data and Address Width Errors</li><li>● ODT Launches Off System Clock</li></ul>
1.1	July 2007	Added the following issues: <ul style="list-style-type: none"><li>● SOPC Builder Data and Address Width Errors</li><li>● ODT Launches Off System Clock</li></ul>
1.0	May 2007	First release.



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