

This document addresses known errata and documentation issues for the DDR and DDR2 SDRAM High-Performance Controller MegaCore® functions version 7.0. Errata are functional defects or errors, which may cause the DDR and DDR2 SDRAM High-Performance Controller MegaCore functions to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

Table 1 shows the issues that affect the DDR and DDR2 SDRAM High-Performance Controller MegaCore functions v7.0.

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For the most up-to-date errata for this release, refer to the errata sheet on the Altera® website:

[www.altera.com/literature/es/es\\_ddr\\_ddr2\\_sdram\\_hp\\_61.pdf](http://www.altera.com/literature/es/es_ddr_ddr2_sdram_hp_61.pdf)

## DDR and DDR2 SDRAM High- Performance Controller v7.0 Issues

This section describes the DDR and DDR2 SDRAM High-Performance Controller MegaCore functions v7.0 issues.

### Data Corruption When Reading from External Memory Devices

There is an issue with the calibration sequencer logic block that can lead to data corruption when reading from external memory devices.

There is an error in the soft logic block that controls the voltage and temperature tracking (VT) mechanism of the ALTMEMPHY megafunction. Because the problem is dependent on voltage and

temperature, it affects only board-level functionality and does not affect design compilation or simulation. This problem is not due to any hardware issues.

### *Affected Configurations*

This issue affects all configurations.

### *Design Impact*

This issue can cause hardware failures in the supported devices including Stratix® II, Stratix II GX and Cyclone® III devices.

### *Workaround*

You should install the Quartus II software patch and the MegaCore IP Library patch before you take your design to production.



For the patch, refer to the [Altera Solutions page](#).

## **Simulating with the NCSim Software**

The DDR and DDR2 SDRAM High-Performance Controller MegaCore functions do not fully support the NCSim software.

### *Affected Configurations*

This issue affects all configurations.

### *Design Impact*

The design does not simulate.

### *Workaround*

Set the `-relax` switch for all calls to the VHDL analyzer.

### *Solution Status*

This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controller.

## **Simulating with the VCS Simulator**

The DDR and DDR2 SDRAM High-Performance Controller MegaCore functions do not fully support the VCS simulator.

### *Affected Configurations*

This issue affects all configurations.

### *Design Impact*

The design does not simulate.

### *Workaround*

The following workarounds exist.

### **VHDL**

Change the following code.

- In file `<variation name>_example_driver.vhd`, change all when statements between lines 333 and 503 from when `std_logic_vector'("<bit_pattern>")` to when `"<bit_pattern>"`.
- In file `testbench\<example name>_tb`, change line 191 from `signal zero_one(gMEM_BANK_BITS -1 downto 0) := (0 => '1', others => '0')` to `signal zero_one(gMEM_BANK_BITS -1 downto 0) := ('1', others=> '0')`.

### **Verilog HDL**

No changes are necessary. Calls to the Verilog analyzer sets the `+v2k` switch to enable Verilog 2000 constructs.

### *Solution Status*

This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controller.

## **Contact Information**

For more information, contact Altera's mySupport website at [www.altera.com/mysupport](http://www.altera.com/mysupport) and click **Create New Service Request**. Choose the **Product Related Request** form.

# Revision History

Table 2 shows the revision history for the DDR and DDR2 SDRAM High-Performance Controller v7.0.

**Table 2. DDR and DDR2 SDRAM High-Performance Controller v7.0 Errata Sheet Revision History**

Version	Date	Errata Summary
1.1	June 2007	Added Data Corruption When Reading from External Memory Devices issue
1.0	December 2006	First release.



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