



DDR & DDR2 SDRAM High-Performance Controller

July 2007, MegaCore Version 7.1 SP1

Errata Sheet

This document addresses known errata and documentation issues for the DDR and DDR2 SDRAM High-Performance Controller MegaCore® functions version 7.1 SP1. Errata are functional defects or errors, which may cause the DDR and DDR2 SDRAM High-Performance Controller MegaCore functions to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

Table 1 shows the issues that affect the DDR and DDR2 SDRAM High-Performance Controller MegaCore functions v7.1 SP1.

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For the most up-to-date errata for this release, refer to the errata sheet on the Altera® website:

www.altera.com/literature/es/es_ddr_ddr2_sdram_hp_71.pdf

DDR and DDR2 SDRAM High-Performance Controller v7.1 SP1 Issues

This section describes the DDR and DDR2 SDRAM High-Performance Controller MegaCore functions v7.1 SP1 issues.

Incorrect Constraints for Multiple Controllers

For designs that contain multiple DDR or DDR2 SDRAM high-performance controllers, the input clock timing constraints are not created correctly.

Affected Configurations

This issue affects all multiple controller designs.

Design Impact

Your design may not meet timing.

Workaround

Create the input clock timing constraints manually with a Synopsis Design Constraints file (.sdc) that creates a clock on the input of each of the PLLs inside each controller instantiation. Add this file to the project before the SDC file scripts that constrain the controller.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controller.

Timing Not Met

Designs that target Stratix II devices may not meet timing on the resynchronization and postamble paths in a default compilation.

Affected Configurations

This issue affects Stratix II designs.

Design Impact

Your design may not meet timing.

Workaround

Place the registers manually on the resynchronization and postamble paths close to the IO pins. Some designs may require additional modifications.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controller.

Timing Not Met—Multiple Controllers

designs that include multiple controllers and have the Use dedicated PLL outputs to drive memory clock turned on may give incorrect timing analysis for the DQS versus CK. Also the address and command paths may be incorrect. The setup and hold margins on these paths will be greater than a full cycle with a corresponding negative margin on the other side.

Affected Configurations

This issue affects multiple controller designs.

Design Impact

Your design may not meet timing.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controller.

Controller Does Not Work at Less Than 100 MHz

If you enter a frequency of less than 100 MHz in the MegaWizard Plug-In, you cannot generate a DDR or DDR2 SDRAM High-Performance controller.

Affected Configurations

This issue affects Cyclone III and Stratix II designs.

Design Impact

You cannot generate a design.

Workaround

There is no workaround.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controller.

ODT Pin Generation Critical Warning

When you compile a DDR SDRAM High-Performance Controller variation, the Quartus II software outputs the following message:

```
Critical Warning: Could not find pin of type addrcmd_2t from pattern
*my_ddr_odt_test_phy_alt_mem_phy_ciii_inst|\inst2:adc|\odt*:odt_struct|\
*:powerup_*:addr_pin|auto_generated|ddio_outa[0]|dataout
```

Affected Configurations

This issue affects all DDR SDRAM High-Performance Controllers v7.1 SP1.

Design Impact

There is no design impact.

Workaround

Ignore this message for DDR SDRAM designs—it is only valid for DDR2 SDRAM designs.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controller.

Latency Information Missing from the User Guide

The following latency information was missing from the user guide.

There are two types of latency that you must consider for memory controller designs—read and write latencies. We define the read and write latencies as follows.

- Read latency is the time it takes for the read data to appear at the local interface after you initiate the read request
- Write latency is the time it takes for the write data to appear at the memory interface after you initiate the write request

Latency calculations have the following assumptions:

- Reading and writing to the rows that are already open
- The `local_ready` signal is asserted high (no wait states)
- The latency is defined using the local side frequency and absolute time (ns)



For the half-rate controller the local side frequency is half the memory interface frequency; for the full rate controller it is equal to the memory interface frequency.

Altera defines the read and write latencies in terms of the local interface clock frequency and by the absolute time for the memory controllers.

Read latency has the following definition.

$$\text{Read latency} = \text{controller latency} + \text{command output latency} + \text{CAS latency} + \text{PHY read data input latency}$$

Write latency has the following definition:

$$\text{Write latency} = \text{controller latency} + \text{command output latency} + \text{write data latency}$$


Table 2 shows the read and write latency component definitions.

Table 2. Latency Definitions	
Term	Description
Controller latency	<code>local_read_req</code> to <code>control_doing_rd</code> .
Command output latency	<code>control_doing_rd</code> to <code>mem_cs_n</code> .
CAS latency	Read command to DQ data appearing on the bus.
PHY read data input latency	Read data that appears on the local interface.
Write data latency	Write data that appears on the memory interface.

Table 3 shows read and write latency derived from the write and read latency definitions for half and full-rate controllers and for Cyclone III, Stratix II, and Stratix III devices.

Table 3. Typical Latency

Device	Controller Rate	Frequency (MHz)	Latency Type	Latency (Cycles)	Latency (ns)
Cyclone III	Half	200	Read	$6 + 4 + 1.5 + 5.5 = 17$	85
			Write	$8 + 2 + 1 = 11$	55
	Full	167	Read	$5 + 3 + 3 + 8 = 19$	114
			Write	$8 + 0 + 2 = 10$	60
Stratix II	Half	333	Read	$6 + 4 + 1.5 + 8.5 = 20$	60
			Write	$8 + 2 + 1 = 11$	33
	Full	267	Read	$6 + 4 + 1.5 + 8.5 = 20$	75
			Write	$8 + 0 + 2 = 10$	37.5
Stratix III	Half	333	Read	$6 + 4 + 1.5 + 8.5 = 20$	60
			Write	$8 + 0 + 2 = 10$	30

 The latency depends on your precise configuration. You should obtain precise latency from simulation, but this figure may vary in hardware because of the automatic calibration process.

Simulating with the NCSim Software

The DDR and DDR2 SDRAM High-Performance Controller MegaCore functions do not fully support the NCSim software.

Affected Configurations

This issue affects all configurations.

Design Impact

The design does not simulate.

Workaround

Set the `-relax` switch for all calls to the VHDL analyzer.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controller.

Simulating with the VCS Simulator

The DDR and DDR2 SDRAM High-Performance Controller MegaCore functions do not fully support the VCS simulator.

Affected Configurations

This issue affects all configurations.

Design Impact

The design does not simulate.

Workaround

The following workarounds exist.

VHDL

Change the following code.

- In file *<variation name>_example_driver.vhd*, change all when statements between lines 333 and 503 from when `std_logic_vector'("<bit_pattern>")` to when `"<bit_pattern>"`.
- In file `testbench\<example name>_tb`, change line 191 from `signal zero_one(gMEM_BANK_BITS -1 downto 0) := (0 => '1', others => '0')` to `signal zero_one(gMEM_BANK_BITS -1 downto 0) := ('1', others=> '0')`.

Verilog HDL

No changes are necessary. Calls to the Verilog analyzer sets the +v2k switch to enable Verilog 2000 constructs.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controller.

Simulating VHDL Designs using SOPC Builder

The DDR and DDR2 SDRAM High-Performance Controller fail to simulate correctly in some VHDL configurations when using the **Run As ModelSim** feature in the Nios II IDE software.

Affected Configurations

This issue affects Stratix III VHDL designs and Cyclone III VHDL designs. All Verilog HDL designs and other device families are unaffected.

Design Impact

The design does not simulate correctly.

Workaround

For Stratix III VHDL designs, edit the SOPC Builder-generated testbench which is at the end of the file that contains your SOPC Builder system. For example, if your SOPC Builder system is **my_sopc_sys**, edit the **my_sopc_sys.vhd** file and search for the **test_bench** entity.

On the instantiation of **my_sopc_sys**, change the connection on the **global_reset_n_to_the_altmemddr** port from:

```
global_reset_n_to_the_altmemddr =>  
global_reset_n_to_the_altmemddr,
```

to:

```
global_reset_n_to_the_altmemddr => reset_n,
```

For Cyclone III VHDL designs, edit the SOPC Builder-generated testbench, which is at the end of the file that contains your SOPC Builder system. For example, if your SOPC Builder system is **my_sopc_sys**, edit the **my_sopc_sys.vhd** file and search for the **test_bench** entity.

Insert the following line into the testbench:

```
mem_dq_to_and_from_the_altmemddr <= (others => 'L');
```

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controller.

Simulating Designs with “Enable User-Controlled Refresh” Option

The example top-level design fails to simulate correctly if you turn on **Enable user-controlled refresh**.

Affected Configurations

This issue affects all designs with the **Enable user-controlled refresh** option.

Design Impact

The design does not simulate correctly.

Workaround

Edit the example top-level design file to add your own logic to generate periodic refresh requests to the drive `local_refresh_req` input of the DDR or DDR2 SDRAM High-Performance Controller. For example, if you created a controller `my_controller`, edit the `my_controller_example_top.v(hd)` file.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controller.

Compilation Fails

The example top-level design fails to compile correctly if you turn on **Enable external access to reconfigure PLL prior to calibration**.

Affected Configurations

This issue affects Stratix II designs with the **Enable external access to reconfigure PLL prior to calibration** option.

Design Impact

The design does not compile.

Workaround

Edit the example top-level design file to add the PLL reconfiguration ports to the instantiation of the DDR/DDR2 SDRAM High-Performance Controller. For example, if you created a controller **my_controller**, edit the **my_controller_example_top.v(hd)** file and search for the instantiation of **my_controller**.

Add the following connections to the instantiation (and for VHDL, the component).

```
.pll_reconfig_enable      (pll_reconfig_enable),
.pll_reconfig_write_param (pll_reconfig_write_param),
.pll_reconfig_read_param  (pll_reconfig_read_param),
.pll_reconfig             (pll_reconfig),
.pll_reconfig_counter_type (pll_reconfig_counter_type),
.pll_reconfig_counter_param (pll_reconfig_counter_param),
.pll_reconfig_data_in     (pll_reconfig_data_in),
.pll_reconfig_busy        (pll_reconfig_busy),
.pll_reconfig_data_out    (pll_reconfig_data_out),
.pll_reconfig_clk         (pll_reconfig_clk),
.pll_reconfig_reset       (pll_reconfig_reset)
```

You should also implement the appropriate logic to drive these signals.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controller.

Contact Information

For more information, contact Altera's mySupport website at www.altera.com/mysupport and click **Create New Service Request**. Choose the **Product Related Request** form.

Revision History

Table 4 shows the revision history for the DDR and DDR2 SDRAM High-Performance Controller v7.1 SP1.

Version	Date	Errata Summary
1.3	July 2007	Added the following issues: <ul style="list-style-type: none"> ● Incorrect Constraints for Multiple Controllers ● Timing Not Met ● Timing Not Met—Multiple Controllers ● Controller Does Not Work at Less Than 100 MHz
1.2	July 2007	Added the ODT Pin Generation Critical Warning issue

Table 4. DDR and DDR2 SDRAM High-Performance Controller v7.1 SP1 Errata Sheet Revision History

Version	Date	Errata Summary
1.1	June 2007	Added the following issues: <ul style="list-style-type: none"> • Latency Information Missing from the User Guide • Simulating VHDL Designs using SOPC Builder • Simulating Designs with "Enable User-Controlled Refresh" Option • Compilation Fails
1.0	May 2007	First release.



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