

This document addresses known errata and documentation changes for DSP Builder version 7.0. Errata are functional defects or errors which may cause DSP Builder to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

DSP Builder v7.0 Issues

Table 1 shows the issues that affect DSP Builder, version 7.0.

<i>Table 1. DSP Builder v7.0 Issues</i>	
Issue	Page
Error When Directory Pathname is a Network UNC Path	1
State Machine VHDL Incorrect if Logic Operator used as Input	2
SOPC Builder Files Not Added to the Quartus II Project	2
Clock Information Incorrect in VEC File for Multi-Clock Designs	3
HIL Simulation Stays at Zero if Global Reset is set to Active Low	3
SignalTap II Analyzer Cannot Plot a 64-bit Bus Signal	4
VIP Suite v1.0 is Not Supported in v7.0 of DSP Builder	4
Multiclock Designs May Not Simulate Correctly in ModelSim	5
Signed Fractional HIL Simulation is Incorrect	6
Unique Entity Names Option Cannot be Unset	6
VHDL for Black Box Not in Generated Scripts	7
Previous DSP Builder Path Not Removed	7



For the most up-to-date errata for this release, refer to the errata page on the Altera website:

www.altera.com/literature/es/es_dsp_builder_70.pdf

Altera has identified the following issues in DSP Builder version 7.0.

Error When Directory Pathname is a Network UNC Path

DOS commands invoked from within a m-script cannot resolve a UNC path to a remote file system.

Affected Configurations

All configurations are affected.

Design Impact

An error is issued when you attempt to run Signal Compiler.

Workaround

Map the network UNC path to a local drive.

Solution Status

This issue is due to a limitation in MATLAB.

State Machine VHDL Incorrect if Logic Operator used as Input

When state machine VHDL is generated, the expression strings for the port names are replaced by signals named <port name>_sig. This replacement can interfere with the expression logic. For example, if you have an AND statement and a port named A, then AND is replaced by A_sigAND in the generated VHDL. Similar problems occur if AN, AND, O or OR are used as input names.

Affected Configurations

All configurations are affected.

Design Impact

Invalid VHDL is generated.

Workaround

Avoid using inputs named A, AN, AND, O or OR.

Solution Status

This issue will be fixed in a future release of DSP Builder.

SOPC Builder Files Not Added to the Quartus II Project

An SOPC Builder component created in DSP Builder does not add all the necessary files to the project when instantiated in the Quartus II software.

Affected Configurations

Any SOPC Builder component created by DSP Builder in a directory other than the directory containing the Quartus II project from where the component will be used.

Design Impact

Compilation in the Quartus II software fails at Analysis & Synthesis because it fails to find all the source files for the DSP Builder design.

Workaround

Manually add the missing files to the Quartus II project.

Solution Status

This issue will be fixed in a future release of DSP Builder.

Clock Information Incorrect in VEC File for Multi-Clock Designs

The VEC file generated by SignalCompiler for multi-clock designs does not contain the correct clock information.

Affected Configurations

All configurations are affected.

Design Impact

The design will fail in Quartus II simulation.

Workaround

None.

Solution Status

This issue will be fixed in a future release of DSP Builder.

HIL Simulation Stays at Zero if Global Reset is set to Active Low

Hardware-in-the-Loop (HIL) simulation stays at zero if a global reset is used and set to `Active Low`.

Affected Configurations

This issue affects designs that require a global reset and are used for HIL simulation.

Design Impact

The hardware simulation may not give the correct results.

Workaround

Select an `Active High` global reset in SignalCompiler and assert `SCLR` before starting the simulation in the HIL dialog box parameters before running HIL simulation.

Solution Status

This issue will be fixed in a future release of DSP Builder.

SignalTap II Analyzer Cannot Plot a 64-bit Bus Signal

If you try to observe a signal bus with more than 64 bits using SignalTap II in DSP Builder, an error occurs during MATLAB plotting.

Affected Configurations

All configurations are affected.

Design Impact

The M-file, `xxx_group_plot.m`, created by SignalTap II has an incorrect axis range setting command.

Workaround

Use a `BusConversion` block to split the bus into two buses with less than 64 bits and monitor each bus with a separate SignalTap II block.

Solution Status

This issue will be fixed in a future release of DSP Builder.

VIP Suite v1.0 is Not Supported in v7.0 of DSP Builder

The MegaCore functions in version 1.0 of the Video and Image Processing (VIP) Suite are not compatible with version 7.0 of DSP Builder.

Affected Configurations

This issue affects all configurations.

Design Impact

The MegaCore functions in version 1.0 of the Video and Image Processing Suite fail to launch the MegaWizard® Plug-In Manager in version 7.0 of DSP Builder. This is because the hardware generation engine used by these MegaCore functions has been changed to significantly reduce generation times.

Workaround

Install version 7.0 of the Video and Image Processing Suite and replace any existing blocks using these functions by the new versions.

Solution Status

Future versions of the MegaCore functions in the Video and Image Processing Suite will be supported by the current and previous primary release of the Quartus® II software tools including DSP Builder.

Multiclock Designs May Not Simulate Correctly in ModelSim

Some multiclock designs may not simulate correctly in ModelSim.

Affected Configurations

All configurations are affected.

Design Impact

When a design involves a clock rate change from low to high, the `.salt` file could be in the lower rate clock domain. If the outputs to be monitored are in the high clock rate domain, the `.salt` file will be misinterpreted in the testbench causing simulation in ModelSim to be incorrect.

Workaround

None.

Solution Status

This issue will be fixed in a future release of DSP Builder.

Signed Fractional HIL Simulation is Incorrect

Hardware-in-the-loop (HIL) signed fractional simulation does not match the non-HIL simulation.

Affected Configurations

All configurations are affected.

Design Impact

HIL simulation matches the non-HIL simulation in a signed integer design but does not match in a signed fractional version of the design.

Workaround

The HIL (and HDL Import) blocks require integer inputs and outputs. Insert Binary Point Casting blocks at the inputs and outputs to convert between signed fractional and integer signal types.

Solution Status

This issue will be fixed in a future release of DSP Builder.

Unique Entity Names Option Cannot be Unset

The option in SignalCompiler to generate unique hierarchical names cannot easily be unset.

Affected Configurations

All configurations are affected.

Design Impact

When running SignalCompiler, the analyze stage has a check box for **Hierarchical VHDL entity names are unique**. Once turned on, this setting can not be easily turned off, as it makes changes to the model.

Workaround

The unique names option is disabled in version 7.0. However, it can be enabled by setting the following MATLAB workspace variable:
`dspbuilder_enable_unique_hierarchy_name = true;`

Solution Status

This issue will be fixed in a future release of DSP Builder.

VHDL for Black Box Not in Generated Scripts

The VHDL source code for black box blocks is not included in the generated scripts.

Affected Configurations

All configurations are affected.

Design Impact

When SignalCompiler generates Tcl scripts for the Quartus® II software and all 3rd party synthesis and simulation tools, the VHDL source code for the top level is included. However, VHDL source code for any black boxes in the design is not included.

Workaround

Manually edit the Tcl scripts to include VHDL source code for all black box sources in the design. If any VHDL source refers to any special libraries, those libraries also need to be included with appropriate compiler directives.

Solution Status

This issue will be fixed in a future release of DSP Builder.

Previous DSP Builder Path Not Removed

If DSP Builder version 5.0 has been previously installed then its path will not be removed from the MATLAB path list when DSP Builder version 5.0 is un-installed.

Affected Configurations

Configurations which have been updated from DSP Builder version 5.0.

Design Impact

Error messages are issued due to library objects existing at more than one location.

Workaround

The DSP Builder path for version 5.0 was written to a **startup.m** file in the MATLAB installation (for example: *<MATLAB install directory> \toolbox\local\startup.m*). You should manually comment out (using the % character) or remove the DSP Builder path specified in this file. For example:

```
%path(path, 'C:\altera\DSPBuilder\AltLib');
```

Solution Status

This issue will be fixed in a future release of DSP Builder.

Contact Information

For more information, contact Altera's mySupport website at www.altera.com/mysupport and click **Create New Service Request**. Choose the **Product Related Request** form.

Revision History

Table 2 shows the revision history for the *DSP Builder 7.0 Errata Sheet*.

<i>Table 2. DSP Builder Errata Sheet Version 7.0 Revision History</i>		
Version	Date	Errata Summary
1.0	March 2007	New document for DSP Builder 7.0.
1.1	March 2007	Added errata for “Error When Directory Pathname is a Network UNC Path” and “State Machine VHDL Incorrect if Logic Operator used as Input”



101 Innovation Drive
 San Jose, CA 95134
www.altera.com
 Literature Services:
literature@altera.com

Copyright © 2007 Altera Corporation. All rights reserved. Altera, The Programmable Solutions Company, the stylized Altera logo, specific device designations, and all other words and logos that are identified as trademarks and/or service marks are, unless noted otherwise, the trademarks and service marks of Altera Corporation in the U.S. and other countries. All other product or service names are the property of their respective holders. Altera products are protected under numerous U.S. and foreign patents and pending applications, maskwork rights, and copyrights. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera Corporation. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

