

This document addresses known errata and documentation changes for the DSP Builder software v7.1 SP1. Errata are functional defects or errors which may cause DSP Builder to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

## DSP Builder, v7.1 SP1 Issues

Table 1 shows the issues that affect DSP Builder, v7.1 SP1.

<i>Table 1. DSP Builder v7.1 SP1 Issues</i>	
Issue	Page
HIL Design Stays in Reset During Simulation	1
ena Port on Counter Block is Incorrectly Connected	2
Development Board Output Clocks Missing in VHDL	2
Cannot Initialize RAM From HEX Files if Widths are Different	3
Dual-Clock FIFO Simulation Does Not Match ModelSim	4
Error When Directory Pathname is a Network UNC Path	4
State Machine VHDL Incorrect if Logic Operator used as Input	5



For existing up-to-date errata, refer to the *DSP Builder, v7.1 Errata Sheet* on the [Errata Sheets](#) page of the Altera literature website.

Altera has identified the following issues in DSP Builder, v7.1 SP1.

### HIL Design Stays in Reset During Simulation

An asynchronous reset is permanently asserted for a Hardware-in-the-Loop (HIL) design.

#### *Affected Configurations*

All HIL configurations are affected.

#### *Design Impact*

When running a HIL design in Simulink, the output always returns 0.

### *Workaround*

For a v7.1 design, add a Clock block to the original MDL and set `ac1r` to *Active High*. Recompile both the original version and HIL version. The simulation then works as expected.

For a v7.1 SP1 design, you can use the `alt_dspb_hil_reset` workspace variable to specify an active low (0) or active high (1) reset.

### *Solution Status*

This issue will be fixed in a future release of DSP Builder so that the required reset setting is automatically detected.

## **ena Port on Counter Block is Incorrectly Connected**

In v6.1, the `ena` port was connected to the clock enable (`clk_ena`) on the LPM. However, in v7.1, it is connected to the count enable (`cnt_ena`).

### *Affected Configurations*

All configurations are affected.

### *Design Impact*

`sload` loads data while not enabled.

### *Workaround*

Modify the input to the `sload` port by ANDing the synchronous load signal with the enable signal into this port (to make sure that you are not performing a synchronous load while the enable is low).

### *Solution Status*

This issue will be fixed in a future release of DSP Builder.

## **Development Board Output Clocks Missing in VHDL**

In DSP Builder v7.0 or earlier, one or more PLLs are automatically included to provide output clocks which are listed in the top level VHDL, with the clock locations assigned to the selected pins from the board configuration block.

In v7.1, PLL are not automatically added in the design to produce the required clock outputs.

### *Affected Configurations*

All configurations are affected.

### *Design Impact*

The clock outputs selected from the board configuration block do not appear in the top level of the generated VHDL.

### *Workaround*

Add PLL blocks into your design and configure them to provide the required output clocks. The PLL output clocks need to be exported for them to appear in the VHDL top level.

You can assign locations to the pins by creating a Tcl script named `<pll_clock_pins>_add.tcl` in the `DSPBuilder_<design_name>_import` folder within the design folder. The following example shows the required assignments for the `Test2S60Board.mdl` design example:

```

set_location_assignment PIN_C16 -to PLL_clk0_out
set_location_assignment PIN_B15 -to PLL_clk1_out
set_location_assignment PIN_B18 -to PLL_clk2_out
set_location_assignment PIN_D18 -to PLL_clk3_out
set_location_assignment PIN_D16 -to PLL_clk4_out
set_location_assignment PIN_C15 -to PLL_clk5_out

```

### *Solution Status*

This issue will be fixed in a future release of DSP Builder.

## **Cannot Initialize RAM From HEX Files if Widths are Different**

You cannot initialize the Single-Port RAM, Dual-Port RAM, True Dual-Port RAM, or ROM blocks using an Intel format HEX file unless the widths in the HEX file and on the block are the same or a multiple of 8.

### *Affected Configurations*

All configurations are affected.

### *Design Impact*

An exception is issued.

### *Workaround*

Set the block width to be the same or a value divisible by 8. For example, if you want a width of 65, set it to 72 instead. This will then not give an exception. In general, make sure that the data width in any initialization HEX file is identical to the data width specified for the block. A warning is issued if this is not the case and the simulation results may not be the same as hardware. Note that you can quickly compare the simulation results with hardware using a TestBench block.

### *Solution Status*

This issue will be fixed in a future release of DSP Builder.

## **Dual-Clock FIFO Simulation Does Not Match ModelSim**

The Dual-Clock FIFO simulation in Simulink is functionally equivalent to hardware, but not cycle-accurate.

### *Affected Configurations*

Most configurations are affected.

### *Design Impact*

The delay between the write-side adding data and the read-side seeing it, and between the read-side clearing space in the FIFO and the write-side seeing it, does not match hardware.

### *Workaround*

Do not rely on these timing characteristics for correctness of a design.

### *Solution Status*

This issue will be fixed in a future release of DSP Builder.

## **Error When Directory Pathname is a Network UNC Path**

DOS commands invoked from within a m-script cannot resolve a UNC path to a remote file system.

### *Affected Configurations*

All configurations are affected.

### *Design Impact*

An error is issued when you attempt to run a MATLAB script. This affects Signal Compiler, MegaCore function, HDL import, functional simulation, hardware-in-the-loop and the state machine block.

### *Workaround*

Map the network UNC path to a local drive.

### *Solution Status*

This issue is due to a limitation in MATLAB.

## **State Machine VHDL Incorrect if Logic Operator used as Input**

When state machine VHDL is generated, the expression strings for the port names are replaced by signals named <port name>\_sig. This replacement can interfere with the expression logic. For example, if you have an AND statement and a port named A, then AND is replaced by A\_sigAND in the generated VHDL. Similar problems occur if AN, AND, O or OR are used as input names.

### *Affected Configurations*

All configurations are affected.

### *Design Impact*

Invalid VHDL is generated.

### *Workaround*

Avoid using inputs named A, AN, AND, O or OR.

### *Solution Status*

This issue will be fixed in a future release of DSP Builder.

## **Contact Information**

For more information, contact Altera's mySupport website at [www.altera.com/mysupport](http://www.altera.com/mysupport) and click **Create New Service Request**. Choose the **Product Related Request** form.

**Revision History** Table 2 shows the revision history for the *DSP Builder, v7.1 Errata Sheet*.

<i>Table 2. DSP Builder Errata Sheet v7.1 Revision History</i>		
<b>Version</b>	<b>Date</b>	<b>Errata Summary</b>
1.1	June 2007	Updated for DSP Builder v7.1 SP1.
1.0	May 2007	New document for DSP Builder v7.1.



101 Innovation Drive  
 San Jose, CA 95134  
[www.altera.com](http://www.altera.com)  
**Literature Services:**  
[literature@altera.com](mailto:literature@altera.com)

Copyright © 2007 Altera Corporation. All rights reserved. Altera, The Programmable Solutions Company, the stylized Altera logo, specific device designations, and all other words and logos that are identified as trademarks and/or service marks are, unless noted otherwise, the trademarks and service marks of Altera Corporation in the U.S. and other countries. All other product or service names are the property of their respective holders. Altera products are protected under numerous U.S. and foreign patents and pending applications, maskwork rights, and copyrights. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera Corporation. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

