

This document addresses known errata and documentation issues for the FFT MegaCore® function version 7.1. Errata are functional defects or errors, which may cause the FFT MegaCore function to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents. [Table 1](#) shows the issues that affect the FFT MegaCore function v7.1.

<i>Table 1. FFT MegaCore function v7.1 Issues</i>	
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For the most up-to-date errata for this release, refer the errata sheet on the Altera® website:

www.altera.com/literature/es/es_fft_71.pdf

FFT MegaCore Function v7.1 Issues

This section describes the FFT MegaCore function v7.1 issues.

Incorrect Timing Diagrams in the User Guide

The following figures are incorrect in the user guide:

- Figure 3-3
- Figure 3-4
- Figure 3-12
- Figure 3-15

[Figures 1 to 4](#) show the correct figures.

Figure 1. FFT Streaming Data Flow Architecture Simulation

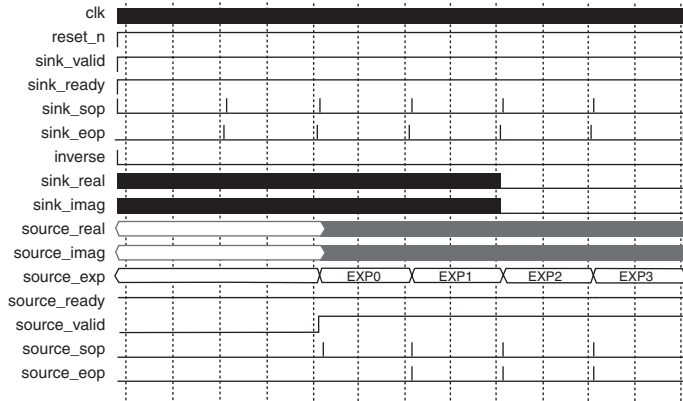


Figure 2. FFT Streaming Data Flow Architecture Input Flow Control

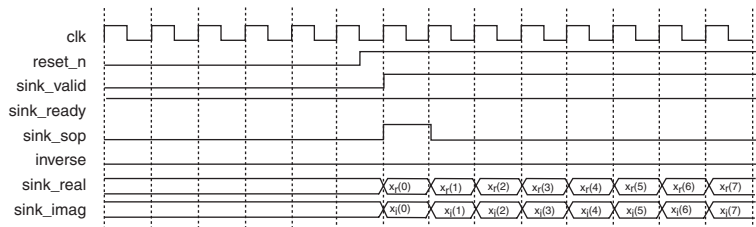


Figure 3. FFT Buffered Burst Data Flow Architecture Simulation

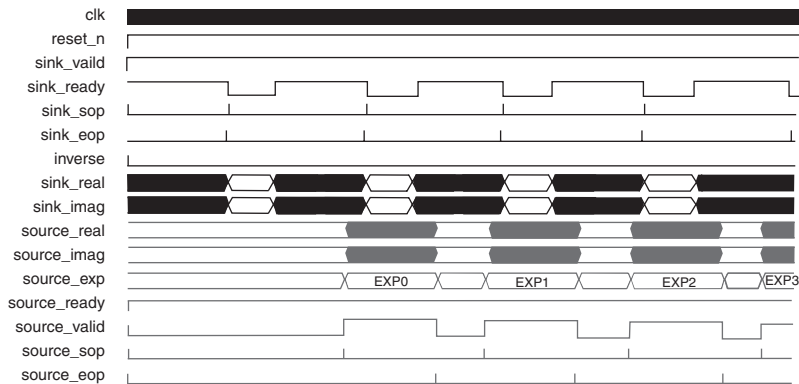
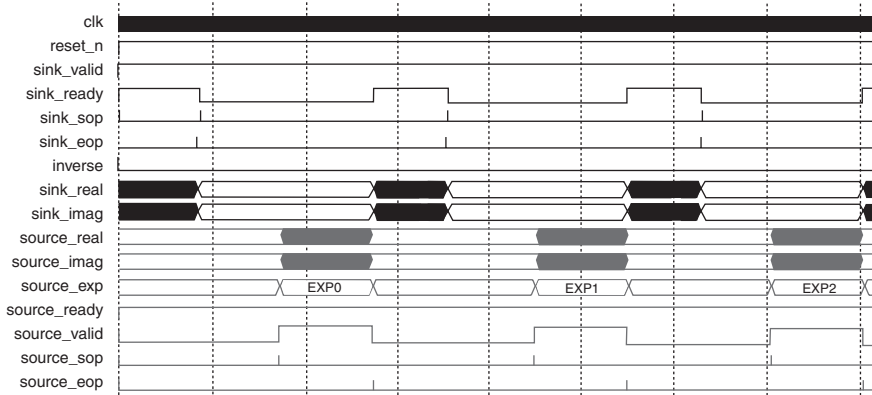


Figure 4. FFT Burst Data Flow Architecture Simulation

IP Toolbench Fails to Generate a .bsf File

IP Toolbench fails to generate the Quartus® II block symbol file (.bsf) for some configurations of the FFT MegaCore function.

Affected Configurations

This issue affects all configurations using the streaming, burst, or buffered burst architectures when the top-level output file type is VHDL.

Design Impact

There is no design impact. The design compiles and simulates correctly.

Workaround

To generate the .bsf file, select the top-level output file type as Verilog HDL. Continue to parameterize and generate the MegaCore function as required. When the IP Toolbench generates a .bsf file, you may switch back to using a VHDL top-level design.

Solution Status

This issue will be fixed in a future version of the FFT MegaCore function.

Simulation Errors—Synopsys VCS

When you use NativeLink to perform an RTL simulation using the generated Verilog HDL testbench in the VCS simulator, you see the following error:

```
Error: VCS: Error-[V2KS] Verilog 2000 IEEE 1364-2000 syntax used. Please
compile with +v2k
Error: VCS:      to support this construct
Error: VCS:      operator '**' .
```

Affected Configurations

This issue affects all Verilog HDL configurations.

Design Impact

There is no design impact; the design compiles correctly.

Workaround

In the Verilog HDL testbench `<variation name>_tb.v`, replace the power of operator '**' with the calculated value. Alternatively, compile with the +v2k option in the VCS simulator.

Solution Status

This issue will be fixed in a future version of the FFT MegaCore function.

Simulation Errors—Incorrect Results

When the input is defined as N bit wide, the permissible input range is from $-2^{N-1} + 1$ to $2^{N-1} - 1$. If the input contains the value -2^{N-1} , the HDL output is incorrect, and does not match the MATLAB simulation result.

Affected Configurations

This issue affects all configurations.

Design Impact

The design compiles but gives incorrect results.

Workaround

If you expect your input signal to contain the value -2^{N-1} , you should add a block in front of the FFT, which maps the value -2^{N-1} to $-2^{N-1} + 1$.

Solution Status

This issue will be fixed in a future version of the FFT MegaCore function.

Simulation Errors—MATLAB Model Mismatch

For one particular FFT parameter combination, the HDL output does not match the MATLAB simulation results (for some frames of data).

HDL simulation results are scaled down by a factor of two compared to the MATLAB simulation results. The exponent value produced by the HDL simulation is one less than the output of the MATLAB simulations. When the exponent is taken into account, the MATLAB and the HDL version may differ by one least significant bit (LSB).

Affected Configurations

This issue affects the following parameter combination:

- Transform length: 64
- I/O data flow: burst architecture
- FFT engine architecture: quad output
- Number of parallel engines: 2

Design Impact

There is no design impact, the design compiles and operates correctly.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the FFT MegaCore function.

Gate-Level Simulations

The testbench provided with the FFT MegaCore function is not suitable for gate-level simulations. The testbench assumes zero delays in post-fitting simulation models. Therefore, running gate-level simulations using the testbench may produce incorrect simulation results.

Affected Configurations

This issue affects all configurations.

Design Impact

There is no design impact; the design compiles correctly.

Workaround

Provide appropriate input and output constraints using the Quartus® II Assignments Editor and create a testbench that matches these requirements.

Solution Status

This issue will be fixed in a future version of the FFT MegaCore function.

Contact Information

For more information, contact Altera's mySupport website at www.altera.com/mysupport and click **Create New Service Request**. Choose the **Product Related Request** form.

Revision History

Table 2 shows the revision history for FFT MegaCore function version 7.1.

Version	Date	Errata Summary
1.1	May 2007	Added the following issues: <ul style="list-style-type: none">● Incorrect Timing Diagrams in the User Guide● IP Toolbench Fails to Generate a .bsf File
1.0	May 2007	First release.



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