

This document addresses known errata and documentation issues for the POS-PHY Level 2 and 3 Compiler version 7.1. Errata are functional defects or errors, which may cause the POS-PHY Level 2 and 3 Compiler to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents. **Table 1** shows the issues that affect the POS-PHY Level 2 and 3 Compiler v7.1.

<i>Table 1. POS-PHY Level 2 and 3 Compiler v7.1 Issues</i>	
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For the most up-to-date errata for this release, refer to the errata sheet on the Altera® website:

www.altera.com/literature/es/es_posphy_l2_l3_71.pdf

POS-PHY Level 2 & 3 Compiler v7.1 Issues

This section describes the POS-PHY Level 2 and 3 Compiler v7.1 issues.

IP Toolbench Incorrect Behavior

In the IP Toolbench Parameterize window, after you click **Finish**, if you click **Parameterize** to review your settings, the options show incorrect behavior.

Affected Configurations

This issue affects all configurations.

Design Impact

There is no design impact.

Workaround

When you click **Finish**, ensure you close IP Toolbench (which cancels any changes) or click **Generate**. You can view the parameterize window again by reopening IP Toolbench.

Solution Status

This issue will be fixed in a future release of the POS-PHY Level 2 and 3 Compiler.

Errors with Pin Planner Top-Level File

When you compile a Quartus® II Pin Planner-generated top-level file you receive errors.

Affected Configurations

This issue affects all configurations.

Design Impact

The design does not compile.

Workaround

Do not use Pin Planner with the POS-PHY Level 2 and 3 Compiler.

Solution Status

This issue will be fixed in a future release of the POS-PHY Level 2 and 3 Compiler.

Master Sink Atlantic Enable Output Signal Does Not Respond to Reset

The `bN_ena` output signals on the Atlantic™ master sink interfaces are not guaranteed to be zero during reset (`bN_reset_n` low). Instead, these signals reflect the value of the `bN_dav` input signals.

Affected Configurations

This issue affects any POS-PHY Level 2 and 3 source variation that uses an Atlantic master sink interface on the B-side—in version or previous versions of the POS-PHY Level 2 and 3 Compiler.

Design Impact

The `bN_ena` signal may be asserted despite the assertion of the `bN_reset_n` signal. If your Atlantic source slave logic asserts the `bN_dav` while the POS-PHY Level 2 and 3 MegaCore[®] function is in reset, the MegaCore function inadvertently begins to read data from the sink logic. The data read is not stored in the MegaCore function's buffers nor is it transmitted, which results in lost data.

Workaround

The workaround consists of ensuring that the `bN_dav` input to the MegaCore function holds the desired value for `bN_ena` while the MegaCore function is in reset.

This workaround can be implemented in many ways, including the following:

1. Ensure that the Atlantic slave source logic is reset while the MegaCore function is in reset.

or

2. Drive the `bN_dav` input signal from a flip-flop reset by `bN_reset_n` and fed by your desired `dav` signal.

Solution Status

This issue will be fixed in a future release of the POS-PHY Level 2 and 3 Compiler.

Contact Information

For more information, contact Altera's mySupport website at www.altera.com/mysupport and click **Create New Service Request**. Choose the **Product Related Request** form.

Revision History

Table 2 shows the revision history for *POS-PHY Level 2 & 3 Compiler v7.1 Errata Sheet*.

<i>Table 2. POS-PHY Level 2 & 3 Compiler v7.1 Errata Sheet Revision History</i>		
Version	Date	Errata Summary
1.0	May 2007	First release.



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