

This document addresses known errata and documentation issues for the QDRII SRAM Controller MegaCore® function version 7.1. Errata are functional defects or errors, which may cause the QDRII SRAM Controller MegaCore function to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

Table 1 shows the issues that affect the QDRII SRAM Controller MegaCore function v7.1.

<i>Table 1. QDRII SRAM Controller MegaCore Function v7.1 Issues</i>	
<b>Issue</b>	<b>Page</b>
Wide Mode is Nonoperational	2
Incorrect IP Toolbench Latency Behavior	2
Simulating with the VCS Simulator	3
TimeQuest Timing Analyzer Failure	3
PLL Placement	4
Constraints Errors With Companion Devices	4
Supported Device Families	5
No Description of Datapath Signals	6
Changing HDL	6
Compilation Error (Stratix II Series & HardCopy II Devices Only)	7
Gate-Level Simulation Filenames	7
The ModelSim Script Does Not Support Companion Devices	8



For the most up-to-date errata for this release, refer to the errata page on the Altera® website:

[www.altera.com/literature/es/es\\_qdrii\\_sram\\_71.pdf](http://www.altera.com/literature/es/es_qdrii_sram_71.pdf)

## QDRII SRAM Controller MegaCore Function v7.1 Issues

This section describes the QDRII SRAM Controller MegaCore function v7.1 issues.

### Wide Mode is Nonoperational

If you select wide mode in IP Toolbench and generate a core, you end up with a nonoperational QDRII SRAM controller.

#### *Affected Configurations*

This issue affects all configurations with wide mode.

#### *Design Impact*

The design is nonoperational.

#### *Workaround*

This issue has no workaround.

#### *Solution Status*

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

### Incorrect IP Toolbench Latency Behavior

When you open the IP Toolbench Parameterize window, you can select any latency for the default **QDRII**, but it only supports 1.5.

#### *Affected Configurations*

This issue affects all QDRII SRAM configurations.

#### *Design Impact*

IP Toolbench does not generate a variation and gives the following error message:

```
Megacore Function Generation Error
```

```
IP Functional Simulation creation Failed. The following error was returned:
```

```
Error: Top-level design entity "qdr_auk_qdrii_sram_avalon_controller_ipfs_wrap" is undefined.
```

### *Workaround*

For longer latency, select **QDRII+**.

### *Solution Status*

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

## **Simulating with the VCS Simulator**

The QDRII SRAM Controller MegaCore function v7.1 does not support the VCS simulator.

### *Affected Configurations*

This issue affects all configurations.

### *Design Impact*

The design does not simulate.

### *Workaround*

There is no workaround for VHDL simulations. For Verilog HDL simulations. Change line 154 in the **qdrii\_model.v** file to:

```
begin : f1
```

Also, change line 417 to:

```
begin : f2
```

### *Solution Status*

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

## **TimeQuest Timing Analyzer Failure**

When you use the Quartus II TimeQuest timing analyzer, it reports a recovery issue, because the reset is not in the same clock domain as the system clock.

### *Affected Configurations*

This issue affects all configurations.

### *Design Impact*

There is no design impact.

### *Workaround*

Change the reset sequence for the signals clocked on the CQ clock, before you run the TimeQuest analyzer.

### *Solution Status*

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

## **PLL Placement**

The IP Toolbench-generated example design uses a PLL phase shift of 90°, which can cause the design to miss hold timing analysis. The source synchronous PLL for the read capture should have a location constraint to place it on the same side of the device as the Q pins, otherwise, the source synchronous compensation does not compensate for the expected delays.

### *Affected Configurations*

This issue affects all configurations.

### *Design Impact*

The design misses hold timing analysis.

### *Workaround*

The PLL must be located on the same side of the device as the CQ/CQn groups, for the PLL to compensate properly.

### *Solution Status*

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

## **Constraints Errors With Companion Devices**

When you change the device in your project or add a HardCopy II companion device to a Stratix II project and you reopen the variation with IP Toolbench, the constraints editor sometimes does not show all

previously set byte groups in the floorplan. The constraints editor only shows the constraints applied to byte groups that are valid for the current device.

### *Affected Configurations*

This issue affects all configurations.

### *Design Impact*

The design fails.

### *Workaround*

Reassign the byte groups for the new device in the constraints editor.

### *Solution Status*

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

## **Supported Device Families**

The QDRII SRAM Controller MegaCore function only supports Stratix and Stratix II series, and HardCopy® II devices. However, if you choose an unsupported device for your Quartus II project and subsequently start the MegaWizard® Plug-In Manager, you can choose a different device family in the MegaWizard Plug-In Manager, which allows you to choose the QDRII SRAM Controller MegaCore function. There are no error messages when you perform this illegal operation.

### *Affected Configurations*

This issue affects all configurations.

### *Design Impact*

You cannot compile a design.

### *Workaround*

Ensure you choose a supported device family for the Quartus II project.

### *Solution Status*

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

### **No Description of Datapath Signals**

The *QDRII SRAM Controller MegaCore Function User Guide* does not describe the controller's internal signals that interface the datapath to the control logic and the resynchronization logic. For the signal descriptions, contact Altera mySupport.

### *Affected Configurations*

This issue affects all configurations.

### *Design Impact*

There is no design impact.

### *Workaround*

For the signal descriptions, contact Altera mySupport.

### *Solution Status*

This issue will be fixed in a future version of the *QDRII SRAM Controller MegaCore Function User Guide*.

### **Changing HDL**

Be aware that when you change the HDL (Verilog HDL to VHDL or VHDL to Verilog HDL) of your custom variation, IP Toolbench does not delete all the necessary files and during compilation the Quartus II software may try to access incorrect files, which results in errors.

### *Affected Configurations*

This issue affects all configurations.

### *Design Impact*

When you choose **Start Compilation**, there may be error messages and the design may not compile.

### *Workaround*

If you change which HDL you use, ensure you remove all unnecessary files from the Quartus II project.

### *Solution Status*

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

## **Compilation Error (Stratix II Series & HardCopy II Devices Only)**

The IP Toolbench constraints window allows the illegal situation where you can share DQ groups on the top and bottom banks for Stratix II series and HardCopy devices. When you compile your design the Quartus® II software issues a no fit error.

### *Affected Configurations*

This issue affects all DQS mode QDRII SRAM controllers on Stratix II series and HardCopy II devices.

### *Design Impact*

When you choose **Start Compilation**, there is an error message and the design does not compile.

### *Workaround*

If you are targeting Stratix II series or HardCopy II devices, in the Constraints window ensure you choose bytegroups on either the top or the bottom of the device, but not both.

### *Solution Status*

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

## **Gate-Level Simulation Filenames**

Various Quartus II software options may cause it to generate a netlist with a different filename than that expected by the gate-level simulation script. The simulation script expects *<project name>.vho* or *.vo* and *<project name>\_v* or *\_vhd.sdo* files to be present.

### *Affected Configurations*

This issue affects all configurations.

### *Design Impact*

You cannot run gate-level simulations.

### *Workaround*

For VHDL gate-level simulations, in the **simulation/modelsim** directory follow these steps:

1. Rename *<filename>.vho* file to *<project name>.vho*.
2. Rename *<filename>.sdo* file to *<project name>\_vhd.sdo*.

For Verilog HDL gate-level simulations, in the **simulation/modelsim** directory follow these steps:

1. Rename the *<filename>.vo* file to *<project name>.vo*.
2. Rename the *<filename>.sdo* file to *<project name>\_v.sdo*.
3. In the *<project name>.vo* file change the following line to point to the *<project name>\_v.sdo* file:

```
initial $sdf_annotate("<project name>_v.sdo");
```

### *Solution Status*

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

## **The ModelSim Script Does Not Support Companion Devices**

If you have a HardCopy II companion device in a Stratix II project, be aware that the ModelSim simulation scripts do not work if you change to your companion device.

### *Affected Configurations*

This issue affects designs with companion devices.

### *Design Impact*

The simulation script does not run.

### Workaround

Edit the Modelsim script to include the correct libraries.

### Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

## Contact Information

For more information, contact Altera's mySupport website at [www.altera.com/mysupport](http://www.altera.com/mysupport) and click **Create New Service Request**. Choose the **Product Related Request** form.

## Revision History

Table 2 shows the errata sheet revision history for the QDRII SRAM Controller MegaCore function v7.1.

<b>Table 2. QDRII SRAM Controller v 7.1 Errata Sheet Revision History</b>		
<b>Version</b>	<b>Date</b>	<b>Errata Summary</b>
1.1	June 2007	Added the Wide Mode is Nonoperational issue.
1.0	May 2007	First release.



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