



RapidIO MegaCore Function

This document addresses known errata and documentation issues for the Altera® RapidIO® MegaCore® function version 6.1. Errata are functional defects or errors, which may cause the RapidIO MegaCore function to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.



For the most up-to-date errata for this release, refer to the [RapidIO MegaCore Function v6.1 Errata Sheet](#) on the Altera website.

RapidIO MegaCore Function v6.1 Issues

Table 1 shows the issues that affect the RapidIO MegaCore function v6.1.

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Incorrect Clocking Between 1x RapidIO Physical Layers and Stratix II GX Transceiver

An incorrect clocking scheme was used between the 1x RapidIO MegaCore function's Physical Layers and the Stratix II GX Transceiver. This problem occasionally prevents the RapidIO link from being established or results in data corruption errors. This problem is the issue "Incorrect Clocking Between 4x RapidIO Physical Layers and Stratix II GX Transceiver", appearing in serial 1x RapidIO configurations.

Affected Configurations

All serial 1x RapidIO variations using the Stratix II GX PHY transceiver selection are affected.

Design Impact

The problem may occasionally prevent the RapidIO link from being established or results in data corruption errors on the link.

Workaround

Upgrade to RapidIO MegaCore function v7.1 or later.

Solution Status

This issue is fixed in RapidIO MegaCore function v7.1.

The Value Written to a Physical Layer Register Can Be Overwritten

A write transfer to registers in the Physical Layer is sometimes followed by an erroneous internal write transaction that overwrites the written value with an invalid value. This erroneous behavior has been observed only when a write transaction to a Physical Layer register is immediately followed by an access to one of the registers outside of the Physical Layer.

Affected Configurations

This issue affects all variations that implement some of the Logical Layer modules or the passthrough interface.

Design Impact

An incorrect value is sometimes written to Physical Layer registers.

Workaround

When writing to a register in the Physical Layer, read back the register after writing to make sure the correct value was written.

Solution Status

This issue will be fixed in a future release.

An Empty Demo Testbench Is Generated for Variations with an Atlantic Passthrough Port But No Logical Layer Module

The demo testbench that is generated for variations that include the Transport layer and an Atlantic™ passthrough port, but no other Logical Layer module, does not generate any packet traffic.

Affected Configurations

This issue affects all variations that have a Transport Layer and an Atlantic passthrough port, but have no Logical Layer module.

Design Impact

You cannot use the demonstration testbench to verify operation of the Atlantic passthrough port.

Workaround

Add a logical layer module or remove the Transport Layer and Atlantic Passthrough port.

Solution Status

This issue is fixed in release 7.1 of the RapidIO MegaCore function.

RapidIO MegaWizard Interface May Hang When Upgrading a Variant Created by a 3.x Version

The RapidIO MegaWizard interface may hang when you upgrade a variant created by a previous version of the Quartus® II software. When this happens the MegaWizard interface pauses indefinitely on the **Loading MegaWizard** splash screen.

Affected Configurations

This issue affects any RapidIO variation created by a version earlier than version 3.1.0. Upgrading the variant to 3.1.0 or 3.1.1 before loading version 6.1 or later does not fix the problem.

Design Impact

None.

Workaround

Restart the Quartus II software and create a new variation of the RapidIO MegaCore function v6.1 using the MegaWizard Plug-In Manager. You will have to reenter your parameters using the RapidIO MegaWizard interface.

Solution Status

This issue is fixed in release 7.0 of the RapidIO MegaCore function.

Incorrect Revision ID Label in RapidIO MegaWizard

The parameter to set the Assembly Register **Revision ID** is mislabeled as **Vendor ID**.

Affected Configurations

This issue affects any RapidIO variation.

Workaround

On the **Capabilities Register** page of the MegaWizard interface there are two parameters labeled **Vendor ID** under **Assembly Registers**.

The bottom parameter is incorrectly labeled **Vendor ID**: this parameter should be labeled **Revision ID**.

Solution Status

This issue is fixed in release 7.1 of the RapidIO MegaCore function.

Incorrect I/O Logical Layer Avalon-MM Slave Write Request Packets

The RapidIO Input/Output Logical Layer Avalon[®]-MM Slave can generate an incorrect write request packet if an invalid combination of burstcount, byteenable and address is applied to the datapath write Avalon-MM slave interface.

Affected Configurations

This issue affects all 32-bit variations that include the Input/Output Logical Layer module and may also affect 64-bit variations.

Design Impact

An incorrect write request packet can be sent.

Workaround

Avoid using invalid combinations of burstcount, byteenable, and address.

Solution Status

This issue is fixed in RapidIO MegaCore function v7.1.

RapidIO MegaWizard Interface Options for the Stratix II GX Transceiver Have No Effect

Editing the transceiver parameters in the RapidIO MegaCore MegaWizard interface has no effect on the generated transceiver.

Affected Configurations

This issue affects all Stratix II GX serial RapidIO variations.

Design Impact

Transceiver parameters cannot be adjusted through the RapidIO MegaWizard interface.

Workaround

Use the MegaWizard Plug-In Manager to edit the `*_riophy_gxb.v` MegaCore function directly.

Solution Status

This issue is fixed in release 7.1 of the rapidIO MegaCore function.

Incorrect Clocking Between 4x RapidIO Physical Layers and Stratix II GX Transceiver

An incorrect clocking scheme was used between the 4x RapidIO MegaCore function's Physical Layers and the Stratix II GX Transceiver. This problem occasionally prevents the RapidIO link from being established or results in data corruption errors.

Affected Configurations

All serial 4x RapidIO variations using the Stratix II GX PHY transceiver selection are affected.

Design Impact

The problem may occasionally prevent the RapidIO link from being established or results in data corruption errors on the link.

Workaround

Upgrade to RapidIO MegaCore function v7.1 or later.

Solution Status

This issue is fixed in RapidIO MegaCore function v7.1.

Read Request that Times Out on Maintenance Slave Port Hangs Avalon-MM Master

When a read request presented on the Maintenance Slave port times out, the signals `mnt_s_rd_readererror` and `mnt_s_readdatavalid` are not asserted. This leaves the Avalon-MM master that issued the read request hung waiting for the read data which is never returned.

Affected Configurations

All RapidIO variations that implement the Maintenance Slave port and have the possibility of read requests timing out in the RapidIO fabric are affected.

Design Impact

A maintenance read request that times out in the RapidIO fabric never completes at the Avalon-MM master that initiated the read.

Workaround

Upgrade to RapidIO MegaCore function v7.1 or later.

Solution Status

This issue is fixed in RapidIO MegaCore function v7.1.

When a readererror is Returned to an Avalon-MM Master Port a RapidIO Error Response is Not Generated

When the `readererror` signal is asserted in response to a read issued by one of the Avalon-MM master ports, a corresponding error response is not issued on the RapidIO link. The read operation instead times out at the initiating endpoint.

Affected Configurations

All RapidIO variations that implement the Maintenance master or I/O Read master ports that might have the `readererror` signal asserted are affected.

Design Impact

RapidIO read requests that encounter an Avalon `readererror` times out instead of terminating with an error response.

Workaround

Upgrade to RapidIO MegaCore function v7.1 or later.

Solution Status

This issue is fixed in RapidIO MegaCore function v7.1.

Reception of a Malformed Write Request Packet Causes the Next Request Packet to be Lost

If an `NWRITE` or `NWRITE_R` request packet without any payload (that is, shorter than 10 bytes), but with a valid CRC, is received by the IO Avalon-MM Master module, the next request packet received by the IO Avalon-MM Master is silently discarded.

Affected Configurations

This issue affects variations with a 64-bit wide internal data path that implements the IO Avalon-MM Master module.

Design Impact

In the unlikely event that such a malformed request packet is received, the following request packet is ignored. If that request required a response, the response is not sent and the request eventually times out. The far end entity determines how to deal with the timed out request. If the request did not require a response, it is silently ignored and normal operation continues.

Workaround

Avoid sending write request packets with no payload.

Solution Status

This issue will be fixed in a future release.

Error Response is Sent for an `SWRITE` Packet that Follows a Bad `NWRITE_R` Packet

When an `SWRITE` packet is received from the RapidIO link after a bad `NWRITE_R` is received, error responses are returned for both the `NWRITE_R` and the `SWRITE`. No response should be sent for the `SWRITE`. This causes the endpoint that initiated the `SWRITE` to declare an unexpected response error.

Affected Configurations

All RapidIO variations are affected.

Design Impact

Other endpoints may report unexpected response errors to `SWRITE` packets that happen to follow bad `NWRITE_R` packets.

Workaround

Ignore the unexpected response errors or upgrade to RapidIO MegaCore function v7.1 or later.

Solution Status

This issue is fixed in RapidIO MegaCore function v7.1.

RTL Generation Issue when Transport Layer Enabled with no Maintenance Port

Incorrect RTL is generated for configurations where the Transport Layer is enabled, and the Maintenance Port is set to `None`. This results in a non-functional core.

Affected Configurations

Configurations where the Transport Layer is enabled, and the Maintenance Port is set to `None`.

Design Impact

The port response time-out register becomes a single bit register instead of a 24-bit register. The reduced register size causes the Rapid IO core to constantly time-out.

Work Around

Open the `<variation_name>_rio.v` file, and add the following wire declaration immediately below the last input/output declarations:

```
wire [23:0] port_response_timeout;
```

To regenerate the IP Functional Simulation model, please file a my-support service request to receive instructions.

Solution Status

This issue is fixed in version 7.2.

Write Transactions Lost or Altered if `io_s_wr_write` and `io_s_wr_chipselect` are De-Asserted Inside a Write Burst Transaction

If the `io_s_wr_chipselect` or `io_s_wr_write` signal are de-asserted inside a burst write transfer, an invalid write request packet can be generated by the Input/Output Avalon-MM Slave module. In some cases this packet is cancelled by the physical layer, in other cases an incorrect write request packet is sent.

Affected configuration

All configurations which use the Input/Output Avalon-MM Slave module and burst write transfers.

Design Impact

Write transactions can be lost or replaced by incorrect write transactions.

Work Around

Make sure the `io_s_wr_chipselect` and `io_s_wr_write` signals remain asserted for the full duration of the write burst transfer.

Solution Status

This is fixed in version 7.2.

Connections to Non-Existing Ports are Attempted in Demo Testbench when Maintenance Logical Layer Module is Absent

The instantiations of the `rio DUT` and the `sister_rio` in the `hookup` file of the demo testbench have extra ports that do not exist in the `rio DUT` and `sister_rio` modules. This causes errors when simulating the demo testbench.

Affected configurations

All variations that have no Maintenance module but have an Input/Output Avalon-MM master module are affected.

Design Impact

None, only the demo testbench fails to compile or run.

Workaround

The <variation_name>_hookup.iv can be edited to remove the extra ports.

The lines to remove are:

```
// -----
// Error Management
// -----
,.io_m_err_unsupported_transaction      (io_m_err_unsupported_transaction) // output
,.io_m_err_illegal_transaction_decode  (io_m_err_illegal_transaction_decode) // output
,.io_m_err_source_id                   (io_m_err_source_id) // output [8-1:0]
,.io_m_err_destination_id              (io_m_err_destination_id) // output [8-1:0]
,.io_m_err_ttype                        (io_m_err_ttype) // output [3:0]
,.io_m_err_ftype                        (io_m_err_ftype) // output [3:0]
,.io_m_err_xamsbs                       (io_m_err_xamsbs) // output [1:0]
,.io_m_err_address                     (io_m_err_address) // output [28:0]

and

// -----
// Error Management
// -----
,.io_m_err_unsupported_transaction      (sister_io_m_err_unsupported_transaction) // output
,.io_m_err_illegal_transaction_decode  (sister_io_m_err_illegal_transaction_decode) // output
,.io_m_err_source_id                   (sister_io_m_err_source_id) // output [8-1:0]
,.io_m_err_destination_id              (sister_io_m_err_destination_id) // output [8-1:0]
,.io_m_err_ttype                        (sister_io_m_err_ttype) // output [3:0]
,.io_m_err_ftype                        (sister_io_m_err_ftype) // output [3:0]
,.io_m_err_xamsbs                       (sister_io_m_err_xamsbs) // output [1:0]
,.io_m_err_address                     (sister_io_m_err_address) // output [28:0]
```

Solution Status

This issue is fixed in version 7.2.

Contact Information

For more information, contact Altera's mySupport website at www.altera.com/mysupport and click **Create New Service Request**. Choose the **Product Related Request** form.

Revision History

Table 2 shows the revision history for the *RapidIO MegaCore Function v6.1 Errata Sheet*.

Version	Date	Errata Summary
1.3	December 2007	<p>Added the following erratum:</p> <ul style="list-style-type: none"> Incorrect Clocking Between 1x RapidIO Physical Layers and Stratix II GX Transceiver <p>Corrected Revision History entry for v1.2 of the document:</p> <ul style="list-style-type: none"> Added: Reception of a Malformed Write Request Packet Causes the Next Request Packet to be Lost Added: Incorrect I/O Logical Layer Avalon-MM Slave Write Request Packets Removed: When a readerror is Returned to an Avalon-MM Master Port an Error Response is Not Generated
1.2	September 2007	<p>Added the following errata:</p> <ul style="list-style-type: none"> Reception of a Malformed Write Request Packet Causes the next request Packet to be Lost Incorrect I/O Logical Layer Avalon-MM Slave Write Request Packets Incorrect Clocking Between 4x RapidIO Physical Layers and Stratix II GX Transceiver Incorrect Revision ID Label in RapidIO MegaWizard Read Request that Times Out on Maintenance Slave Port Hangs Avalon-MM Master When a readerror is Returned to an Avalon-MM Master Port a RapidIO Error Response is Not Generated Error Response for SWRITE Packet that Follows a Bad NWRITE_R Packet RTL Generation Issue when Transport Layer Enabled with no Maintenance Port Write Transactions Can Be Lost or Altered if <code>io_s_wr_write</code> and <code>io_s_wr_chipselect</code> are De-asserted Inside a Write Burst Transaction Connections to Non-Existing Ports are Attempted in Demo Testbench when Maintenance Logical Layer Module is Absent An Empty Demo Testbench Is Generated for Variations with an Atlantic Passthrough Port But No Logical Layer Module RapidIO MegaWizard Interface May Hang When Upgrading a Variant Created by a Previous Version
1.1	April 2007	<p>Added the following erratum:</p> <ul style="list-style-type: none"> RapidIO MegaWizard Interface Options for the Stratix II GX Transceiver Have No Effect
1.0	December 2006	<p>The following erratum exists:</p> <ul style="list-style-type: none"> The Value Written to a Physical Layer Register Can Be Overwritten



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