



# RapidIO MegaCore Function

October 2007, MegaCore Function Version 7.0

Errata Sheet

This document addresses known errata and documentation issues for the Altera® RapidIO MegaCore® function version 7.0. Errata are functional defects or errors, which may cause the RapidIO MegaCore function to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.



For the most up-to-date errata for this release, refer to the [RapidIO MegaCore Function v7.0 Errata Sheet](#) on the Altera website.

## RapidIO MegaCore Function Version 7.0 Issues

Table 1 shows the issues that affect the RapidIO MegaCore Function v7.0.

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### **Exchange of Packets Stops if Link Partner Sends a Restart-From-Error in Response to a Packet-Retry**

If a link partner sends a `link-request input-status` control symbol (also known as `restart-from-error` control symbol) in response to a `packet-retry` control symbol sent by the RapidIO MegaCore function, the MegaCore function responds with a `link-response OK` control symbol, but the input port remains in the `retry-stopped` mode until a `restart-from-retry` control symbol is received.

#### *Affected Configurations*

All serial RapidIO variations.

#### *Design Impact*

Processing of incoming traffic stops until the MegaCore function receives a `restart-from-retry` control symbol, detects an input error, or is reset.

#### *Workaround*

Perform one of the following workarounds:

- Make sure the link partner sends a `restart-from-retry` in response to a `packet-retry`.

Or:

- Monitor the state of the input control state machine with software and have the link partner cause a detectable error or reset the MegaCore function when the input state machine remains in the `retry-stopped` for excessive amounts of time.

### *Solution Status*

This issue will be fixed in a future release of the RapidIO MegaCore function. Until then you can use the workaround or contact Altera for a patch if you encounter this problem.

## **Input-Output Avalon-MM Master Module Stops Accepting Write Request Packets if it Receives Too Many Malformed Packets**

When the Input-Output Avalon-MM master module receives a malformed packet that has an invalid payload size (larger than 8-bytes but not a multiple of 8-bytes) but with valid CRC(s), it executes the burst write transfer, using undefined values to fill in for the missing payload on the last word of the Avalon-MM burst write transfer. Furthermore, the Input-Output Avalon-MM master module fails to de-allocate some internal resources. If this occurs several times, the Input-Output Avalon-MM master module eventually expends all aforementioned resources and is unable to accept any further write request packets, causing traffic to back up in the transport and physical layer, and causing the received packets to be retried indefinitely.

### *Affected Configurations*

All RapidIO variations using the Avalon-MM write master interface of the Input-Output Avalon-MM master module.

### *Design Impact*

The MegaCore function stops accepting all incoming packets.

### *Workaround*

Avoid sending malformed packets of the type described above.

### *Solution Status*

This issue will be fixed in a future release of the RapidIO MegaCore function.

## Illegal IO Slave Write Transaction Prevents RapidIO Core from Sending Doorbell Packet

An IO Slave Write Transaction with the `byteenable` bus set to all zeros causes the RapidIO core to miss sending a Doorbell Packet.

### *Affected Configurations*

This issue affects all variants that have the IO Slave and Doorbell modules enabled. Both 1x and 4x at all data rates are affected.

### *Design Impact*

The Doorbell Packet is never received by the intended target. Any processing by the remote processing endpoint dependent on the doorbell message is affected.

### *Workaround*

Avoid a zero value on the `io_s_wr_byteenable` bus when issuing write transactions across the IO Slave Write port.

### *Solution Status*

This issue will be fixed in a future release of the RapidIO MegaCore function.

## Packets from Other Logical Layer Modules May Not be Transmitted After a Write Burst is Paused

After the `io_s_wr_write` or `io_s_wr_chipselect` signals are deasserted inside an Avalon-MM burst write transfer near the end of the burst, the packet transmission scheduler in the Transport layer may fail to select packets from other Logical layers for transmission.

### *Affected Configurations*

All RapidIO variations that include a Input/Output Avalon-MM slave module and at least one other Logical layer module or the pass-through interface.

### *Design Impact*

Packets from Logical layer modules other than the Input/Output Avalon-MM slave or from the pass-through interface might not get transmitted.

### *Workaround*

Avoid de-asserting the `io_s_wr_write` or `io_s_wr_chipselect` signals inside a burst transfer.

### *Solution Status*

This issue is fixed in RapidIO MegaCore function v7.2.

## **Internal Clock Frequency Information Message Is Incorrect for Parallel Variations**

The RapidIO MegaWizard GUI may display incorrect information messages about the internal clock frequency when in parallel mode (these messages are in the **Info:** area at the bottom of the GUI screen).

### *Affected Configurations*

This issue affects any parallel RapidIO variation.

### *Design Impact*

None.

### *Workaround*

The internal clock frequency is set automatically, based on the internal data path width, as follows:  
For 32-bit internal data path variations the internal clock frequency is the baud rate divided by 4.  
For 64-bit internal data path variations the internal clock frequency is the baud rate divided by 8.

### *Solution Status*

This issue is fixed in version 7.1.

## **MegaWizard GUI Permits Generation of Illegal and Invalid Parallel Variations**

The MegaWizard GUI will generate MegaCore files even if the data rate selected for the variation is outside the allowed range. The resulting variation will be invalid and may fail to compile or simulate properly.

*Affected Configurations*

Affects invalid parallel RapidIO variations only.

*Design Impact*

None.

*Workaround*

Do not attempt to generate a variation with a data rate outside the valid range.

*Solution Status*

This issue is fixed in version 7.1.

**The Value Written to a Physical Layer Register Can Be Overwritten**

A write transfer to registers in the Physical Layer is sometimes followed by an erroneous internal write transaction that overwrites the written value with an invalid value. This erroneous behavior has been observed only when a write transaction to a Physical Layer register is immediately followed by an access to one of the registers outside of the Physical Layer.

*Affected Configurations*

This issue affects all variations that implement some of the logical layer modules or the passthrough interface.

*Design Impact*

An incorrect value is sometimes written to physical layer registers.

*Workaround*

When writing to a register in the physical layer, read back the register after writing to make sure the correct value was written.

*Solution Status*

This issue will be fixed in a future release.

## **An Empty Demo Testbench Is Generated for Variations with an Atlantic Passthrough Port But No Logical Layer Module**

The demo testbench that is generated for variations that include the Transport layer and an Atlantic™ passthrough port, but no other Logical Layer module, does not generate any packet traffic.

### *Affected Configurations*

This issue affects all variations that have a Transport Layer and an Atlantic passthrough port, but have no Logical Layer module.

### *Design Impact*

You cannot use the demonstration testbench to verify operation of the Atlantic passthrough port.

### *Workaround*

Add a logical layer module or remove the Transport Layer and Atlantic Passthrough port.

### *Solution Status*

This issue is fixed in release 7.1 of the RapidIO MegaCore function.

## **Incorrect I/O Logical Layer Avalon-MM Slave Write Request Packets**

The RapidIO Input/Output Logical Layer Avalon®-MM Slave can generate an incorrect write request packet if an invalid combination of burstcount, byteenable and address is applied to the datapath write Avalon-MM slave interface.

### *Affected Configurations*

This issue affects all 32-bit variations that include the Input/Output Logical Layer module and may also affect 64-bit variations.

### *Design Impact*

An incorrect write request packet can be sent.

### *Workaround*

Avoid using invalid combinations of burstcount, byteenable, and address.

### *Solution Status*

This issue is fixed in RapidIO MegaCore function v7.1.

## **RapidIO MegaWizard Interface Options for the Stratix II GX Transceiver Have No Effect**

Editing the transceiver parameters in the RapidIO MegaCore MegaWizard® interface has no effect on the generated transceiver.

### *Affected Configurations*

This issue affects all Stratix II GX serial RapidIO variations.

### *Design Impact*

Transceiver parameters cannot be adjusted through the RapidIO MegaWizard interface.

### *Workaround*

Use the MegaWizard Plug-In Manager to edit the \*\_riophy\_gxb.v MegaCore function directly.

### *Solution Status*

This issue is fixed in release 7.1 of the rapidIO MegaCore function.

## **Incorrect Clocking Between 4x RapidIO Physical Layers and Stratix II GX Transceiver**

An incorrect clocking scheme was used between the 4x RapidIO MegaCore function's Physical Layers and the Stratix II GX Transceiver. This problem occasionally prevents the RapidIO link from being established or results in data corruption errors.

### *Affected Configurations*

All serial 4x RapidIO variations using the Stratix II GX PHY transceiver selection are affected.

### *Design Impact*

The problem may occasionally prevent the RapidIO link from being established or results in data corruption errors on the link.

### *Workaround*

Upgrade to RapidIO MegaCore function v7.1 or later.

### *Solution Status*

This issue is fixed in RapidIO MegaCore function v7.1.

## **Read Request that Times Out on Maintenance Slave Port Hangs Avalon-MM Master**

When a read request presented on the Maintenance Slave port times out, the signals `mnt_s_rd_readererror` and `mnt_s_readdatavalid` are not asserted. This leaves the Avalon-MM master that issued the read request hung waiting for the read data which is never returned.

### *Affected Configurations*

All RapidIO variations that implement the Maintenance Slave port and have the possibility of read requests timing out in the RapidIO fabric are affected.

### *Design Impact*

A maintenance read request that times out in the RapidIO fabric never completes at the Avalon-MM master that initiated the read.

### *Workaround*

Upgrade to RapidIO MegaCore function v7.1 or later.

### *Solution Status*

This issue is fixed in RapidIO MegaCore function v7.1.

## **When a readerror is Returned to an Avalon-MM Master Port a RapidIO Error Response is Not Generated**

When the `readerror` signal is asserted in response to a read issued by one of the Avalon-MM master ports, a corresponding error response is not issued on the RapidIO link. The read operation instead times out at the initiating endpoint.

### *Affected Configurations*

All RapidIO variations that implement the Maintenance master or I/O Read master ports that might have the `readerror` signal asserted are affected.

### *Design Impact*

RapidIO read requests that encounter an Avalon `readerror` times out instead of terminating with an error response.

### *Workaround*

Upgrade to RapidIO MegaCore function v7.1 or later.

### *Solution Status*

This issue is fixed in RapidIO MegaCore function v7.1.

## **Reception of a Malformed Write Request Packet Causes the Next Request Packet to be Lost**

If an `NWRITE` or `NWRITE_R` request packet without any payload (that is, shorter than 10 bytes), but with a valid CRC, is received by the IO Avalon-MM Master module, the next request packet received by the IO Avalon-MM Master is silently discarded.

### *Affected Configurations*

This issue affects variations with a 64-bit wide internal data path that implements the IO Avalon-MM Master module.

### *Design Impact*

In the unlikely event that such a malformed request packet is received, the following request packet is ignored. If that request required a response, the response is not sent and the request eventually times out.

The far end entity determines how to deal with the timed out request. If the request did not require a response, it is silently ignored and normal operation continues.

#### *Workaround*

Avoid sending write request packets with no payload.

#### *Solution Status*

This issue will be fixed in a future release.

### **Error Response is Sent for an SWRITE Packet that Follows a Bad NWRITE\_R Packet**

When an SWRITE packet is received from the RapidIO link after a bad NWRITE\_R is received, error responses are returned for both the NWRITE\_R and the SWRITE. No response should be sent for the SWRITE. This causes the endpoint that initiated the SWRITE to declare an unexpected response error.

#### *Affected Configurations*

All RapidIO variations are affected.

#### *Design Impact*

Other endpoints may report unexpected response errors to SWRITE packets that happen to follow bad NWRITE\_R packets.

#### *Workaround*

Ignore the unexpected response errors or upgrade to RapidIO MegaCore function v7.1 or later.

#### *Solution Status*

This issue is fixed in RapidIO MegaCore function v7.1.

### **RTL Generation Issue when Transport Layer Enabled with no Maintenance Port**

Incorrect RTL is generated for configurations where the Transport Layer is enabled, and the Maintenance Port is set to None. This results in a non-functional core.

### *Affected Configurations*

Configurations where the Transport Layer is enabled, and the Maintenance Port is set to None.

### *Design Impact*

The port response time-out register becomes a single bit register instead of a 24-bit register. The reduced register size causes the Rapid IO core to constantly time-out.

### *Work Around*

Open the `<variation_name>_rio.v` file, and add the following wire declaration immediately below the last input/output declarations:

```
wire [23:0] port_response_timeout;
```

To regenerate the IP Functional Simulation model, please file a my-support service request to receive instructions.

### *Solution Status*

This issue will be fixed in a future release of the core.

## **Write Transactions Lost or Altered if io\_s\_wr\_write and io\_s\_wr\_chipselect are De-Asserted Inside a Write Burst Transaction**

If the `io_s_wr_chipselect` or `io_s_wr_write` signal are de-asserted inside a burst write transfer, an invalid write request packet can be generated by the Input/Output Avalon-MM Slave module. In some cases this packet is cancelled by the physical layer, in other cases an incorrect write request packet is sent.

### *Affected configuration*

All configurations which use the Input/Output Avalon-MM Slave module and burst write transfers.

### *Design Impact*

Write transactions can be lost or replaced by incorrect write transactions.

### Work Around

Make sure the `io_s_wr_chipselect` and `io_s_wr_write` signals remain asserted for the full duration of the write burst transfer.

### Solution Status

This issue is fixed in version 7.2.

## Connections to Non-Existing Ports are Attempted in Demo Testbench when Maintenance Logical Layer Module is Absent

The instantiations of the `rio` DUT and the `sister_rio` in the demo testbench hookup file have extra ports that do not exist in the `rio` DUT and `sister_rio` modules. This causes errors when simulating the demo testbench.

### Affected configurations

All variations that have no Maintenance module but have an Input/Output Avalon-MM master module are affected.

### Design Impact

None, only the demo testbench fails to compile or run.

### Workaround

Edit `<variation_name>_hookup.iv` to remove the following lines:

```
// -----
// Error Management
// -----
,.io_m_err_unsupported_transaction (io_m_err_unsupported_transaction) // output
,.io_m_err_illegal_transaction_decode (io_m_err_illegal_transaction_decode) // output
,.io_m_err_source_id (io_m_err_source_id) // output [8-1:0]
,.io_m_err_destination_id (io_m_err_destination_id) // output [8-1:0]
,.io_m_err_ttype (io_m_err_ttype) // output [3:0]
,.io_m_err_ftype (io_m_err_ftype) // output [3:0]
,.io_m_err_xamsbs (io_m_err_xamsbs) // output [1:0]
,.io_m_err_address (io_m_err_address) // output [28:0]

and

// -----
// Error Management
// -----
,.io_m_err_unsupported_transaction (sister_io_m_err_unsupported_transaction) // output
,.io_m_err_illegal_transaction_decode (sister_io_m_err_illegal_transaction_decode) // output
,.io_m_err_source_id (sister_io_m_err_source_id) // output [8-1:0]
,.io_m_err_destination_id (sister_io_m_err_destination_id) // output [8-1:0]
,.io_m_err_ttype (sister_io_m_err_ttype) // output [3:0]
,.io_m_err_ftype (sister_io_m_err_ftype) // output [3:0]
,.io_m_err_xamsbs (sister_io_m_err_xamsbs) // output [1:0]
,.io_m_err_address (sister_io_m_err_address) // output [28:0]
```

*Solution Status*

This issue is fixed in version 7.2.

**Contact  
Information**

For more information, contact Altera's mySupport website at [www.altera.com/mysupport](http://www.altera.com/mysupport) and click **Create New Service Request**. Choose the **Product Related Request** form.

## Revision History

Table 2 shows the revision history for the *RapidIO MegaCore Function v7.0 Errata Sheet*.

**Table 2. RapidIO MegaCore Function v7.0 Errata Sheet Revision History**

Version	Date	Errata Summary
1.1	September 2007	<p>The following errata were added:</p> <ul style="list-style-type: none"> <li>● Exchange of Packets Stops if Link Partner Sends a Restart-From-Error in Response to a Packet-Retry</li> <li>● Input-Output Avalon-MM Master Module Stops Accepting Write Request Packets if it Receives Too Many Malformed Packets</li> <li>● Illegal IO Slave Write Transaction Prevents RapidIO Core from Sending Doorbell Packet</li> <li>● Packets from Other Logical Layer Modules May Not be Transmitted After a Write Burst is Paused</li> <li>● Incorrect Clocking Between 4x RapidIO Physical Layers and Stratix II GX Transceiver</li> <li>● Read Request that Times Out on Maintenance Slave Port Hangs Avalon-MM Master</li> <li>● When a readerror is Returned to an Avalon-MM Master Port a RapidIO Error Response is Not Generated</li> <li>● Reception of a Malformed Write Request Packet Causes the Next Request Packet to be Lost</li> <li>● Error Response is Sent for an SWRITE Packet that Follows a Bad NWRITE_R Packet</li> <li>● RTL Generation Issue when Transport Layer Enabled with no Maintenance Port</li> <li>● Write Transactions Lost or Altered if io_s_wr_write and io_s_wr_chipselect are De-Asserted Inside a Write Burst Transaction</li> <li>● Connections to Non-Existing Ports are Attempted in Demo Testbench when Maintenance Logical Layer Module is Absent</li> <li>● Internal Clock Frequency Information Message Is Incorrect for Parallel Variations</li> <li>● MegaWizard GUI Permits Generation of Illegal and Invalid Parallel Variations</li> <li>● RapidIO MegaWizard Interface Options for the Stratix II GX Transceiver Have No Effect</li> </ul>
1.0	December 2006	<p>The following issues exists:</p> <ul style="list-style-type: none"> <li>● An Empty Demo Testbench Is Generated for Variations with an Atlantic Passthrough Port But No Logical Layer Module</li> <li>● The Value Written to a Physical Layer Register Can Be Overwritten</li> <li>● Incorrect I/O Logical Layer Avalon-MM Slave Write Request Packets</li> </ul>



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