



RapidIO MegaCore Function

September 2007, MegaCore Function Version 7.1

Errata Sheet

This document addresses known errata and documentation issues for the Altera® RapidIO® MegaCore® function version 7.1. Errata are functional defects or errors, which may cause the RapidIO MegaCore function to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.



For the most up-to-date errata for this release, refer to the [RapidIO MegaCore Function v7.1 Errata Sheet](#) on the Altera website.

RapidIO MegaCore Function Version 7.1 Issues

Table 1 shows the issues that affect the RapidIO MegaCore Function 7.1.

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Illegal IO Slave Write Transaction Prevents RapidIO Core from Sending Doorbell Packet

An IO Slave Write Transaction with the `byteenable` bus set to all zeros causes the RapidIO core to miss sending a Doorbell Packet.

Affected Configurations

This issue affects all variants that have the IO Slave and Doorbell modules enabled. Both 1x and 4x at all data rates are affected.

Design Impact

The Doorbell Packet is never received by the intended target. Any processing by the remote processing endpoint dependent on the doorbell message is affected.

Workaround

Avoid a zero value on the `io_s_wr_byteenable` bus when issuing write transactions across the IO Slave Write port.

Solution Status

This issue will be fixed in a future release of the RapidIO MegaCore function.

Packets from Other Logical Layer Modules May Not be Transmitted After a Write Burst is Paused

After the `io_s_wr_write` or `io_s_wr_chipselect` signals are de-asserted inside an Avalon-MM burst write transfer near the end of the burst, the packet transmission scheduler in the Transport layer may fail to select packets from other Logical layers for transmission.

Affected Configurations

All RapidIO variations that include a Input/Output Avalon-MM slave module and at least one other Logical layer module or the pass-through interface.

Design Impact

Packets from Logical layer modules other than the Input/Output Avalon-MM slave or from the pass-through interface might not get transmitted.

Workaround

Avoid de-asserting the `io_s_wr_write` or `io_s_wr_chipselect` signals inside a burst transfer.

Solution Status

This issue is fixed in RapidIO MegaCore function v7.2.

Exchange of Packets Stops if Link Partner Sends a Restart-From-Error in Response to a Packet-Retry

If a link partner sends a `link-request input-status` control symbol (also known as `restart-from-error` control symbol) in response to a `packet-retry` control symbol sent by the RapidIO MegaCore function, the MegaCore function responds with a `link-response OK` control symbol, but the input port remains in the retry-stopped mode until a `restart-from-retry` control symbol is received.

Affected Configurations

All serial RapidIO variations.

Design Impact

Processing of incoming traffic stops until the MegaCore function receives a `restart-from-retry` control symbol, detects an input error, or is reset.

Workaround

Perform one of the following workarounds:

- Make sure the link partner sends a `restart-from-retry` in response to a `packet-retry`.

Or:

- Monitor the state of the input control state machine with software and have the link partner cause a detectable error or reset the MegaCore function when the input state machine remains in the retry-stopped for excessive amounts of time.

Solution Status

This issue will be fixed in a future release of the RapidIO MegaCore function. Until then you can use the workaround or contact Altera for a patch if you encounter this problem.

Input-Output Avalon-MM Master Module Stops Accepting Write Request Packets if it Receives Too Many Malformed Packets

When the Input-Output Avalon-MM master module receives a malformed packet that has an invalid payload size (larger than 8-bytes but not a multiple of 8-bytes) but with valid CRC(s), it executes the burst write transfer, using undefined values to fill in for the missing payload on the last word of the Avalon-MM burst write transfer. Furthermore, the Input-Output Avalon-MM master module fails to de-allocate some internal resources. If this occurs several times, the Input-Output Avalon-MM master module eventually expends all aforementioned resources and is unable to accept any further write request packets, causing traffic to back up in the transport and physical layer, and causing the received packets to be retried indefinitely.

Affected Configurations

All RapidIO variations using the Avalon-MM write master interface of the Input-Output Avalon-MM master module.

Design Impact

The MegaCore function stops accepting all incoming packets.

Workaround

Avoid sending malformed packets of the type described above.

Solution Status

This issue will be fixed in a future release of the RapidIO MegaCore function.

Canceling the Edit of a RapidIO Component in SOPC Builder May Change the Component

When editing a RapidIO component within an SOPC Builder system, clicking **Cancel** may change the RapidIO component. Specifically Avalon-MM ports may be added or deleted.

Affected Configurations

This may affect any RapidIO component used in an SOPC Builder system.

Design Impact

None.

Workaround

Avoid canceling the edit of a RapidIO component within SOPC Builder.

Solution Status

This issue is fixed in RapidIO MegaCore function v7.2.

Cannot Add Multiple RapidIO Instances in SOPC Builder Systems

If you add more than one instance of the RapidIO MegaCore function to an SOPC Builder system, incorrect SOPC Builder system HDL is generated. This causes errors when compiling the SOPC Builder system in the Quartus II or simulator software.

Affected Configurations

This issue affects any SOPC Builder system that requires more than one instance of the RapidIO MegaCore function.

Design Impact

You cannot directly use the SOPC Builder design flow to create a system that requires more than one instance of the RapidIO MegaCore function.

Workaround

You can use an alternative design flow as a workaround this issue. You can create the RapidIO MegaCore function variations you need using the MegaWizard Plug-In Manager design flow. You can then manually

import the RapidIO MegaCore function variations into SOPC Builder using the component editor, which is available from the **New Component** command on the SOPC Builder file menu.

Solution Status

This issue is fixed in version 7.2.

Unable to Edit the alt2gxb Instance Created by the RapidIO MegaCore Function

If you try to edit the alt2gxb instance generated by the RapidIO MegaCore v7.1 with the MegaWizard Plug-In Manager the following error is reported:

```
Cannot implement the requested GXB. Please check  
WIZ_SUBPROTOCOL.
```

Affected Configurations

All RapidIO variations using the Stratix II GX PHY transceiver selection for which you want to modify the alt2gxb instance are affected.

Design Impact

None.

Workaround

Before trying to edit the alt2gxb variation with the MegaWizard Plug-In Manager, edit the variation file and change this line:

```
// Retrieval info: PRIVATE: WIZ_SUBPROTOCOL STRING "No Loopback"
```

To:

```
// Retrieval info: PRIVATE: WIZ_SUBPROTOCOL STRING "None"
```

Solution Status

This issue is fixed in version 7.2.

The Value Written to a Physical Layer Register Can Be Overwritten

A write transfer to registers in the Physical Layer is sometimes followed by an erroneous internal write transaction that overwrites the written value with an invalid value. This erroneous behavior has been observed only when a write transaction to a Physical Layer register is immediately followed by an access to one of the registers outside of the Physical Layer.

Affected Configurations

This issue affects all variations that implement some of the Logical Layer modules or the passthrough interface.

Design Impact

An incorrect value is sometimes written to Physical Layer registers.

Workaround

When writing to a register in the Physical Layer, read back the register after writing to make sure the correct value was written.

Solution Status

This issue will be fixed in a future release.

Reception of a Malformed Write Request Packet Causes the Next Request Packet to be Lost

If an `NWRITE` or `NWRITE_R` request packet without any payload (that is, shorter than 10 bytes), but with a valid CRC, is received by the IO Avalon-MM Master module, the next request packet received by the IO Avalon-MM Master is silently discarded.

Affected Configurations

This issue affects variations with a 64-bit wide internal data path that implements the IO Avalon-MM Master module.

Design Impact

In the unlikely event that such a malformed request packet is received, the following request packet is ignored. If that request required a response, the response is not sent and the request eventually times out.

The far end entity determines how to deal with the timed out request. If the request did not require a response, it is silently ignored and normal operation continues.

Workaround

Avoid sending write request packets with no payload.

Solution Status

This issue will be fixed in a future release.

RTL Generation Issue when Transport Layer Enabled with no Maintenance Port

Incorrect RTL is generated for configurations where the Transport Layer is enabled, and the Maintenance Port is set to `None`. This results in a non-functional core.

Affected Configurations

Configurations where the Transport Layer is enabled, and the Maintenance Port is set to `None`.

Design Impact

The port response time-out register becomes a single bit register instead of a 24-bit register. The reduced register size causes the Rapid IO core to constantly time-out.

Work Around

Open the `<variation_name>_rio.v` file, and add the following wire declaration immediately below the last input/output declarations:

```
wire [23:0] port_response_timeout;
```

To regenerate the IP Functional Simulation model, please file a my-support service request to receive instructions.

Solution Status

This issue will be fixed in a future release of the core.

Write Transactions Lost or Altered if `io_s_wr_write` and `io_s_wr_chipselect` are De-Asserted Inside a Write Burst Transaction

If the `io_s_wr_chipselect` or `io_s_wr_write` signal are de-asserted inside a burst write transfer, an invalid write request packet can be generated by the Input/Output Avalon-MM Slave module. In some cases this packet is cancelled by the physical layer, in other cases an incorrect write request packet is sent.

Affected configuration

All configurations which use the Input/Output Avalon-MM Slave module and burst write transfers.

Design Impact

Write transactions can be lost or replaced by incorrect write transactions.

Work Around

Make sure the `io_s_wr_chipselect` and `io_s_wr_write` signals remain asserted for the full duration of the write burst transfer.

Solution Status

This issue is fixed in version 7.2.

Connections to Non-Existing Ports are Attempted in Demo Testbench when Maintenance Logical Layer Module is Absent

The instantiations of the `rio DUT` and the `sister_rio` in the hookup file of the demo testbench have extra ports that do not exist in the `rio DUT` and `sister_rio` modules. This causes errors when simulating the demo testbench.

Affected configurations

All variations that have no Maintenance module but have an Input/Output Avalon-MM master module are affected.

Design Impact

None, only the demo testbench fails to compile or run.

Workaround

The `<variation_name>_hookup.iv` can be edited to remove the extra ports.

The lines to remove are:

```
// -----  
// Error Management  
// -----  
,.io_m_err_unsupported_transaction (io_m_err_unsupported_transaction) // output  
,.io_m_err_illegal_transaction_decode (io_m_err_illegal_transaction_decode) // output  
,.io_m_err_source_id (io_m_err_source_id) // output [8-1:0]  
,.io_m_err_destination_id (io_m_err_destination_id) // output [8-1:0]  
,.io_m_err_ttype (io_m_err_ttype) // output [3:0]  
,.io_m_err_ftype (io_m_err_ftype) // output [3:0]  
,.io_m_err_xamsbs (io_m_err_xamsbs) // output [1:0]  
,.io_m_err_address (io_m_err_address) // output [28:0]  
  
and  
  
// -----  
// Error Management  
// -----  
,.io_m_err_unsupported_transaction (sister_io_m_err_unsupported_transaction) // output  
,.io_m_err_illegal_transaction_decode (sister_io_m_err_illegal_transaction_decode) // output  
,.io_m_err_source_id (sister_io_m_err_source_id) // output [8-1:0]  
,.io_m_err_destination_id (sister_io_m_err_destination_id) // output [8-1:0]  
,.io_m_err_ttype (sister_io_m_err_ttype) // output [3:0]  
,.io_m_err_ftype (sister_io_m_err_ftype) // output [3:0]  
,.io_m_err_xamsbs (sister_io_m_err_xamsbs) // output [1:0]  
,.io_m_err_address (sister_io_m_err_address) // output [28:0]
```

Solution Status

This issue is fixed in version 7.2.

Address Information Not Captured in Error Management Registers When NREAD Request Times Out

Affected Configurations

This issue affects all variations that implement the Input/Output Avalon-MM slave logical layer module.

Design Impact

This issue results in some missing debug information when an NREAD request times out.

Workaround

There is no workaround for this issue.

Solution Status

This issue will be fixed in a future release.

Contact Information

For more information, contact Altera's mySupport website at www.altera.com/mysupport and click **Create New Service Request**. Choose the **Product Related Request** form.

Revision History

Table 2 shows the revision history for the *RapidIO MegaCore Function v7.1 Errata Sheet*.

Version	Date	Errata Summary
1.1	September 2007	<ul style="list-style-type: none"> ● Illegal IO Slave Write Transaction Prevents RapidIO Core from Sending Doorbell Packet ● Packets from Other Logical Layer Modules May Not be Transmitted After a Write Burst is Paused ● Exchange of Packets Stops if Link Partner Sends a Restart-From-Error in Response to a Packet-Retry ● Input-Output Avalon-MM Master Module Stops Accepting Write Request Packets if it Receives Too Many Malformed Packets ● Canceling the Edit of a RapidIO Component in SOPC Builder May Change the Component ● Cannot Add Multiple RapidIO Instances in SOPC Builder Systems ● Unable to Edit the alt2gxb Instance Created by the RapidIO MegaCore Function ● The Value Written to a Physical Layer Register Can Be Overwritten ● RTL Generation Issue when Transport Layer Enabled with no Maintenance Port ● Write Transactions Lost or Altered if io_s_wr_write and io_s_wr_chipselect are De-Asserted Inside a Write Burst Transaction ● Connections to Non-Existing Ports are Attempted in Demo Testbench when Maintenance Logical Layer Module is Absent
1.0	May 2007	<ul style="list-style-type: none"> ● Reception of a Malformed Write Request Packet Causes the Next Request Packet to be Lost ● Address Information Not Captured in Error Management Registers When NREAD Request Times Out



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