

This document addresses known errata and documentation issues for the SDI MegaCore® function version 7.1. Errata are functional defects or errors, which may cause the SDI MegaCore function to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

Table 1 shows the issues that affect the SDI MegaCore function v7.1.

<i>Table 1. SDI MegaCore Function v7.1 Issues</i>	
Issue	Page
NativeLink Fails with the ModelSim Simulator	1
Functional Simulation Netlist Error	2
Compilation Errors when Using Include PLLs Option	2
The rx_AP signal shows Incorrect Operation	3



For the most up-to-date errata for this release, refer to the errata sheet on the Altera® website:

[www.altera.com/literature/es/es\\_sdi\\_71.pdf](http://www.altera.com/literature/es/es_sdi_71.pdf)

## SDI MegaCore Function v7.1 Issues

This section describes the SDI MegaCore function v7.1 issues.

### NativeLink Fails with the ModelSim Simulator

When using NativeLink to run simulations using the ModelSim simulator, the testbench fails.

#### *Affected Configurations*

This issue affects all configurations.

#### *Design Impact*

The design does not simulate and the testbench reports a failure.

### *Workaround*

Use the Altera-provided ModelSim simulation scripts.

### *Solution Status*

This issue will be fixed in a future release of the SDI MegaCore function.

## **Functional Simulation Netlist Error**

The SDI MegaCore function compiles successfully, but when you try to generate a functional simulation netlist, you get the following error:

```
Error: Can't generate functional simulation netlist because cannot convert  
WYSIWYG primitive pll for a different device family
```

```
Error: Can't elaborate user hierarchy  
"sdi_megacore_top:sdi_megacore_top_inst|sdi_clocks:pll_gen.u_pll|stratix_  
c2_pll_sclk:u_rx_pll|altpll:altpll_component"
```

### *Affected Configurations*

This issue affects all Stratix® II designs using the **Use 27-MHz reference clock and include oversampler PLL** option.

### *Design Impact*

There is no design impact.

### *Workaround*

Parameterize the transmitter MegaCore function but turn off the **Use 27-MHz reference clock and include oversampler PLL** option.

### *Solution Status*

This issue will be fixed in a future release of the SDI MegaCore function.

## **Compilation Errors when Using Include PLLs Option**

When you turn on **Use 27-MHz reference clock and include oversampler PLL** for Cyclone® III or Stratix III devices, the design does not compile because of errors.

### *Affected Configurations*

This issue only affects designs on Cyclone III and Stratix III devices.

### *Design Impact*

The design will fail in compilation.

### *Workaround*

Parameterize the MegaCore function but turn off **Use 27-MHz reference clock and include oversampler PLL**. Generate the required clock signals from a PLL outside the MegaCore function.

### *Solution Status*

This issue will be fixed in a future release of the SDI MegaCore function.

## **The rx\_AP signal shows Incorrect Operation**

The rx\_AP signal is internally wired to the rx\_H signal, so does not indicate active picture content.

### *Affected Configurations*

This issue affects all configurations with the exception of HD-SDI dual link.

### *Design Impact*

There is no design impact.

### *Workaround*

You may generate the rx\_AP signal outside of the core by combining the rx\_H and rx\_V signal:

```
rx_AP = ~rx_H & ~rx_V
```

### *Solution Status*

This issue will be fixed in a future release of the SDI MegaCore function.

## **Contact Information**

For more information, contact Altera's mySupport website at [www.altera.com/mysupport](http://www.altera.com/mysupport) and click **Create New Service Request**. Choose the **Product Related Request** form.

## Revision History

Table 2 shows the revision history for the *SDI MegaCore Function v7.1 Errata Sheet*.

Version	Date	Errata Summary
1.0	May 2007	First release.



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