

This errata sheet provides updated information on known device issues affecting Stratix® III devices.

## Stratix III Device Issue

Table 1 shows the specific issues and which Stratix III devices are affected by each issue.

**Table 1.** Stratix III Family Issues (Part 1 of 3)

Issue	Affected Devices	Fixed Devices
<p><a href="#">“Error Detection CRC Feature, When Enabled, May Cause the MLAB RAM Blocks to Operate Incorrectly” on page 3</a></p> <p>Error Detection CRC feature, when enabled, may cause the MLAB RAM blocks to operate incorrectly.</p>	All Stratix III Devices	<ul style="list-style-type: none"> <li>■ EP3SL50 Revision G</li> <li>■ EP3SL70 Revision F</li> <li>■ EP3SL110 Revision I</li> <li>■ EP3SL150 Revision H</li> <li>■ EP3SL200 Revision G</li> <li>■ EP3SL340 Revision E</li> <li>■ EP3SE50 Revision D</li> <li>■ EP3SE80 Revision G</li> <li>■ EP3SE110 Revision F</li> <li>■ EP3SE260 Revision F</li> </ul>
<p><a href="#">“Remote System Upgrade Feature” on page 4</a></p> <p>Remote System Upgrade feature fails when loading an invalid application configuration image.</p>	All Stratix III Devices	—
<p><a href="#">“CRC Error Injection Feature” on page 4</a></p> <p>The CRC error injection feature may not operate correctly.</p>	All Stratix III Devices	—
<p>MLAB final timing models were updated post Quartus II Software version 8.1. Only a subset of designs using MLAB blocks are affected. See the information in the second paragraph of <a href="#">“Updated MLAB Final Timing Model (Affecting a Subset of MLAB Designs)” on page 5</a>.</p>	<ul style="list-style-type: none"> <li>■ EP3SL110</li> <li>■ EP3SL150</li> <li>■ EP3SL340</li> <li>■ EP3SE110</li> <li>■ EP3SE80</li> </ul>	—
<p><a href="#">“Updated LVDS Final Timing Model” on page 5</a></p> <p>LVDS final timing models were updated post Quartus II Software version 8.1.</p>	All Stratix III Devices	—
<p>Dynamic phase alignment (DPA) circuitry in Stratix III devices might get stuck at the initial configured phase or move to the optimum phase after a longer than expected period of time.</p>	All Stratix III Devices	—
<p>V<sub>CCPT</sub> Power-Up Issue. Device may fail to power-up successfully.</p>	All Stratix III Devices	—
<p>CRC_ERROR may toggle unexpectedly in user mode without detecting an actual SEU.</p>	All Stratix III Devices	—

**Table 1.** Stratix III Family Issues (Part 2 of 3)


Issue	Affected Devices	Fixed Devices
M9K and M144K RAM blocks can be put into a locked, inactive state when driven by a clock with a very narrow pulse (for example, a glitch).	All Stratix III Devices	—
Stratix III devices can fail JTAG configuration in certain positions of the JTAG chain, depending on the setup conditions.	<ul style="list-style-type: none"> <li>■ 3SL150 Revision B and earlier</li> <li>■ 3SE50/L70/E110/E260/L340 Revision A</li> </ul>	<ul style="list-style-type: none"> <li>■ 3SL150 Revision C</li> <li>■ 3SE50/L70/E110/E260/L340 Revision B</li> <li>■ EP3SL200</li> <li>■ EP3SL110</li> <li>■ EP3SL50</li> <li>■ EP3SE80</li> </ul>
Interface timing issues with the LVDS hard macro.	All Stratix III devices	All Stratix III devices
The dynamic phase alignment (DPA) lock signal ( <code>rx_dpa_locked</code> ) does not assert on some channels during link initialization.	All Stratix III devices	All Stratix III devices
The DPA circuit in the EP3SL150 ES devices fails to lock and data is corrupted at data rates of 150 Mbps to 385 Mbps and data rates above 622 Mbps.	EP3SL150 ES devices	EP3SL150 production devices
Analog-to-digital converter (ADC) for temperature sensing diode (TSD) no longer supported.	All Stratix III ES and production devices	—
TSD must have $V_{CCPT}$ powered on to operate.	<ul style="list-style-type: none"> <li>■ Revision A of EP3SE50, EP3SL70, EP3SE110, EP3SE260, EP3SL340</li> <li>■ Revisions A and B of EP3SL150 devices</li> </ul>	Future revisions of the affected Stratix III devices
Device may enter power-on reset (POR) during reconfiguration cycle. New information for <a href="#">“Device Reconfiguration Issue” on page 9</a> .	<ul style="list-style-type: none"> <li>■ Revision A of EP3SE50, EP3SL70, EP3SE110, EP3SE260, EP3SL340</li> <li>■ Revisions A and B of EP3SL150 devices</li> </ul>	Future revisions of the affected Stratix III devices
Write speed decrease for M144K blocks in certain modes.	<ul style="list-style-type: none"> <li>■ Revision A of EP3SE50, EP3SL70, EP3SE110, EP3SE260, EP3SL340</li> <li>■ Revisions A and B of EP3SL150 devices</li> </ul>	Future revisions of the affected Stratix III devices

**Table 1.** Stratix III Family Issues (Part 3 of 3)

Issue	Affected Devices	Fixed Devices
MLAB RAM block size changed from 64×10 or 32×20 (640 bits) to 16×20 (320 bits).	All Stratix III ES and production devices	—
The TSD is not backwards compatible with Stratix II devices.	EP3SL150 ES devices	EP3SL150 production devices
Extra I <sub>CCL</sub> current in user mode.	EP3SL150 ES devices	EP3SL150 production devices
DPA fails to lock in some cases.	EP3SL150 ES devices	EP3SL150 production devices

The die revision is identified by the fourth alphanumeric character (Z) from the left printed on the top side of the device. [Figure 1](#) shows a Stratix III device's top side date code.

**Figure 1.** Stratix III Device Top Side Date Code

A XβZ ## #####  


## Error Detection CRC Feature, When Enabled, May Cause the MLAB RAM Blocks to Operate Incorrectly

The Error Detection CRC feature is typically used to detect single event upsets (SEU). This feature, when enabled, may cause the MLAB RAM blocks to operate incorrectly in Stratix III devices. Only write operations in MLAB RAM blocks are affected.



The Error Detection CRC feature itself and CRC error flag operate correctly as expected. FPGA configuration bits are not affected by this issue.

No action is required if Error Detection CRC is not used. The MLAB RAM blocks will operate correctly.

If Error Detection CRC is enabled, disabling the Error Detection CRC will resolve the problem.

Using M9K/M144K RAM blocks or Logic Cells (LC) instead of MLAB RAM blocks will also resolve the problem.



For additional information on converting MLAB RAM blocks to other memory types, refer to [Are there known issues regarding the Stratix III Error Detection CRC feature that may result in incorrect MLAB operation?](#)

## Remote System Upgrade Feature

The Remote System Upgrade feature does not operate correctly when you initiate a reconfiguration cycle that goes from a factory configuration image to an invalid application configuration image. For example, the Stratix III device fails to revert back to the factory configuration image after a configuration error is detected while loading the invalid application configuration. The failure is indicated by a continuous toggling signal on the nSTATUS pin.

In normal operation, the Stratix III device should revert back to the factory configuration image after a configuration error is detected with the invalid configuration image.



An invalid application configuration image is classified as one of the following:

- partially programmed application image
- blank application image
- application image assigned with a wrong start address

The remote system upgrade feature works correctly with all other reconfiguration trigger conditions.

A workaround is being implemented in the ALTREMOTE\_UPDATE megafunction and will be available in the Quartus® II software version 9.1 and later. If you need to use remote system upgrade feature prior to the Quartus II software version 9.1 release, contact Altera Technical Support at [www.altera.com/support](http://www.altera.com/support).

## CRC Error Injection Feature

The CRC error injection feature on Stratix III devices may not operate correctly when running the EDERROR\_INJECT JTAG instruction at error detection clock frequencies of 50 MHz and lower. The CRC\_ERROR output status pin may remain low, incorrectly indicating no CRC errors.

If error detection clock frequency is set to 50 MHz, the chance of the EDERROR\_INJECT JTAG instruction to work is 50 percent. For frequencies lower than 50 MHz, the chances for EDERROR\_INJECT JTAG instruction to work decreases significantly. At 50 MHz, Altera recommends that you should repeat the issuance of EDERROR\_INJECT JTAG instruction to resolve the issue.

If you need to correctly inject error at a CRC error detection frequency lower than 50 MHz, contact Altera Technical Support at [www.altera.com/support](http://www.altera.com/support).

The CRC error detection feature operates correctly as expected, and is not affected by this issue.

## Updated MLAB Final Timing Model (Affecting a Subset of MLAB Designs)


The timing model for the memory logic array block (MLAB) has been updated after the Quartus II software version 8.1 release. Altera recommends you recompile in Quartus II software version 9.0 or later.

Affected devices using MLABs could see an MLAB hold time violation if the **Beneficial Skew Optimization** option is set to **ON** or if the MLAB uses any locally routed clocks. The steps below detail how to verify these conditions:

1. To determine if your design uses MLAB, look for MLAB in the `<project name>.fit.rpt` file or the Fitter RAM Summary of the Fitter Compilation Report in the GUI. The type will be MLAB.
2. To determine if the **Beneficial Skew Optimization** option is set to **ON**, look in the `<project name>.qsf` for the following setting:

```
set_global_assignment -name  
ENABLE_BENEFICIAL_SKEW_OPTIMIZATION ON
```

To check for any locally routed clocks, look in the `<project name>.fit.rpt` or the Controls Signals section of the Fitter Compilation Report in the GUI. Each locally routed clock will have **Global** set to **NO**.


 For more information about this solution, refer to [Have the MLAB device timing models changed since the release of the Quartus II software version 8.1?](#)

## Updated LVDS Final Timing Model

The timing models for LVDS/DPA receiver blocks were updated.

The EP3SL340 timing model was updated after the release of the Quartus II software version 8.1. Designs using the LVDS/DPA receiver that were compiled with the Quartus II software version 8.1 must install patch 0.45. After the patch has been installed, a static timing analysis should be rerun on the design. This will ensure that no timing violations have occurred due to the model update. If a timing violation occurs, a recompilation of the design is recommended.

The EP3SL50, EP3SL70, EP3SL110, EP3SL150, EP3SL200, EP3SE50, EP3SE80, EP3SE110, and EP3SE260 timing models were updated after the release of the Quartus II software version 9.1. Designs using the LVDS/DPA receiver that were compiled with the Quartus II software version 9.1 should install the applicable patch available on the link below. After the patch has been installed, a static timing analysis should be rerun on the design. This will ensure that no timing violations have occurred due to the model update. If a timing violation occurs a recompilation of the design is recommended.

 For a list of available patches, refer to [Have the Stratix III device timing models for the LVDS SERDES been updated since the release of the Quartus II software version 8.1?](#)

## Stratix III DPA Misalignment

Stratix III DPA circuitry occasionally becomes stuck at the initial configured phase or takes significantly longer than expected to select the optimum phase. A non-ideal phase may result in data bit errors, even after the DPA lock signal has gone high. Resetting the DPA circuit may not alleviate the problem; in fact, resetting it might trigger the problem. LVDS receivers configured in DPA mode are affected. LVDS receivers configured in Soft CDR mode with 0 PPM difference (synchronous interface) are also affected.



The `rx_dpa_locked` signal (prior to Quartus II software version 9.0) may assert before the DPA has locked to the optimum phase per the soft DPA-lock fix, resulting in errors.

For applications with flexibility in the choice of training patterns, Altera recommends you choose bit sequences with more data transitions and a non-cyclical pattern similar to a PRBS or K28.5 code sequence. For applications using a fixed, cyclical, or data transition sparse training pattern prior to Quartus II software version 9.0, contact Altera's mysupport at [www.mysupport.altera.com](http://www.mysupport.altera.com). For example, if you are using the SPI 4.2 protocol, which specifies a training pattern of 10 0s and 10 1s, contact Altera's mysupport at [www.mysupport.altera.com](http://www.mysupport.altera.com).

## V<sub>CCPT</sub> Power-Up Issue

A small percentage of Stratix III FPGA devices might fail to power-up successfully. The failure may occur because the FPGA device fails to exit power-on reset (POR), as indicated by the `nSTATUS` pin being stuck low. Configuration starts only after `nSTATUS` transitions from low to high.

For systems already operating in the field without power-up failure, Stratix III devices on those systems are not at risk.

For additional support, contact Altera at [www.mysupport.altera.com](http://www.mysupport.altera.com).

## CRC Error Detection Issue

When single event upset (SEU) detection is enabled using the CRC error detection feature, some Stratix III devices might toggle the `CRC_ERROR` pin unexpectedly in user mode without detecting an actual SEU. This is due to the CRC check bits (used to check CRAM frame content) getting overwritten during the device configuration. Functionally, the FPGA operates as expected since the CRAM content for the FPGA is not affected.

A software patch is available for the Quartus II software version 8.0 SP1 and the same changes are made in the Quartus II software version 8.1 and later versions to prevent CRC-check-bits from being overwritten during device configuration.

The change only affects the configuration bitstream generation in the Quartus II software. Configuration bitstream generation occurs when you add an SRAM object file (`.sof`) to the Quartus II programmer or execute file conversion. After installing the software patch or using the Quartus II software version 8.1, design recompilation is not required to generate a new `.sof` file. You can use the existing `.sof` file to configure

Stratix III devices. For other programming files (for example, programmer object file [.pof], JTAG indirect configuration file [.jic], raw binary file [.rbf], jam file [.jam], jam byte-code file [.jbc], serial vector format file [.svf], and so forth), regenerate the files using the existing .sof file through the Convert Programming File utility in the Quartus II software.

## M9K and M144K RAM Lockup Issue

Stratix III M9K and M144K RAM blocks may enter a locked state if driven by a clock with a pulse narrower than the Stratix III TriMatrix Memory Block minimum pulse width specifications. In this state a RAM block no longer responds to reads or writes and requires an FPGA reconfiguration to restore operation. A narrow clock pulse may occur from an unstable clock source or from muxing between two clock sources. Only Stratix III M9K and M144K RAM blocks are affected. Memory logic array blocks (MLAB) RAM are not affected.

The issue occurs in the Read Timer Trigger circuitry within the M9K and M144K RAM blocks. The locked state can occur if a glitch occurs on the RAM input clock, which inadvertently freezes the Read Timer Trigger circuitry, locking the RAM block in its last operation.

The workarounds are to add clock-enable logic, internal PLL, or internal clock-regeneration logic. You can add clock-enable logic (internal or external) to disable RAM block operation until the clock is stable. You can also gate the clock internally or externally. If FPGA resources permit, you can use an internal PLL or clock regeneration logic to ensure a stable clock source at the RAM block input.

The Read Timer circuitry makes RAM block operation independent of the input clock duty cycle, thus maximizing design performance. If you cannot provide a stable clock, a patch for the Quartus II software version 8.0 SP1 works around this problem by bypassing this circuitry. Performance is dependent on the clock's duty cycle in all M9K and M144K RAM blocks, thus preventing this locked, inactive state.

In the long term, Altera will add this feature to the Quartus II software version 8.1. Timing analysis and simulation will be updated to accurately reflect the actual clock duty cycle. Altera will update the *Stratix III Device Handbook* to include minimum pulse width specifications for clock low time and high time.

## JTAG Configuration

JTAG configuration for Stratix III devices, when using the Quartus II Programmer in versions 7.2 or earlier software, fails in JTAG chain positions:

“position – 1” Mod 8 = 6, (where “position” = 7th, 15th, 23rd, 31st, 39th, etc.),  
where the position starts with 1 and represents the device closest to the TDI pin.

Stratix III devices in the reported failing JTAG chain position can fail JTAG configuration when attempted on a failing TCK clock cycle. The window for failure is one TCK clock cycle wide. The issue affects all configuration flows using a JTAG chain connection setup, including Jam, JBC, and SVF configuration flows.

The software patch to Quartus II software version 7.2 SP3 addresses the use of the Quartus II Programmer to configure devices via JTAG with a download cable. It does not address the case where a JTAG programming file (Jam/JBC/SVF) is used. The Quartus II Programmer was updated to adjust the number of TCK padding clock cycles between devices in the `SHIFT_DR` state to avoid this problem. The other configuration flows, including Jam, JBC, and SVF, are not fixed with the patch.

Quartus II software version 8.0 and later have the same modifications as the software patch to Quartus II software version 7.2 SP3.

## Interface Timing Issues with LVDS Hard Macro

The Quartus II software version 7.2 and all 7.2 service packs had incorrect timing models for transfers from the LVDS receive register to the first register in the FPGA fabric for Stratix III devices. Due to this incorrect timing model, data is occasionally corrupted.

This issue is fixed in the Quartus II software version 8.0. Designs with LVDS interfaces need to be recompiled with the Quartus II software version 8.0 or later.

## DPA Lock Signal Does Not Assert on Some Channels

The DPA lock signal (`rx_dpa_locked`) does not assert during link initialization when the DPA circuitry dithers. DPA circuitry dithers only when it has to choose between two adjacent optimum phases. The frequency of occurrence of dithering in DPA circuitry is a probability event. The DPA lock signal not asserting on a given channel is a random event. The DPA phase selection circuitry functions properly and there will be no data corruption.

Soft-CDR mode is not affected since the DPA lock signal is not applicable in this mode.

### Workaround

The workaround for this issue is a soft fix implemented in the ALTLVDS megafunction of the Quartus II software version 8.0 and later. All designs with DPA mode enabled and the **External PLL** option disabled must be recompiled with the Quartus II software version 8.0 or later.



For designs with DPA mode enabled and the **External PLL** option enabled, refer to [DPA Circuitry and rx\\_dpa\\_locked Signal Behavior in Stratix III Devices](#).

## DPA Circuit Fails to Lock

The DPA circuit in EP3SL150 ES devices fails to lock and data is corrupted at data rates from 150 Mbps to 385 Mbps and data rates above 622 Mbps. This issue is caused by a timing violation in the DPA circuitry. DPA circuitry functions properly in the data range of 385 Mbps to 622 Mbps.

This issue is fixed in the Stratix III EP3SL150 production devices. The Stratix III production devices operate over the full range of supported data rate.

## ADC No Longer Supported


The ADC circuitry for the TSD is no longer supported. The TSD itself is not affected. In order to convert the output of the TSD into a temperature reading, use an external temperature sensor device, such as those offered by Maxim Integrated Products (MAX66xx series and MAX1617).

## TSD Must have $V_{CCPT}$ Powered On

Affected devices require  $V_{CCPT}$  to be powered for the TSD to operate. Future silicon revisions of the affected Stratix III devices will be fixed and will not require  $V_{CCPT}$  to be powered on for TSD operation.


## Device Reconfiguration Issue

Affected devices might enter POR after a reconfiguration cycle (during user mode) is initiated, thereby causing an additional delay from when the reconfiguration cycle is initiated to when the reconfiguration process actually begins. The amount of delay depends on the PORSEL setting you choose.

 For more information about PORSEL settings, refer to the *Hot Socketing and Power-On Reset in Stratix III Devices* chapter in the *Stratix III Device Handbook*.

All configuration modes are affected. Initial configuration attempts at power-up are not affected.

When the device is in user mode, a reconfiguration cycle is initiated by pulsing the nCONFIG pin low and transitions it to a logic high.

 For more information on reconfiguration cycles, refer to the *Configuring Stratix III Device* chapter in the *Stratix III Device Handbook*. This chapter also contains a specification called tCF2ST1. This indicates the time from an nCONFIG rising edge to an nSTATUS rising edge on a reconfiguration attempt. The specification for tCF2ST1 is maximum 100  $\mu$ s. Affected devices will exceed this specification.

For customers using JTAG mode, an initialization file (**.ini**) variable was added to the Quartus II software version 8.0 to introduce a delay right after the PROGRAM instruction is issued. The variable is PGME\_JTAG\_PGM\_POR\_DELAY, and takes a value in microseconds. To introduce the recommended worst-case 300 ms delay, add the line PGME\_JTAG\_PGM\_POR\_DELAY=300000 to the **quartus.ini** file. The Quartus II software first looks for a **quartus.ini** file in the **quartus\bin** installation directory and then the project directory.

Due to the device entering POR, the Remote Update feature is not supported. Additionally, any type of JTAG boundary scan operation that relies on data being captured and held at the device pins during reconfiguration will fail because the entering POR will clear those values.

Future silicon revisions of the affected Stratix III devices will be fixed. The fixed devices will not exhibit the POR issue and will provide full support for Remote Update and the JTAG boundary scan operations mentioned above.

## M144K Block Issue

The Stratix III M144K RAM block timing performance has decreased for memory blocks using fast write mode in  $\times 9$  and  $\times 18$  data widths. Fast write mode is used for M144K memories when the Read-During-Write option is set to “Don’t Care” or “New Data” in the RAM MegaWizard® Plug-In Manager. The timing model change does not affect memories using ECC mode or ROM mode or for which the Read-During-Write option is set to “Old Data” or “Old memory contents appear.”

To determine the implemented width of the memory block you are using, look in the Resource Section of the Quartus II software Fitter Report under the “RAM Summary” and “Implementation Port A/B Width” columns.

Recompile your design with the Quartus II software version 7.2 SP3 or later to apply the updated timing model for M144K RAM blocks.

Future silicon revisions of the affected Stratix III devices will be fixed.

## MLAB RAM Block Size Change

The Stratix III MLAB RAM size changed from  $64 \times 10$  or  $32 \times 20$  (640 bits) to  $16 \times 20$  (320 bits) and no longer has native byte enable signals. The MLAB in ROM mode is not affected and remains at  $64 \times 10$  or  $32 \times 20$  (640 bits).

If your design uses MLABs, you must recompile in the Quartus II software version 7.2 SP3 or later. The Quartus II software version 7.2 SP3 service pack includes the changes to the MLABs detailed above and has automatic fixes to ensure device functionality when targeting MLABs.

To determine whether your design uses MLABs, check the Quartus II Fitter Report. There are two reasons your design might contain MLABs:

The first reason is because of an explicit (hard) assignment to the MLAB type. This is done either through a third-party EDA synthesis tool or through the Quartus II RAM MegaWizard® Plug-In Manager when you set the block type to MLAB.

The second reason your design might contain MLABs is because of a determination that is made at the discretion of the Quartus II software synthesizer or fitter at the compile time. The Quartus II software version 7.2 SP3 or later automatically uses MLABs in the new configuration when appropriate, and promotes larger RAM blocks to M9K blocks where necessary.

## User Action

Recompile your design with the Quartus II software version 7.2 SP3 or later.

## EP3SL150 ES Device Information

This section describes silicon issues affecting the EP3SL150 ES devices and describes additional differences between the EP3SL150 ES and production silicon.

Although the configuration file sizes are the same, the configuration files for EP3SL150 ES devices and EP3SL150 production devices are not compatible. If a designer attempts to configure an EP3SL150 production device with an EP3SL150 ES configuration file, or vice versa, the nSTATUS pin is driven low and configuration fails. To make sure the Quartus II software generates the correct configuration file, designers must select the EP3SL150 ES ordering codes when compiling for EP3SL150 ES devices. Similarly, designers must select the EP3SL150 production ordering codes when compiling for EP3SL150 production devices.

### EP3SL150 ES Device Issues

Altera has identified silicon issues affecting the Stratix III EP3SL150 ES devices. These issues will be fixed in Stratix III EP3SL150 production devices. The issues are:

#### TSD Issue

The temperature sensing diode in EP3SL150 ES devices is not supported because it is not backwards compatible with Stratix II devices.

- In Stratix II devices, TEMPDIODEn is at 0.6 V and TEMPDIODEp is at 1.2 V.
- In Stratix III devices, TEMPDIODEn is at 0 V and TEMPDIODEp is at 0.6 V.

While the voltage difference is the same, some external temperature sensing devices have a bias diode from TEMPDIODEn to ground. When you connect the external temperature sensing device to the EP3SL150 ES device, the diode is shorted out and the external temperature sensing device will not be able to read the temperature correctly.

Stratix III EP3SL150 production devices will be fixed to be backwards compatible with Stratix II devices.

#### Extra $I_{CCL}$ Current Issue

Stratix III EP3SL150 ES devices exhibit an extra 300 mA in current draw from the  $V_{CCL}$  supply in user mode operation. This issue will be fixed in all Stratix III production devices.

#### Dynamic Phase Aligner (DPA) Lock Issue

The DPA circuitry in Stratix III EP3SL150 ES devices fails to lock in some cases. This issue will be fixed in all Stratix III production devices. Contact Altera Technical Support at [www.altera.com/mysupport](http://www.altera.com/mysupport) for more information.



The high speed differential transmitter (TX) and receiver (RX) channels available in Stratix III EP3SL150 ES devices are fully functional and are not affected by this issue.

## Document Revision History

Table 2 lists the revision history for this Errata Sheet.

**Table 2.** Document Revision History

Date and Document Version	Changes Made	Summary of Changes
August 2010, v7.4	<ul style="list-style-type: none"> <li>■ Updated Stratix III MLAB EDCRC errata with updated die revision fix in <a href="#">Table 1</a></li> <li>■ Updated “<a href="#">Updated LVDS Final Timing Model</a>” section</li> </ul>	—
July 2009, v7.3	<ul style="list-style-type: none"> <li>■ Updated “VCCPT Power-Up Issue” section</li> </ul>	—
July 2009, v7.2	<ul style="list-style-type: none"> <li>■ Added “Error Detection CRC Feature, When Enabled, May Cause the MLAB RAM Blocks to Operate Incorrectly” and “Remote System Upgrade Feature” sections</li> </ul>	—
June 2009, v7.1	<ul style="list-style-type: none"> <li>■ Added “CRC Error Injection Feature” section</li> <li>■ Updated “VCCPT Power-Up Issue” section</li> </ul>	—
February 2009, v7.0	<ul style="list-style-type: none"> <li>■ “Updated MLAB Final Timing Model (Affecting a Subset of MLAB Designs)”</li> <li>■ “Updated LVDS Final Timing Model”</li> </ul>	—
November 2008, v6.0	<ul style="list-style-type: none"> <li>■ “Stratix III DPA Misalignment”</li> </ul>	—
September 2008, v5.0	<ul style="list-style-type: none"> <li>■ “VCCPT Power-Up Issue”</li> <li>■ “Error Detection CRC Issue”</li> <li>■ “M9K and M144K RAM Lockup Issue”</li> </ul>	—
July 2008, v4.1	<ul style="list-style-type: none"> <li>■ “JTAG Configuration”</li> </ul>	Note: this was released in error as version 5.0. The correct version is 4.1
June 2008, v4.0	<ul style="list-style-type: none"> <li>■ “Interface Timing Issues with LVDS Hard Macro”</li> <li>■ “DPA Lock Signal Does Not Assert on Some Channels”</li> <li>■ “DPA Circuit Fails to Lock”</li> </ul>	—
April 2008, v3.0	<ul style="list-style-type: none"> <li>■ “ADC No Longer Supported”</li> <li>■ “TSD Must have VCCPT Powered On”</li> <li>■ “Device Reconfiguration Issue”</li> <li>■ “M144K Block Issue”</li> </ul>	—
March 2008, v2.0	<ul style="list-style-type: none"> <li>■ “MLAB RAM Block Size Change”</li> </ul>	—
October 2007, v1.0	<ul style="list-style-type: none"> <li>■ “EP3SL150 ES Device Information”</li> </ul>	—



101 Innovation Drive  
San Jose, CA 95134  
[www.altera.com](http://www.altera.com)  
Technical Support  
[www.altera.com/support](http://www.altera.com/support)

Copyright © 2010 Altera Corporation. All rights reserved. Altera, The Programmable Solutions Company, the stylized Altera logo, specific device designations, and all other words and logos that are identified as trademarks and/or service marks are, unless noted otherwise, the trademarks and service marks of Altera Corporation in the U.S. and other countries. All other product or service names are the property of their respective holders. Altera products are protected under numerous U.S. and foreign patents and pending applications, maskwork rights, and copyrights. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera’s standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera Corporation. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.



I.S. EN ISO 9001