# Arria II GX Device Family Errata Sheet

© August 2009 Errata Sheet

## Introduction

This errata sheet provides updated information about known device issues affecting Arria® II GX devices.

Table 1 shows the specific issues and which Arria II GX devices are affected by each issue.

**Table 1.** Arria II GX Family Issues

| Issue | Affected Devices | Planned Fix |
|---|---|---|
| XAUI State Machine Failure—Channel 0 Shifted by One Cycle<br>Channel 0 data is shifted by one cycle with respect to Channels 1, 2, and 3. | EP2AGX125 ES | EP2AGX125 Production devices |
| High I/O Pin Leakage Current<br>All I/O pins have higher leakage than the published Arria II GX Data Sheet, version 1.2 specifications. | EP2AGX125 ES | All production devices |
| Error Detection CRC Feature<br>When enabled, the Error Detection CRC feature may cause the MLAB RAM blocks to operate incorrectly. | EP2AGX125 ES | EP2AGX125 production devices |
| M9K RAM Block Lock-Up<br>The M9K RAM blocks may lock up due to a glitchy non-PLL clock. | EP2AGX125 ES | EP2AGX125 production devices |
| Automatic Clock Switchover<br>The automatic clock switchover feature may not operate correctly. | EP2AGX125 ES | None |
| Remote System Upgrade<br>The remote system upgrade feature fails when loading an invalid configuration image. | EP2AGX125 ES | Software fix |

## High I/O Pin Leakage Current

I/O pins on ES devices have a higher leakage current than what is specified in the Arria II GX Data Sheet version 1.2. For Arria II GX ES device I/O pin leakage current for all I/O pins, refer to Table 2.

**Table 2.** I/O Pin Leakage Current for Arria II GX ES Devices

| Symbol | Description | Conditions | Min | Type | Max | Unit |
|---|---|---|---|---|---|---|
| $I_I$ | Input pin | $V_I$ = 0V to $V_{CCIOMAX}$ | -80 | — | 80 | µA |
| $I_{OZ}$ | Tri-stated I/O Pin | $V_O$ = 0V to $V_{CCIOMAX}$ | -80 | — | 80 | µA |

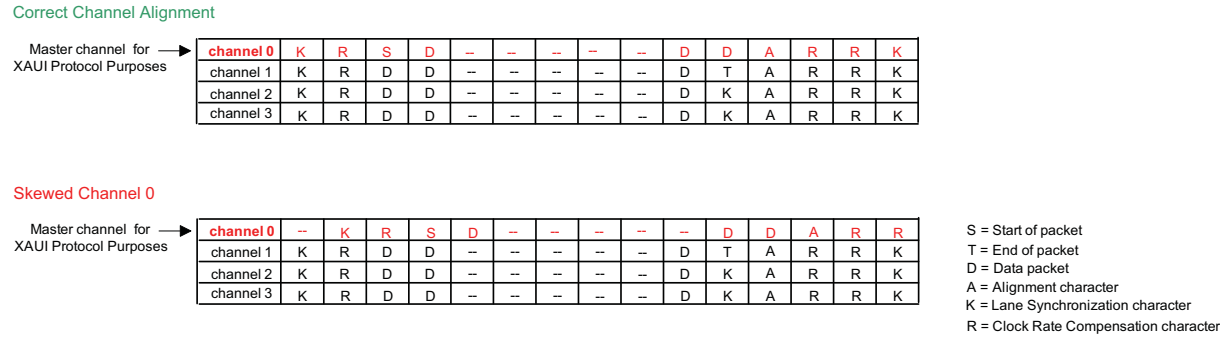
All Arria II GX production devices will have a lower leakage current. Refer to the Arria II GX Data Sheet for production device specifications.

# XAUI State Machine Failure—Channel 0 Shifted by One Cycle

In XAUI functional mode, the data out of the channel 0 Rate Match FIFO may be shifted by one byte with respect to the data of the other three channels. This causes incorrect idle ordered set conversion, resulting in incorrect received parallel data. This issue happens only during initialization or receiver channel reset (assertion of `rx_analogreset` or `rx_digitalreset`).

Figure 1 shows the channel skew.

**Figure 1.** Rate Matcher FIFO Skew




## Workaround

A soft IP solution for this issue is available by contacting Altera.

# Error Detection CRC Feature

The Error Detection CRC feature is typically used to detect single event upsets (SEU). When enabled, the Error Detection CRC feature may cause the memory logic array block (MLAB) RAM to operate incorrectly in Arria II GX ES devices. Only write operations in the MLAB RAM blocks are affected.

The Error Detection CRC feature and CRC error flag operate correctly. FPGA configuration bits are not affected by this issue.

If you do not use Error Detection CRC, no action is required. The MLAB RAM blocks will operate correctly.

If you enable Error Detection CRC, disabling the Error Detection CRC resolves the problem.

Also, using M9K RAM blocks or Logic Cells (LCs) instead of MLAB RAM blocks resolves the problem.

This issue will be fixed in production devices.

# M9K RAM Block Lock-Up

The M9K RAM blocks can lock up if the read clock glitches when `rden=1`, which can occur if the clock source is not from a phase-locked loop (PLL). In this state, a RAM block no longer responds to read or write operations and requires an FPGA reconfiguration to restore operation. The issue occurs in the Read Timer Trigger circuitry, where a glitchy non-PLL clock may inadvertently freeze the Read Timer Trigger circuitry, locking the RAM block in its last operation. All RAM block modes are affected. Memory logic array blocks (MLABs) are not affected.

## Workarounds

The workarounds are to add clock-enable logic, an internal PLL, or clock generation logic (for example, a clock divider). You can add clock-enable logic (internal or external) to disable the RAM block operation until the clock is stable. You can also gate the clock internally or externally. If your FPGA resources permit, use an internal PLL or clock generation logic to ensure a stable clock source at the RAM block input.

This issue will be fixed in production devices.

# Automatic Clock Switchover

The automatic clock switchover feature may fail to operate correctly on Arria II GX devices when the two clocks are running at different frequencies. If both clocks are running at the same frequency, there is no impact to your design. The following modes are affected:

- Automatic
- Automatic with manual override

You may observe two possible issues:

- Switchover from `inclk0` to `inclk1`, even though `inclk0` is active (and vice-versa)
- `clkbad[0,1]` status signals may glitch, even if the input clocks are active

Manual clock switchover mode operates correctly and is not affected by this issue.

There is no planned fix for this issue.

# Remote System Upgrade

The remote system upgrade feature does not operate correctly when you initiate a reconfiguration cycle that goes from a factory configuration image to an invalid application configuration image. In this scenario, the Arria II GX device fails to revert back to the factory configuration image after a configuration error is detected while loading the invalid application configuration image. The failure is indicated by a continuous toggling of the `nSTATUS` pin.

In correct operation, the Arria II GX device should revert back to the factory configuration image after a configuration error is detected with the invalid configuration image.

An invalid application configuration image is classified as one of the following:

- A partially programmed application image
- A blank application image
- An application image assigned with a wrong start address

The remote system upgrade feature works correctly with all other reconfiguration trigger conditions.

## Workaround

A workaround is being implemented in the ALTREMOTE_UPDATE megafunction and will be available in the Quartus II software version 9.1. If you are using the remote system upgrade feature prior to the Quartus II software version 9.1 release, contact Altera® Technical Support at www.altera.com/support for assistance.

# Document Revision History

Table 3 shows the revision history for this errata sheet.

**Table 3.** Document Revision History

| Date and Document Version | Changes Made | Summary of Changes |
|---|---|---|
| August 2009, v2.0 | Added "High I/O Pin Leakage Current" and "XAUI State Machine Failure—Channel 0 Shifted by One Cycle" sections. | — |
| June 2009, v1.0 | Initial release. | — |

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