

This document addresses known errata and documentation issues for the ASI MegaCore function version 1.0.0. Errata are functional defects or errors, which may cause the ASI MegaCore function to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents. [Table 1](#) shows the issues that affect the ASI MegaCore Function v1.0.0.

<i>Table 1. ASI MegaCore Function v1.0.0 Issues</i>	
Issue	Page
Simulation Instructions Incorrect In User Guide	1
Receiver Signals Held in Reset (Stratix II GX Devices Only)	2
VCS Simulator	2
Verilog HDL Error	3
Incorrect Product Page Link In IP Toolbench	3



For the most up-to-date errata for this release, refer to the errata sheet on the Altera website:

www.altera.com/literature/es/es_asi_100.pdf

ASI MegaCore Function v1.0.0 Issues

This section describes the ASI MegaCore function v1.0.0 issues.

Simulation Instructions Incorrect In User Guide

The simulate the design section in the user guide gives the following instruction:

- In a text editor open the simulation batch file, **simulation\modelsim\asi_run.bat**, and edit it to point to your installation of the ModelSim-Altera simulator.

The ModelSim-Altera simulator v6.1d does not have a **win32** directory; it has a **win32aloem** directory

Affected Configurations

This issue affects all simulations in the ModelSim-Altera simulator v6.1d.

Design Impact

If you simulate your design in the ModelSim-Altera simulator v6.1d, it does not work.

Workaround

When using ModelSim Altera 6.1d change line 7 of `\simulation\modelsim\asi_sim.bat` to the following code:

```
set PATH = %MODELSIM_DIR%\win32aloem
```

Solution Status

This issue will be fixed in a future release of the *ASI MegaCore Function User Guide*.

Receiver Signals Held in Reset (Stratix II GX Devices Only)

If you use Stratix II GX transceivers for a receiver design, the ASI uses an incorrect control signal for the transceiver reset and the receiver signals are permanently held in reset.

Design Impact

The design is permanently in reset.

Workaround

Implement the ASI MegaCore function in soft logic—turn on **Use soft logic for transceiver** in IP Toolbench.

Solution Status

This issue will be fixed in a future release of the ASI MegaCore function.

VCS Simulator

The ASI MegaCore function may not work with the VCS simulator.

Affected Configurations

This issue affects all configurations.

Design Impact

If you simulate your design in the VCS simulator, it may not work.

Workaround

Use a different simulator.

Solution Status

This issue will be fixed in a future release of the ASI MegaCore function.

Verilog HDL Error

When you generate a Verilog HDL ASI MegaCore function you may get one of the following errors during compilation:

```
Error (10170): Verilog HDL syntax error at asi_receive.v(97) near text
"generate"; expecting ";", or an identifier ("generate" is a reserved
keyword ), or a sequential statement,
```

```
Error (10170): Verilog HDL syntax error at asi_receive.v(100) near text
"generate"; expecting ":", or "end", or an identifier ("generate" is a
reserved keyword ), or a sequential statement,
```

Affected Configurations

This issue affects all Verilog HDL configurations.

Design Impact

You cannot compile your design.

Workaround

In the Quartus II software on the Assignments menu, click **Settings**. Expand **Analysis and Synthesis settings** and click **Verilog HDL input**. Ensure that you turn on the **Verilog-2001**.

Solution Status

This issue will be fixed in a future release of the ASI MegaCore function.

Incorrect Product Page Link In IP Toolbench

When you click on the product page link in the Documentation window in IP Toolbench, the link fails.

Affected Configurations

This issue affects all configurations.

Design Impact

There is no design impact.

Workaround

Type in the following correct web address into your web browser to view the ASI product page:

www.altera.com/products/ip/iup/additional_functions_iup/m-alt-asi.html

Solution Status

This issue will be fixed in a future release of the ASI MegaCore function.

Contact Information

For more information, contact Altera's mySupport website at www.altera.com/mysupport and click **Create New Service Request**. Choose the **Product Related Request** form.

Revision History

Table 2 shows the revision history for the *ASI MegaCore Function v1.0.0 Errata Sheet*.

Table 2. ASI MegaCore Function v1.0.0 Errata Sheet Revision History		
Version	Date	Errata Summary
1.2	October 2006	Added the Incorrect Product Page Link In IP Toolbench issue.
1.1	May 2006	Added the following issues: <ul style="list-style-type: none">• Simulation Instructions Incorrect In User Guide• Receiver Signals Held in Reset (Stratix II GX Devices Only)
1.0	April 2006	First release.



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