

This document addresses known errata and documentation issues for the ASI MegaCore® function version 6.1. Errata are functional defects or errors, which may cause the ASI MegaCore function to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents. [Table 1](#) shows the issues that affect the ASI MegaCore Function v6.1.

<i>Table 1. ASI MegaCore Function v6.1 Issues</i>	
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For the most up-to-date errata for this release, refer to the errata sheet on the Altera® website:

www.altera.com/literature/es/es_asi_61.pdf

ASI MegaCore Function v6.1 Issues

This section describes the ASI MegaCore function v6.1 issues.

NativeLink Does Not Support Gate-Level Simulation

When using the Nativelink simulation example, the gate level simulation design fails.

Affected Configurations

This issue affects all simulators supported by NativeLink.

Design Impact

This issue only affects simulation and does not affect the design compilation.

Workaround

Perform an RTL simulation of the NativeLink simulation example.

Solution Status

This issue will be fixed in a future release of the ASI MegaCore Function

Functional Simulation Netlist Error

The ASI MegaCore function compiles successfully, but when you try to generate a functional simulation netlist, you get the following error:

```
Error: Can't generate functional simulation netlist because cannot convert  
WYSIWYG primitive pll for a different device family
```

```
Error: Can't elaborate user hierarchy  
"asi_megacore_top:asi_megacore_top_inst|asi_clocks:pll_gen.u_pll|stratix_  
c2_pll_sclk:u_rx_pll|altpll:altpll_component"
```

Affected Configurations

This issue affects all configurations.

Design Impact

This issue affects all Stratix II designs using the **Include PLL** option.

Workaround

Parameterize the transmitter MegaCore function but turn off the **Include PLL** option.

Solution Status

This issue will be fixed in a future release of the ASI MegaCore function.

Timing Errors in Slow Speed Grade Devices

When you turn on **Include PLL** for transmitters you may see timing errors in slow speed grade devices.

Affected Configurations

This issue only affects soft transceiver variations.

Design Impact

The design does not meet timing.

Workaround

Parameterize the transmitter MegaCore function but turn off the **Include PLL** option. Generate the required 27-MHz and 270-MHz from the outputs of the same PLL.

Solution Status

This issue will be fixed in a future release of the ASI MegaCore function.

VCS Simulator

The ASI MegaCore function may not work with the VCS simulator.

Affected Configurations

This issue affects all configurations.

Design Impact

If you simulate your design in the VCS simulator, it may not work.

Workaround

Use a different simulator.

Solution Status

This issue will be fixed in a future release of the ASI MegaCore function.

Compilation Errors when Using Include PLLs Option

When you turn on **Include PLLs** for Stratix® III devices, the design does not compile because of errors.

Affected Configurations

This issue only affects designs on Stratix III devices.

Design Impact

The design will fail in compilation.

Workaround

Parameterize the MegaCore function but turn off **Include PLLs**. Generate the required clock signals from a PLL outside the MegaCore function.

Solution Status

This issue will be fixed in a future release of the ASI MegaCore function.

Contact Information

For more information, contact Altera's mySupport website at www.altera.com/mysupport and click **Create New Service Request**. Choose the **Product Related Request** form.

Revision History

Table 2 shows the revision history for the *ASI MegaCore Function v6.1 Errata Sheet*.

<i>Table 2. ASI MegaCore Function v6.1 Errata Sheet Revision History</i>		
Version	Date	Errata Summary
1.0	December 2006	First release.



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