

This document addresses known errata and documentation issues for the RLDRAM II Controller MegaCore® function version 1.0.0. Errata are functional defects or errors, which may cause the RLDRAM II Controller MegaCore Function to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

RLDRAM II Controller MegaCore Function v1.0.0 Issues

Altera has identified the following issues that affect the RLDRAM II Controller MegaCore function:

- “Initialization May Cause RLDRAM II Devices to Lock Up” on page 1
- “Timing Assignments Information (Missing from User Guide)” on page 2
- “Quartus II Software Version 6.0” on page 3
- “Multiple Instances of the auk_ddr_functions.vhd File” on page 3
- “RLDRAM II Controller Issues a MRS Command Instead of a Refresh Command” on page 4
- “Multiple VHDL Support Files” on page 4
- “Gate-Level Simulation Filenames” on page 5
- “Non-integer Feedback Clock Phase Values” on page 6
- “Unpredictable Results for Gate-Level Simulations (HardCopy II Devices only)” on page 7
- “Editing the Custom Variation (non-DQS Mode)” on page 7



For the most up-to-date errata for this release, refer to the errata sheet on the Altera® website:

www.altera.com/literature/es/es_rldram_ii_100.pdf

Initialization May Cause RLDRAM II Devices to Lock Up

When interfacing with RLDRAM II devices, the power-up sequence of the Stratix® II or Stratix II GX devices may cause the attached RLDRAM II devices to become locked-up or to be put into an unknown state.

Affected Configurations

This issue affects all configurations.

Design Impact

The RLDRAM II device locks up or goes into an unknown state.

Workaround

There is no hardware workaround. You can use a dummy read sequence to clear portions of the RLDRAM II devices. Contact your RLDRAM II vendor for more details.

Solution Status

This issue is fixed in the RLDRAM II controller v6.1.

Timing Assignments Information (Missing from User Guide)

When generating an RLDRAM II controller that connects to RLDRAM II devices that have more than a single pair of QK output read strobes (18-bit or 36-bit RLDRAM II devices), you must apply timing assignments to the project. These timing assignments guarantee safe data transfer between the capture QK clock domain and another QK clock domain inside the FPGA. IP Toolbench automatically generates the timing assignments that are applied to the Quartus II project.

The following example is for a 18-bit RLDRAM II controller that is connected to an 18-bit RLDRAM II device, for example an MT49H16M18FM-25. The read data, DQ[17:9] is captured by QK[1] and is transferred to the QK[0] clock domain inside the FPGA.

From the datasheet the skew between QK[0] and QK[1] is given by the following equation:

$$\begin{aligned}\text{Skew} &= t_{\text{QKQ}} - (t_{\text{QKQ0}} \text{ or } t_{\text{QKQ1}}) \\ &= \pm 300 \text{ ps} - \pm 200 \text{ ps} \\ &= \pm 100 \text{ ps}\end{aligned}$$

So the worst case skew between QK[0] and QK[1] is ± 100 ps. Therefore, you must apply a clock uncertainty of ± 100 ps to the RLDRAM II interface when transferring between QK[1] and QK[0] clock domains. With a ± 50 -ps board skew, you can set the following `clock_setup_uncertainty` and `clock_hold_uncertainty` timing assignments in the Quartus II Assignment Editor for your project:

```
rldramii_qk[1] rldramii_qk[0] Clock Setup Uncertainty 0.15 ns Yes
rldramii_qk[1] rldramii_qk[0] Clock Hold Uncertainty 0.15 ns Yes
```

These assignments are required for each attached 18 or 36-bit RLDRAM II device from the capture QK clock domain to the the target QK clock domain.

This issue is fixed in the RLDRAM II controller v6.1.

Quartus II Software Version 6.0

The RLDRAM II Controller MegaCore Function version 1.0.0 is not compatible with the Quartus II software v6.0.

Affected Configurations

This issue affects all configurations.

Workaround

If you want to use the Quartus II software v6.0, upgrade to the RLDRAM II Controller MegaCore Function version 1.1.0.

Solution Status

This issue will never be fixed.

Multiple Instances of the auk_dds_functions.vhd File

When a project contains multiple memory MegaCore functions, the Quartus® II project has multiple instances of the **auk_dds_functions.vhd** file (one per MegaCore function).

Affected Configurations

This issue affects all configurations.

Design Impact

The Quartus II project fails during compilation.

Workaround

Remove the **auk_dds_functions.vhd** file associated with the RLDRAM II controller from the list of files added to the Quartus II project, by choosing **Add/Remove Files from Project** (Project menu). Keep only the **auk_dds_functions.vhd** file associated with the DDR or DDR2 SDRAM controller.

Solution Status

This issue will be fixed in a future version of the RLDRAM II controller.

RLDRAM II Controller Issues a MRS Command Instead of a Refresh Command

When you request a refresh in the clock cycle after a write request at the local interface, the RLDRAM II controller issues a MRS command instead of a refresh command.

Affected Configurations

This issue affects all configurations.

Design Impact

Your design works incorrectly.

Workaround

Do not request a refresh in the clock cycle that directly follows a write request at the local interface.

Solution Status

This issue will be fixed in a future version of the RLDRAM II controller.

Multiple VHDL Support Files

The following Altera MegaCore functions generate the Altera VHDL support package (**altera_vhdl_support.vhd**):

- DDR or DDR2 SDRAM Controller MegaCore function
- QDR II SRAM Controller MegaCore function
- RLDRAM II Controller MegaCore function
- PCI Express MegaCore function

When you have a Quartus II project that contains multiple MegaCore functions that are in separate directories, there are multiple instances of the **altera_vhdl_support.vhd** file. If the Quartus II compilation adds two or more separate copies of **altera_vhdl_support.vhd**, the compilation fails.

Affected Configurations

This issue affects all configurations.

Design Impact

There is no design impact.

Workaround

Either generate all the project MegaCore functions in the Quartus II project directory, or ensure only one instance of the **altera_vhdl_support.vhd** file exists in your project.



Ignore the warning that IP Toolbench running outside of SOPC Builder generates, when it overwrites an existing **altera_vhdl_support.vhd** file.

To ensure your project only includes one instance of the **altera_vhdl_support.vhd** file, follow these steps:

1. Choose **Add/Remove Files in Project** (Project menu).
2. Choose all instances of **altera_vhdl_support.vhd** except the first instance.
3. Click **Remove**.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Gate-Level Simulation Filenames

Various Quartus II software options may cause it to generate a netlist with a different filename to that expected by the gate-level simulation script. The simulation script expects *<project name>.vho* or *.vo* and *<project name>_v* or *_vhdl.sdo* files to be present.

Affected Configurations

This issue affects all configurations.

Design Impact

You cannot run gate-level simulations.

Workaround

For VHDL gate-level simulations, in the **simulation/modelsim** directory follow these steps:

1. Rename *<filename>.vho* file to *<project name>.vho*.
2. Rename *<filename>.sdo* file to *<project name>_vhd.sdo*.

For Verilog HDL gate-level simulations, in the **simulation/modelsim** directory follow these steps:

1. Rename the *<filename>.vo* file to *<project name>.vo*.
2. Rename the *<filename>.sdo* file to *<project name>_v.sdo*.
3. In the *<project name>.vo* file change the following line to point to the *<project name>_v.sdo* file:

```
initial $sdf_annotate("<project name>_v.sdo");
```

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Non-integer Fed-Back Clock Phase Values

If you enter a non-integer clock phase into **Feedback PLL phase offset**, when you click **Generate**, IP Toolbench shows a MegaCore Function Generation Failed error and fails to generate a MegaCore function.

Affected Configurations

This issue affects all configurations.

Design Impact

IP Toolbench fails to generate your custom MegaCore function.

Workaround

Ensure that only integer values are entered into **Feedback PLL phase offset**.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Unpredictable Results for Gate-Level Simulations (HardCopy II Devices only)

Gate-level simulations may not work as expected on HardCopy® II devices, because HardCopy II timing is preliminary in the Quartus II software version 5.1.

Affected Configurations

This issue affects all configurations on HardCopy II devices.

Design Impact

There is no design impact.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the Quartus II software.

Editing the Custom Variation (non-DQS Mode)

When you generate a non-DQS mode custom variation with wide databus widths, you may encounter one of the following characteristics when you try to edit the custom variation:

- IP Toolbench does not reload
- IP Toolbench reloads, but the databus width and constraints are set to the default for the selected RLDRAM II device
- IP Toolbench reloads, but the databus width is set to the default value for the selected RLDRAM II device and the constraints floorplan shows no chosen byte groups

Affected Configurations

This issue affects non-DQS mode designs only.

Design Impact

There is no design impact, if you implement the workaround.

Workaround

Use one of the following workarounds:

- If IP Toolbench does not reload, you must regenerate a new custom variation and re-enter your parameters
- If IP Toolbench reloads, but the databus width and constraints are set to the default, reselect the databus width and rechoose the byte groups in the constraints floorplan
- If IP Toolbench reloads, but the databus width is set to the default and the constraints floorplan shows no byte groups, reselect the databus width and rechoose the byte groups in the constraints floorplan

Solution Status

This issue will be fixed in a future version of the RLDRAM II controller.

Contact Information

For more information, contact Altera's mySupport website at www.altera.com/mysupport and click **Create New Service Request**. Choose the **Product Related Request** form.

Revision History

Table 1 shows the revision history for the RLDRAM II Controller MegaCore function v1.0.0.

Version	Date	Errata Summary
1.6	November 2006	Changed Solution Status for: <ul style="list-style-type: none"> ● Initialization May Cause RLDRAM II Devices to Lock Up ● Timing Assignments Information (Missing from User Guide)
1.5	October 2006	Added "Initialization May Cause RLDRAM II Devices to Lock Up" issue.
1.4	October 2006	Added "Timing Assignments Information (Missing from User Guide)" issue.
1.3	May 2006	Added "Quartus II Software Version 6.0" issue.
1.2	January 2006	Added "Multiple Instances of the auk_ddr_functions.vhd File" issue.
1.1	November 2005	Added "RLDRAM II Controller Issues a MRS Command Instead of a Refresh Command" issue.
1.0	October 2005	First release.



101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
www.altera.com
Applications Hotline:
(800) 800-EPLD
Literature Services:
literature@altera.com

Copyright © 2006 Altera Corporation. All rights reserved. Altera, The Programmable Solutions Company, the stylized Altera logo, specific device designations, and all other words and logos that are identified as trademarks and/or service marks are, unless noted otherwise, the trademarks and service marks of Altera Corporation in the U.S. and other countries. All other product or service names are the property of their respective holders. Altera products are protected under numerous U.S. and foreign patents and pending applications, maskwork rights, and copyrights. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera Corporation. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

